LTC3882 ERRATA

This errata describes the conditions that cause an LTC®3882 device to operate differently than expected or as described in the data sheet.

REVISION HISTORY

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ERRATA #1: RESTORE_USER_ALL

The device does not use external resistor configuration when RESTORE_USER_ALL is executed, even if bit 6 of MFR_CONFIG_ALL_LTC3882 is clear.

Conditions:

The following conditions, when present simultaneously, may expose this problem:

1. External resistor configuration is used to set any portion of the device behavior instead of EEPROM.
2. A RESTORE_USER_ALL command is issued to the device.

Impact:

Communication at the expected device address can be lost when the above conditions occur. The LTC3882 always responds at global addresses 0x5A and 0x5B, but writing data to these locations is not recommended. Output voltages, PWM frequency or phasing may be incorrect.

Root Cause:

Internal firmware does not use external programming resistors to set device configuration when RESTORE_USER_ALL is executed, regardless of the state of bit 6 of MFR_CONFIG_ALL_LTC3882. Only values stored in EEPROM are applied.

Additional RESTORE_USER_ALL Deviations:

RESTORE_USER_ALL does not execute the full device initialization described in the "Power Up and Initialization" segment of the data sheet Operations section. This command will not execute when the die temperature is above 130°C, which does not agree with statements in the "Internal EEPROM with CRC" and "Hardwired PWM Response to Temperature Faults" Operations section segments. No faults are cleared by execution of RESTORE_USER_ALL, though this is indicated throughout the data sheet. When this command is executed, only the related EEPROM contents are copied to RAM PMBus command space after disabling both PWM channels, if either is on. Channels that are then configured to be on will not be enabled after RAM is loaded until that channel's MFR_RESTART_DELAY has expired.

Workarounds:

Several workarounds are possible, depending on the system configuration and requirements. Additional workarounds may be possible. Contact LTC Factory Applications for assistance.

Use MFR_RESET – Where resistor configuration is necessary, MFR_RESET can be used in lieu of RESTORE_USER_ALL to load all PMBus command values from EEPROM into working RAM while properly applying settings programmed by external resistors.

Program the Device Strictly With EEPROM – The desired value of bus address, output voltage, and PWM frequency and phase can be programmed into EEPROM by issuing the appropriate PMBus commands, setting bit 6 of MFR_CONFIG_ALL_LTC3882, and issuing a STORE_USER_ALL command. At that point, the ASEL0/1 pins should be left open to ensure power-up behavior is self-consistent. Once the device is configured in this fashion, RESTORE_USER_ALL can be executed at any time without error. EEPROM configuration can also be loaded during the production process. Contact LTC sales for details.

ERRATA #2: EXTERNAL SYNC INPUT

The device may not properly lock to an external SYNC input that has high or low duty cycle.

Conditions:

The following conditions, when present simultaneously, may expose this problem:

1. An external SYNC source is applied to the LTC3882.
2. The external SYNC source has a duty cycle outside of the range of 40% to 60%.
3. Bit 4 of MFR_CONFIG_ALL_LTC3882 (SYNC output disable) is not set.
4. Internal FREQUENCY_SWITCH is set to a frequency greater than 1.2 times the applied external SYNC.

Impact:

Clocking provided to the internal PLL that generates the PWM oscillator can be irregular when the above conditions occur. This may prevent the PLL from maintaining lock and/or create additional jitter on PWM control outputs.

Root Cause:

The acceptance criteria programmed by internal firmware into the device's SYNC contention resolution filter is too restrictive in cases where SYNC duty cycle is not close to 50%.

Workarounds:

Several workarounds are possible, depending on the system configuration and requirements. Additional workarounds may be possible. Contact Linear Factory Applications for assistance.

Disable Unused SYNC Outputs – In all system configurations, this issue is mitigated by setting bit 4 of MFR_CONFIG_ALL_LTC3882 on any ICs that are not to function as a clock master, as recommended in the LTC3882 data sheet. Additional workarounds detailed below may still be necessary.

Adjust External SYNC Duty Cycle – In cases where an external SYNC source is required, selecting a source that can reliably provide duty cycles between 40% and 60% will allow the LTC3882 to recognize and capture the external SYNC signal as long as its frequency is greater than 50% of the FREQUENCY_SWITCH command value, as the data sheet indicates.

Adjust Internal FREQUENCY_SWITCH – In cases where an external SYNC source is required, and that source cannot reliably provide duty cycles between 40% and 60%, setting the internal FREQUENCY_SWITCH to a value not higher than 1.2 times the external SYNC frequency will allow the LTC3882 to recognize and capture the external SYNC signal.

Disable LTC3882 Clock Master – In cases where an external SYNC source is required and that source cannot reliably provide duty cycles between 40% and 60%, disabling the SYNC output of *all* LTC3882s sharing SYNC (bit 4, MFR_CONFIG_ALL_LTC3882) will allow an external SYNC input to be recognized and captured as long as its frequency is greater than 50% of the FREQUENCY_SWITCH command value. However, the LTC3882 PWM channels will not operate synchronously without application of external SYNC if this approach is used.

ERRATA #3: BOOST REFRESH PULSE WIDTH

Boost refresh pulse width cannot readily be programmed to 50ns or 250ns.

Conditions:

This issue occurs at all valid operating conditions.

Impact:

Only two boost refresh pulse widths are readily available: 25ns (the effective factory EEPROM default) and 125ns, according to the following table. The value written to MFR_PWM_MODE_LTC3882 is correctly retrieved by a PMBus read of this command.

MFR_PWM_MODE Supported Values

BIT	MEANING
7	Output voltage range select 0: Maximum V_{OUT} = 5.25V 1: Maximum V_{OUT} = 2.65V
6*	Enable V_{OUT} servo
5	External temperature sense 0: ΔV_{BE} measurement 1: Direct voltage measurement
4:3	BOOST refresh width 11b: 125ns 10b: 125ns 01b: 25ns 00b: 25ns
2:1	PWM control protocol 11b: Independent TG/BG control outputs 10b: Two-State PWM output (with active-low OD, open-drain) 01b: Two-State PWM output (with active-high EN) 00b: Three-State PWM output (EN pin selects sub-protocol, refer to Applications Information)
0	PWM mode 0: Forced discontinuous inductor current 1: Discontinuous inductor current

*This bit is ignored (servo disabled) if MFR_VOUT_AVP for this channel is programed to a value greater than 0%.

Root Cause:

Internal firmware does not move bit[3] of MFR_PWM_MODE_LTC3882 to the proper hardware register. This bit in the hardware register retains its POR value of 0 when MFR_PWM_MODE_LTC3882 is written.

Workarounds:

Several workarounds are possible, depending on the system configuration and requirements. Additional workarounds may be possible. Contact LTC Factory Applications for assistance.

Use Continuous Conduction Mode for the Choke – If light load efficiency is not a major concern, simply select Forced Continuous Inductor Current by setting bit[0] in MFR_PWM_MODE_LTC3882 to 0. In this mode, the boost refresh pulse width setting is not used. The top-side FET boost supply reservoir capacitor will automatically be refreshed every PWM cycle.

Select an Appropriate Power Stage Design – If DCM operation is desired for light load efficiency, select a power stage design that will allow boost capacitor refresh with a bottom FET ON pulse width of 25ns or 125ns. The selected width should allow the pump capacitor to charge to the minimum VGS required by the top power FET for switching in its SOA, plus one diode drop. The LTC3882 will only allow a maximum of eight PWM cycles in DCM without some form of boost refresh.

ERRATA #4: VOUT_TRANSITION_RATE

Actual margin or VOUT_COMMAND transition rates may be inaccurate for very slow voltage changes when the output is in low range.

Conditions:

The following conditions, when present simultaneously, may expose this problem:

1. Output range set to low (bit[7] = 1, MFR_PWM_MODE_LTC3882).
2. VOUT_TRANSITION_RATE set below 10mV/ms.

Impact:

Errors of more than 20% can exist in the time required to transition to the next programmed output voltage. Generally, the error will tend to create a faster transition than programmed.

Root Cause:

An internal firmware constant for handling calculation remainders is incorrect in low range.

Workarounds:

Several workarounds are possible, depending on the system configuration and requirements. Additional workarounds may be possible. Contact LTC Factory Applications for assistance.

Use Higher V_{OUT} Transition Rates – Increasing the programmed value of VOUT_TRANSITION_RATE to 10mV/ms or more will produce reasonably accurate output transitions in both output voltage ranges.

Use High Range for Programming V_{OUT} – Set MFR_PWM_MODE_LTC3882 bit[7] to 0 to select high range for programming V_{OUT}. Output transitions will be consistent with the programmed value of VOUT_TRANSITION_RATE over the entire range specified in the data sheet.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/15	Added Errata 3 and 4	3, 4

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