INTRODUCTION

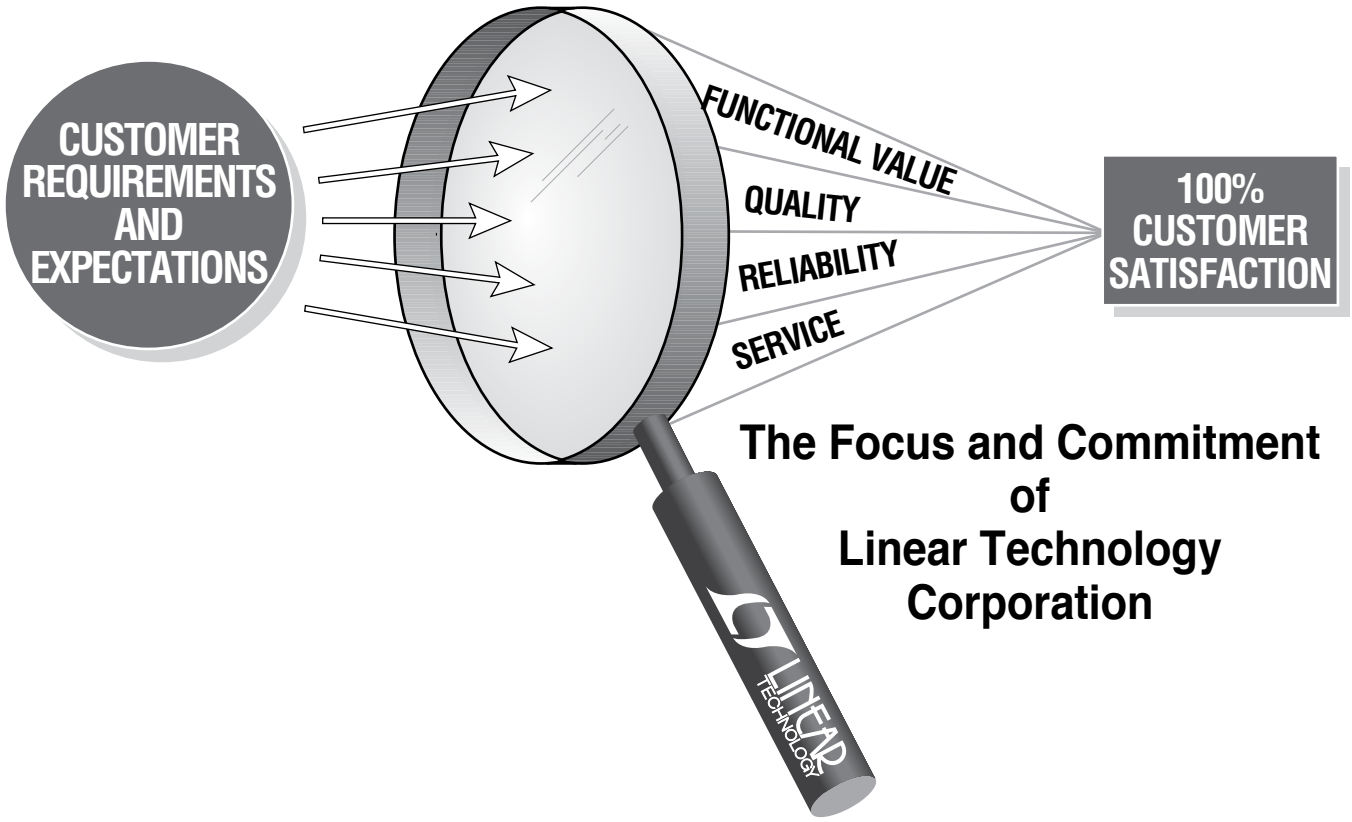
In 1981 Linear Technology Corporation was founded with the intention of becoming a world leader in high performance analog semiconductors. To achieve this goal Linear Technology Corporation committed itself to consistently meet its customers' needs in four areas:

- ❒ Functional Value
- ❒ Quality
- ❒ Reliability
- ❒ Service

Linear Technology Corporation has achieved its primary goal and is now focused to achieve 100% customer satisfaction.

This brochure defines the key elements of Linear Technology Corporation's Reliability Assurance Program which is divided into three groups:

- ❒ Reliability Planning
- ❒ Manufacturing for Reliability
- ❒ Reliability Assessment and Improvement



RELIABILITY PLANNING

Reliability planning takes three forms at Linear Technology Corporation (LTC). The first is the establishment of the reliability requirements for a product to be released to manufacturing. The second is the definition and implementation of a predictive reliability system. The third is designing for reliability, which includes new product development, materials selection, and construction techniques.

We fully realize that the cost of failure in the field is many orders of magnitude more than the initial component cost. Therefore, the goal of the reliability planning process is to provide reliable product to reduce the cost of ownership to our customers.

Reliability Criteria

A key element of reliability planning is LTC's internal specification entitled "Quality Assurance/Reliability Assurance Qualification Requirement." It contains a complete description of the interrelationships of the various groups involved in meeting LTC's reliability objectives and defines the guidelines for release decisions which affect quality and reliability of the device.

Predictive Reliability System

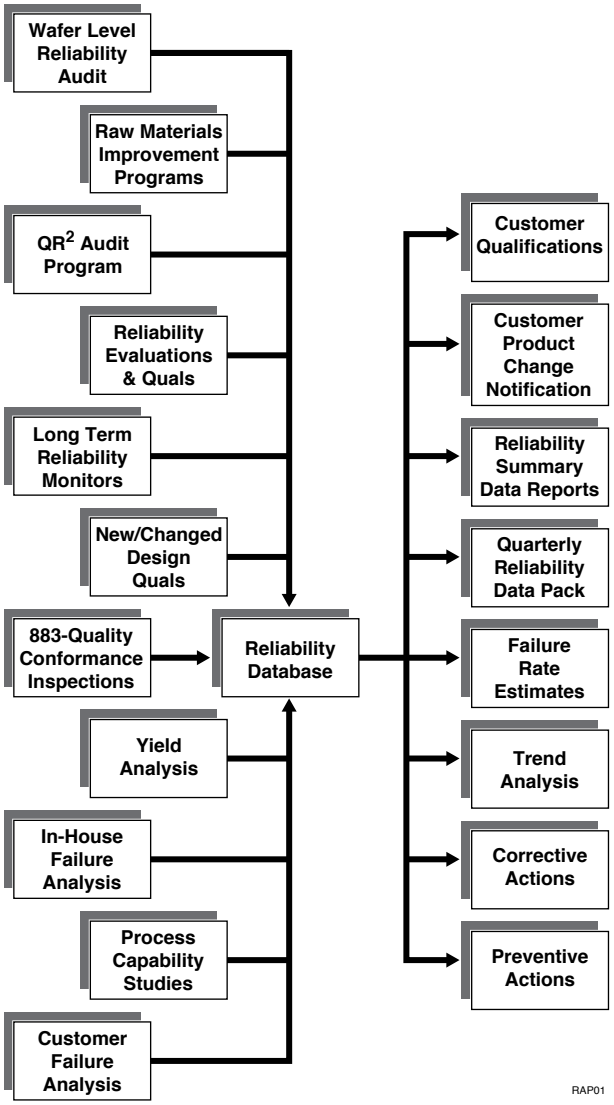
LTC has developed a predictive reliability system which combines quality and reliability information in a database to provide reliability summaries and trend analysis. A block diagram of the system is shown on this page.

Designing for Reliability

Considerable planning goes into the design of LTC's products. This planning includes device layout considerations, selection of input and output protection schemes, selection of fab processing technology, and specification of materials and manufacturing techniques.

A stringent set of bipolar and CMOS design rules have been established to enhance reliability and optimize manufacturability through robust design. At the design stage the reliability of the circuit is heavily dependent on layout considerations. The rules for thickness and width of metallization have been defined to minimize the current density and prevent electromigration. Current density calculations are required to be performed on all products to ensure that the designs are conservative. The routing of the metal pattern is designed to eliminate potential inversion or leakage failures and guard ring structures are used where appropriate. The positions of bonding pads are carefully selected to optimize device performance and also to fit easily into a variety of packages without creating potential bond loop problems that could result in shorted wires.

The Predictive Reliability System

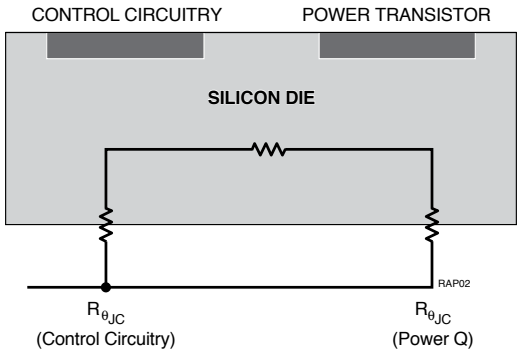


The thermal layout of our circuits also receives considerable attention to minimize parametric drift and optimize performance. In the case of voltage regulators, for any given power dissipation, there will be some temperature difference between the power transistor and the control circuitry due to their separation on the die. This temperature difference is a desirable situation which is used to reduce the power transistor's temperature effect on the control circuitry. Additionally, the power transistor has a

higher maximum junction temperature rating than that of the control circuitry and may be allowed to run warmer without degradation. Such LTC products are also designed for maximum efficiency to reduce power dissipation and thereby improve reliability and reduce the cost of heat sinking in the customer's product.

All of our voltage regulators include thermal limiting in the circuitry to shut down the device if the temperature exceeds the safe operating conditions. Additional insurance is provided by employing short-circuit current protection to safeguard against catastrophic failure. The philosophy of incorporating fault-tolerant designs with innovative circuit protection concepts is a fundamental design rule at LTC.

Thermal Resistance Model of LTC's Voltage Regulators



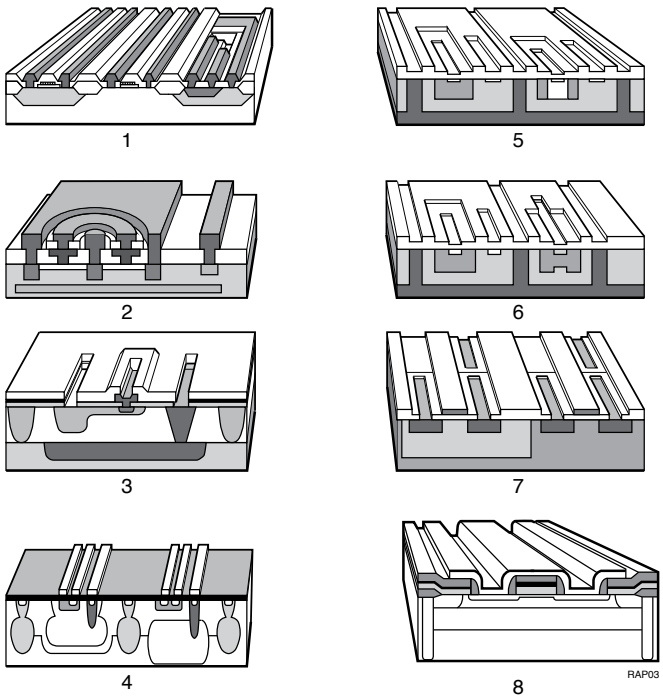
Another major design consideration in circuit reliability is tolerance to electrostatic discharge (ESD) and electrical overstress (EOS). ESD is a problem encountered both in normal handling and circuit assembly. It also affects the reliability of the final product when cables are exposed to ESD such as in line drivers and receivers.

The implementation of ESD protection structures in linear integrated circuits is much more difficult than in digital circuits. The linear circuit must provide protection for electrical overstress while maintaining the ability to measure current levels in the picoamp range. Interface circuits have input and output connections that normally operate at voltages in excess of the power supply, thereby precluding the use of clamp structures to the power supply for ESD protection. LTC, using a combination of circuit design and proprietary structures, provides high levels of overstress immunity to its devices which enhances their reliability. As a goal, all devices are designed for a minimum of 2,000V ESD protection with some devices achieving 5,000V to 10,000V ESD protection.

Linear circuits with total supply currents in the microamp range cannot tolerate leakages induced by contamination. Whether the circuit is bipolar, CMOS or complementary bipolar, the circuit must withstand high operating voltage and high temperature for thousands of hours without leakage currents degrading device performance. LTC uses advanced process techniques to shield the die from sodium contamination while preventing electron accumulation causing surface inversions. This, combined with continuous monitoring of the assembly process, ensures high reliability devices.

LTC utilizes state-of-the-art processes in manufacturing its products. Our high voltage bipolar process provides high gain, low noise general purpose devices as well as high power integrated circuits. CMOS can provide high complexity ICs with a large digital content. Complementary bipolar, a new process developed in-house by LTC, provides high speed NPNs and PNPs on the same monolithic die. Complementary bipolar enables an expanded product range for linear circuits and is suitable for very high speed amplifiers, general purpose linear signal processing or even high speed D/A converters. All of these products are characterized by high reliability, low power consumption and the ability to operate from a wide range of power supplies and over a wide range of ambient temperatures.

LTC's Process Structures



1. N-Well CMOS/BiCMOS
2. Poly J-FET
3. High Speed Bipolar
4. Complementary Bipolar
5. Super Beta Structure
6. BiFET Structure
7. Silicon Gate CMOS Structure
8. RF (High Frequency)

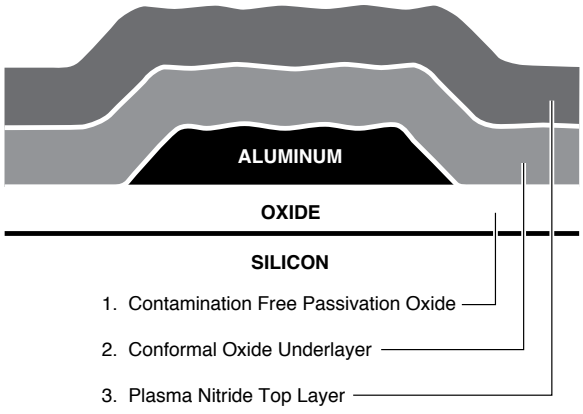
In order to ensure that device performance and reliability goals are achieved on new products, design review meetings are held regularly during the design and development phase.

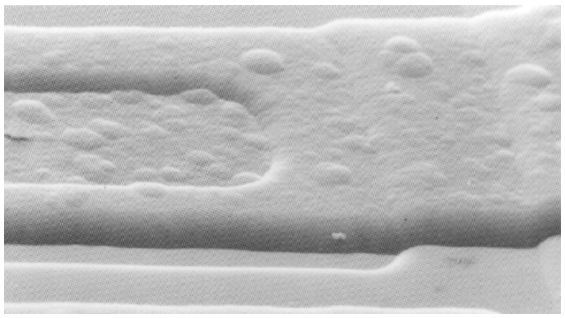
Material Selection

LTC has selected assembly processes and materials that are closely matched to achieve the highest reliability level in both ultra-precision and high power devices. Compatibility between the different package elements, such as the molding compound and lead frame, are carefully researched and qualified. The choice of materials and assembly processes is especially critical in surface mount devices, which must maintain reliability after being subjected to harsh board soldering environments. At LTC we are using the latest state-of-the-art assembly equipment and materials to guarantee reliability. Our low stress epoxy molding compound is extremely low in ionic impurities.

Similar improvements have been made in hermetic packages in the modern low temperature glass ceramic seals and improved die attach materials.

LTC's Dual Layer Passivation System





RAP04

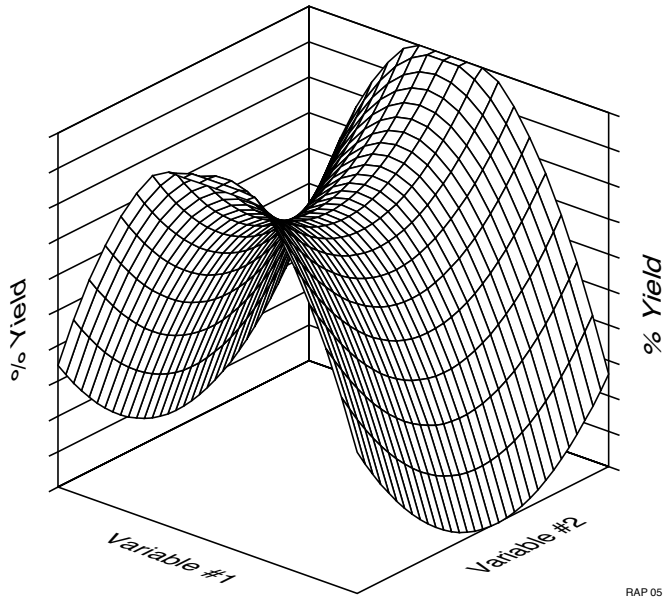
To protect the die from degradation before assembly, and from the long term effects of the package environment, LTC has developed a proprietary dual layer passivation. This dual layer passivation system is free from cracks and pinhole defects and offers an outstanding moisture barrier without detrimental side effects to device performance.

Design of Experiments

LTC is committed to the use of design of experiments (DOE) when developing new products and processes. We firmly believe that design of experiments will be the new industry standard for product and process development.

DOE has been successfully utilized on numerous products and processes at LTC. DOE, coupled with response surface methodology, has provided LTC the ability to solve complex problems that were previously unsolvable. We have used DOE to characterize wafer fab processes and provided this information to our IC designers which enabled them to produce devices that were less sensitive to manufacturing variations.

Response Surface Model of PIND Yield after Welding Operation



RAP 05

MANUFACTURING FOR RELIABILITY

LTC is keenly aware of the influence which the manufacturing process has on the quality and reliability of the finished product. For this reason, LTC has placed critical emphasis on the manufacturing facility and associated process controls. LTC's claims of outstanding manufacturing capability and controls are validated by the fact that we achieved Class S Certification by DESC in November of 1987.

LTC's strategy in manufacturing for reliability includes the use of automated state-of-the-art equipment, protection of the product as it moves through manufacturing, effective inspection and screening, device traceability and statistical process control. These and other similar tight controls are applied from wafer fabrication through product shipment.

Wafer Fab

In wafer fabrication, the key to a reliable process is process control. Two major thrusts of process control in the wafer fab are the application of statistical process control (SPC) and the use of automated processing equipment. Automated equipment employing cassette-to-cassette wafer transfer, proximity mode aligners and projection steppers has significantly reduced handling related defects.

Projection Stepper

RAP 06

Microprocessor-controlled furnaces are used to eliminate the effects of process variations and human errors. Thin film processing employs fully automated sputtering and metal etch systems.

Automated Metal Etch System

RAP 07

All of these equipment enhancements work together to yield a process that is consistent and repeatable with a minimum of wafer handling. Quality control monitors and inspections at various points in the process, coupled with the use of control charting throughout the fab area, ensure consistent processing. The quality of the oxide is checked regularly using CV plots to check for contamination and surface state anomalies. Scanning electron microscope inspection is performed periodically each day to ensure the integrity of the metallization system.

Assembly

The introduction of new equipment and techniques in the assembly process has had a tremendous impact on device reliability. The use of automated equipment has reduced the handling and subsequent damage of die and wafers. In situations where die or wafers must be handled, vacuum wands and vacuum pens have replaced tweezers and thereby decreased damage due to scratches. Automated wire bonding machines have produced more consistent wire bonding quality and improved productivity.

All products receive a thorough visual inspection per Mil-Std-883 Method 2010 Condition B or an equivalent visual criteria prior to encapsulation.

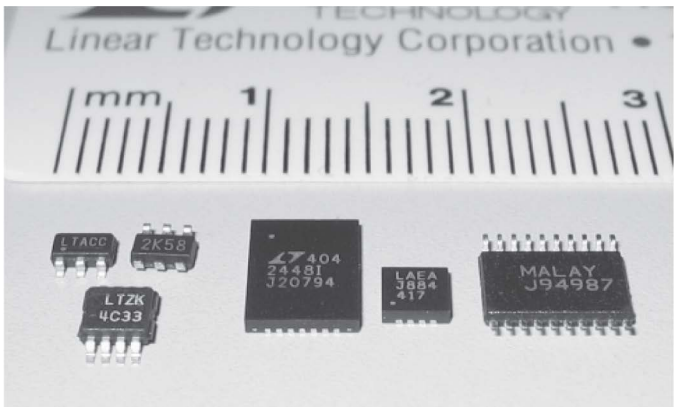
High Speed Automatic Bonder

RAP 08

Traceability

LTC has an outstanding traceability control system. A traceability mark is used to code information including the country of assembly, assembly facility, exact assembly lot seal date, wafer fab lot, die type and revision. Additionally, this traceability mark will identify any nonstandard processing which may have been required using a custom flow. At the wafer level, each wafer is laser-scribed to include the fab run number and wafer serial number. This traceability benefit is offered as a standard feature on all packages where space allows and is part of the "added value" of LTC products.

Traceability Control Using an Identifying Mark Coding



RAP 09

To enhance traceability LTC is using the latest state-of-the-art document archival system. This computerized system incorporates a document scanner which digitizes and compresses documents to be stored on optical disks. As the documents are stored, their ID number, date and classification are recorded in the system's database to facilitate retrieval. This system allows fab travelers, test travelers and other critical documents to be retrieved in minutes as opposed to hours or days.

Optical Disk Archive System

RAP 10

Reliability Screening

Although our standard product families are recognized for their very low infant mortality, customer-requested additional reliability screening can be provided by LTC. This added reliability screening for commercial or industrial level products is offered for both hermetic and plastic devices and is designated as our "R" flow process signified by a /R symbol as a suffix to the part number.

The "R" flow includes temperature cycle, burn-in and QA testing at 0°C, 25°C, and 70°C. A simplified flow chart of the "R" flow is shown in Table 1 at the end of the Reliability Assurance Program section. The hermetic devices are also offered as JAN Class S or Class B, Standardized Military Drawings (SMDs) and also as MIL-STD-883 devices.

LTC offers a cost-effective reliability screen for hermetic product using the MIL-STD-883 screening and quality conformance inspection. This flow is defined in our "MIL-STD-883" brochure and depicted in a brief flow diagram shown in Table 2.

The MIL-STD-883 burn-in at 125°C for 160 hours is roughly equivalent to 80,000 hours or approximately 9 years of continuous operation at a normal operating temperature of around 55°C (assuming an activation energy of 1.0 electron volts).

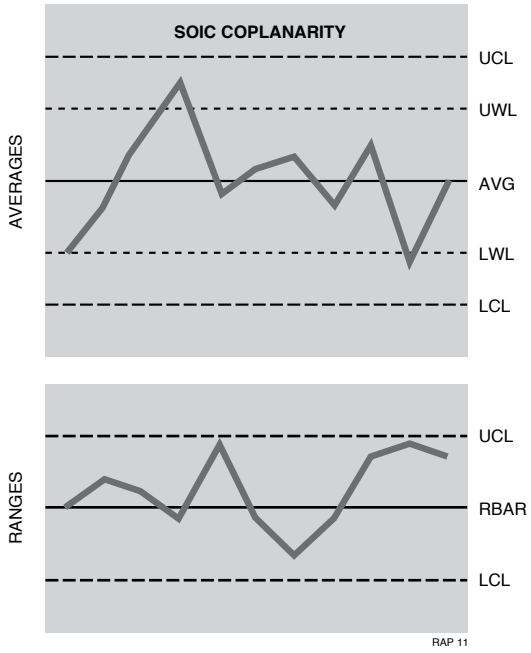
Whether testing plastic or hermetic devices, the engineers at LTC routinely add tests in addition to the standard data sheet tests. These added tests are used to detect potential flaws that could impact reliability and provide additional device compatibility with subtle application-related performance characteristics. Examples of such additional tests are the exercising of thermal shutdown mode of regulators prior to burn-in or the stressing of on-chip capacitors with voltages in excess of the device maximum rating to induce failure in substandard lots.

Data sheet electrical parameters are measured before and after the specified stress testing to ensure the electrical integrity of the devices.

Statistical Process Control

At LTC we believe that quality and reliability should be built into a product as opposed to simply screening out bad devices. Statistical process control (SPC) is ideally suited to our manufacturing goals. SPC has enabled us to run processes with uniform and centered distributions which have not only optimized yields, but have also produced a finished product that is rugged and reliable.

Example of Control Chart for SOIC Coplanarity



Control charting at all critical processes is used to identify the need for corrective action before an out-of-control situation occurs, thus reducing the overall process variation. LTC has an active SPC program. The generic process from wafer fabrication through shipping has been flow-charted with critical nodes defined. The Control Plan Detail outlines the various attributes of the activities surrounding that particular activity. Organization for SPC is comprised of the:

- Steering Committee
- SPC Quality Control Teams (QCTs)
- Process/Preventive Action Teams (PATs)

The Steering Committee provides the leadership for the SPC process, while the QCTs are responsible for the implementation and maintenance of SPC within their respective operational groups. PATs are formed by the QCTs to implement certain initial or corrective measures with specific stated goals using SPC tools. There are four QCTs in place:

- Wafer Fab
- Quality and Reliability
- Local Assembly
- End-of-Line (which includes Test, Mark, Pack, Product and Test Engineering)

Since, by definition, a PAT functions until its stated goal is attained, their number and tasks are constantly changing. We have had as many as 23 active PATs which include operators and maintenance personnel.

Training is provided in-house for a majority of LTC's employees, who receive test materials and instruction in one or more of the following courses:

- Basic SPC
- Advanced SPC
- Design of Experiments
- Team Organization

An important aspect of the SPC program at LTC involves the use of Design of Experiments to solve specific problems, develop new products/processes, and characterize new products and/or processes.

RELIABILITY ASSESSMENT AND IMPROVEMENT

LTC combines a traditional approach to reliability which incorporates product qualification and long term reliability assessment with a "leading edge" approach, which incorporates wafer level reliability testing and in-line assembly reliability monitoring.

Qualification Testing

Before a new product can be released to production, strict qualification testing requirements must be met. These same qualification requirements apply to new processes, new materials, new designs and major changes in any of these areas. The guidelines for qualification of process or product changes are detailed in Appendix 1 of AEC-Q100. At LTC we adhere to those guidelines and in many cases impose additional testing per our own requirements. Examples of some of the qualification tests which are used by LTC are shown in Table 3 at the end of the Reliability Assurance Program.

As part of new product qualification, LTC performs ESD sensitivity classification testing of devices to JESD22-A114 and JESD22-A115. This ESD sensitivity testing uses both the human body model and the machine model. During this rigorous testing, every pin combination on at least three devices is subjected to three positive pulses followed by three negative pulses at the specified voltage increment with a one-second cool down period between pulses. Following this ESD testing, the device is tested for opens or shorts on a curve tracer and then must pass the full data sheet limits on the automatic test equipment.

Additionally for CMOS circuits, latch-up testing is performed per JESD78 on every pin to determine the device's ability to source or sink current without destructive latch-up. We require new LTC products to handle increasingly high currents without latch-up and subsequently meet all data sheet parameters.

Reliable radiation-hardened devices are produced by LTC using a proprietary process technology designed to meet or exceed 100k RADS total dose. Qualification testing of these devices using a Cobalt 60 source has demonstrated excellent results on a number of products. Data sheets for our RAD-hard product line are available from your local sales representative.

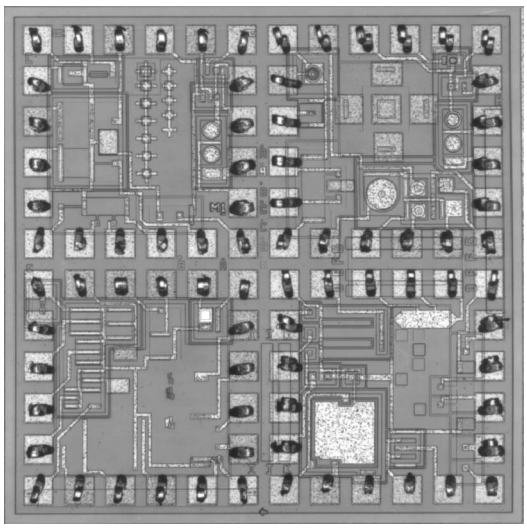
Wafer Level Reliability Assessment

As an additional reliability control, LTC has innovated a strategy for auditing the wafer fab process. Diagnostic structures, in addition to the device structures, are specifically designed as either bipolar or CMOS reliability test patterns and are stepped into all wafers. These structures are tested during fabrication using a parametric analyzer. Then these test vehicles are used to investigate and detect potential yield and reliability hazards after assembly.

The bipolar process version of this structure is optimized to accelerate, under temperature and bias, the two most common failure mechanisms in linear circuits; mobile positive ions and surface charge-induced inversions. This three-terminal structure is scribed from a wafer and assembled in either a hermetic or plastic package. These devices are burned in for a predetermined temperature and time. The same structures becomes sensitive to either failure mechanism depending upon the bias scheme used during burn-in. A limit is defined for the leakage current change during burn-in; a failure indicates a wafer fab problem which will be addressed by the process engineering group.

The CMOS process version allows measurements of thresholds of various sizes and kinds of N-channel and P-channel MOSFETs. Body effects, L effective, sheet resistance, zener breakdown voltage, contact metal resistance and impact ionization current are measurable with this chip which is assembled in a 20-lead DIP.

Bipolar Test Pattern



RAP 12

Electrical testing is performed on the structure before and after burn-in. After evaluating any sample population shifts or failures, process engineering is apprised of the results of this process monitor.

The use of test patterns allows any device to be monitored and also gives faster unambiguous feedback than is normally achieved by performing reliability testing on assembled product. Reliability data is generated in less than one week, giving immediate feedback to the production line.

LTC utilizes this new reliability control technique in addition to the conventional reliability audit on randomly pulled finished product. Operating Life tests are performed and the distributions of key parameters before and after testing are evaluated for stability and control.

Quick Reaction Reliability Monitor

As a complement to the wafer level reliability program, a monitor program focused on assembly-related issues has been fully implemented. This reliability monitor program, known as the quick Reaction Reliability (QR^2) monitor, has been specifically tailored to provide quick feedback of reliability assessment of the assembly operation. The tests in the QR^2 program are designed to identify reliability weaknesses associated with wire bonding, die attach, package encapsulation and contamination-related failures. The actual tests performed in the QR^2 Monitor Program are shown in Table 4.

In order to ensure that representative reliability assessment is made, the QR^2 sampling matrix requires QR^2 testing of every date code from each assembly location on each package type and lead count from that assembly location. This provides a weekly snapshot of the reliability of all packages from all assembly locations. The basic strategy is to evaluate as many production lots as possible to provide maximum confidence to our customers.

Should a failure occur during QR^2 testing, the entire production lot is impounded before shipment. Failures are analyzed to determine validity and the root cause of any valid failure. Quite often additional samples are pulled and tested for an extended period of time. Lots with substandard reliability performance are scrapped. The data generated from this program is used to establish a program for continuous quality improvement with our assembly facilities.

Long Term Reliability Monitor

LTC also conducts a traditional long term reliability monitor program on devices pulled from Boxstock. This long term reliability monitor is used for extended life and end-of-life approximations such as Failure in Time (FIT) calculations. The long term reliability monitor also serves as a check against our short-term reliability estimates.

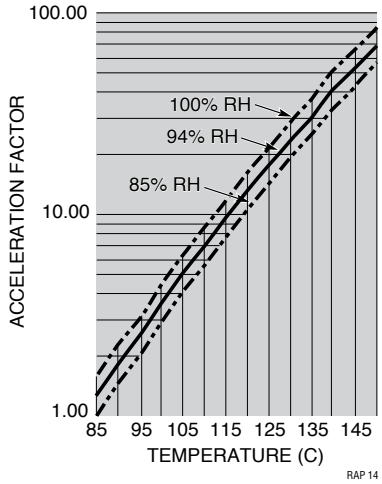
The long term reliability tests are designed to evaluate design, wafer fab and assembly-related weaknesses. Industry standard reliability tests and the relatively new Highly Accelerated Stress Test (HAST) have been incorporated into this program. The long term reliability monitor tests are shown in Table 5.

The most severe tests for plastic package devices are the temperature and humidity tests, particularly HAST testing. We have included HAST testing in the long-term reliability monitor program due to the highly accelerated nature of this test. This test accelerates the penetration of moisture through the external protective encapsulant or along the interface between the encapsulant and the metallic lead frame. Additionally, the HAST test is conducted with the device under bias. The HAST test places the plastic devices in a humid environment of 85% relative humidity under 33.8 psi of pressure at 130°C. Under these conditions, 96 hours of HAST testing at 130°C is roughly equivalent to 1,000 hours of 85°C/85% RH testing. The employment of HAST testing has dramatically reduced the length of time required for qualification.

Qual Samples Being Loaded into the HAST System

RAP 13

Acceleration Factor Using HAST Compared to 85/85



Automotive Reliability

LTC products meet the need for extra ruggedness demanded by automotive customers in the USA, Europe and Asia. These markets have their own unique set of requirements governed by the Automotive Electronics Council specifications such as AEC-Q100. The Production Part Approval Process (PPAP) activity at LTC defines and demonstrates the extra reliability advantage of our products, which are designed to meet the rigors of automotive applications.

Group C and D Testing

Since LTC is a certified producer of MIL-PRF-38535 Appendix A and 883 product, we perform Group C and D testing regularly on our devices. This data is also incorporated into the reliability datapack (consult LTC). The Group C and D test lists are shown in Tables 6 and 7.

Failure Analysis and Corrective Action

LTC is extremely concerned with all failures whether they occur in-house or at a customer location. We have focused significant resources in the area of failure verification and analysis.

LTC offers failure analysis services to its customers, free of charge. In an emergency situation a preliminary failure analysis report can be issued within 24 hours. Our failure analysis database revealed that the vast majority of all devices returned for failure analysis are invalid due to improper application, gross misuse, or they are fully functional and meet all data sheet parameters. LTC also offers outstanding applications assistance to help the customer achieve the full value of our products.

Scanning Electron Microscope with X-RAY Dispersive Analysis

RAP 15

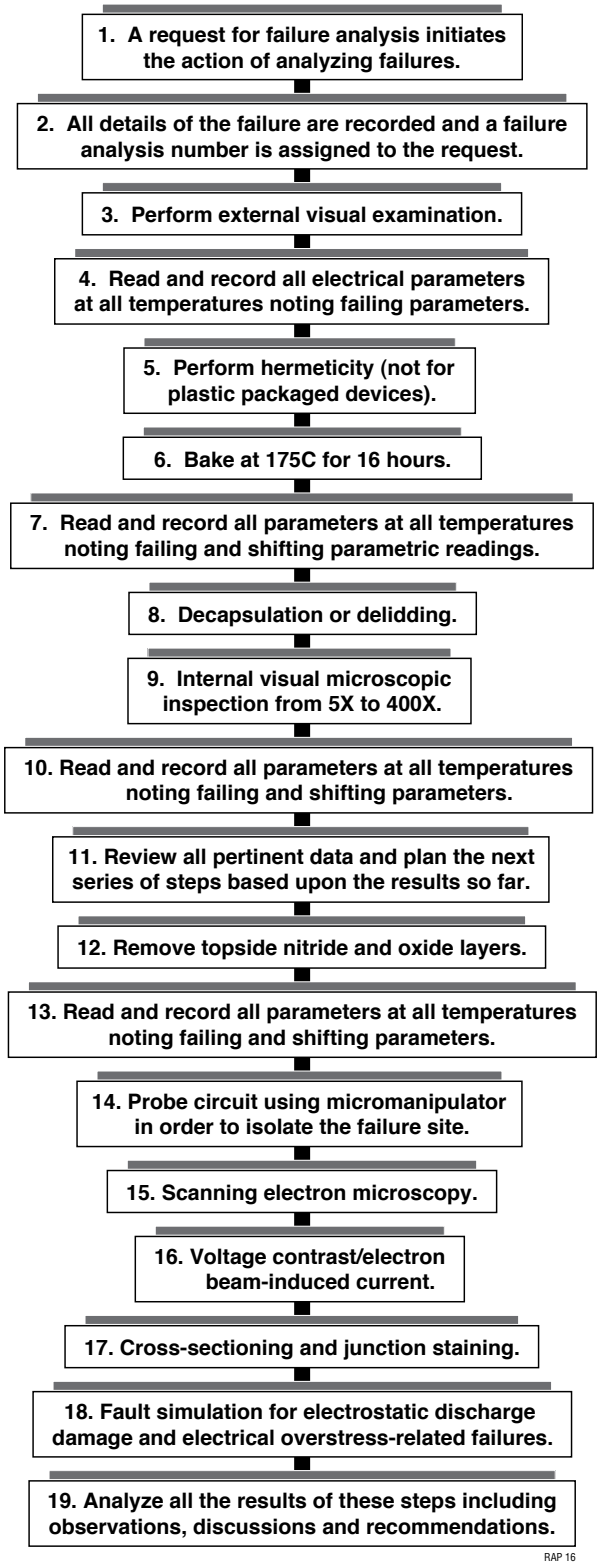
We are equally concerned with failures that are identified during reliability and qualification testing. As with field failures, the in-house failures are analyzed in detail to pinpoint the exact failure mechanism and to identify the root cause. In many cases where ESD or EOS is the suspected cause of the failure, fault simulation is carried out by over-stressing good devices to recreate the fault condition.

LTC has invested in failure analysis resources in the form of experienced, seasoned engineers, and equipment such as a full metallurgical lab, IC deprocessing equipment and a scanning electron microscope with voltage contrasts, Electron Beam-Induced Current (EBIC), Energy Dispersive X-ray Analysis (EDAX), Scanning Acoustic Microscope (CSAM), Fourrier Transform Infrared Microscope (FT-IR), high and low power 3D microscopes, and a computerized database.

All failure analysis reports are documented in detail and distributed appropriately. All valid failure analyses require prompt and effective corrective action which is driven to completion by the quality and reliability organization.

Corrective actions are implemented in accordance with LTC's internal document "Corrective Action Procedure" which details the method and responsibilities for timely corrective action. This procedure is summarized in a separate brochure which is available to our customers upon request.

Typical Failure Analysis Flow



RAP 16

Failure Rate Calculations

Failure rates at LTC are calculated using MIL-STD-690 which is based upon the exponential distribution model for predicting microelectronic device reliability. Examples of FIT and Mean Time Between Failure (MTBF) are shown in the sample calculation below.

Sample Calculation:

Step 1. Calculate Failure Rate at Test Condition (150°C).

Assume 77 units of Op-Life for 1000 hours with Ø failures:

Device Hours at Test Condition = 77 Units × 1000 Hours equals 77,000 Device Hours at 150°C

$$\text{Fail Rate} = \frac{\text{Value from Table A-1 (MIL-STD-690B)}}{\text{Device Hours}}$$

$$= \frac{91{,}641}{77{,}000} = 1.19\%\ 1\text{k Hours} (11{,}900\ \text{FITs})$$

The Arrhenius model is used to extrapolate a failure rate from an accelerated test condition to a use temperature condition.

Step 2. Calculate Acceleration Factor and Extrapolate Equivalent Failure Rate to 55°C.

A_f = Acceleration Factor

$$A_f = e^{\frac{E_a}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

$$A_f = e^{\frac{E_a}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

$$A_f = e^{\left(\frac{1.0}{0.0000863}\right)\left(\frac{1}{328} - \frac{1}{423}\right)}$$

$$A_f = 2791$$

where:

E_a = Activation Energy (Assume 1.0 eV)

K = Boltzmann's Constant = 8.63 X 10^{-5} eV/°Kelvin

T_2 = Test Condition Temperature in °Kelvin

T_1 = Use Condition Temperature in °Kelvin

e = 2.71828 (Natural Antilog)

Now the equivalent failure rate is calculated:

$$\text{Failure Rate } (55°C) = \frac{\text{Failure Rate at Test Condition}}{\text{Acceleration Factor}}$$

$$= \frac{11{,}900 \text{ FITs}}{2791}$$

$$= 4.2637 \text{ FITs}$$

Finally MTBF is calculated:

$$\text{MTBF} = \frac{100{,}000}{0.000426} = \frac{234{,}700{,}000 \text{ Hours}}{\text{or } 26{,}778 \text{ Years}}$$

Reliability Datapack

On a quarterly basis, the reliability department compiles and publishes a report which summarizes all the reliability testing results. This report is intended to provide our customers with a means of determining system reliability. The data is presented at 150°C and at 125°C for those customers who wish to perform their own failure rate calculations. Access this report at www.linear.com. Click on the site map and then Quality Assurance.

In addition, up to the minute reliability summary data reports on particular devices can be generated from the computerized reliability database on the website as well by entering the part number in the search box, selecting the data sheet link and downloading the reliability data pdf. ESD simulation testing reports and current density calculations of individual device types are also available upon request.

Should you desire additional information, please contact your local LTC representative.

Table 1. "R" Flow for Plastic Dual-In-Line Packages

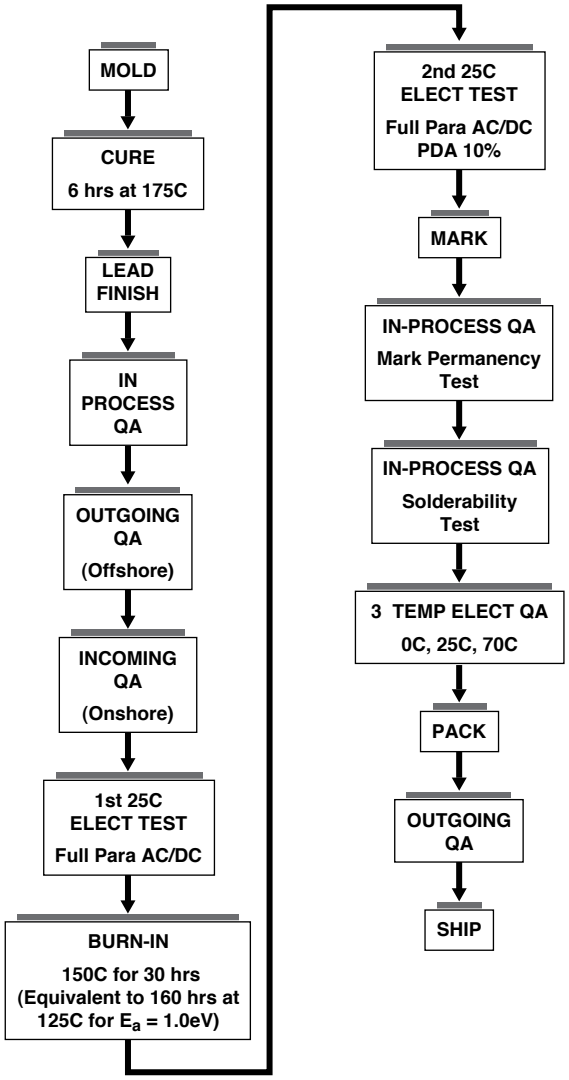
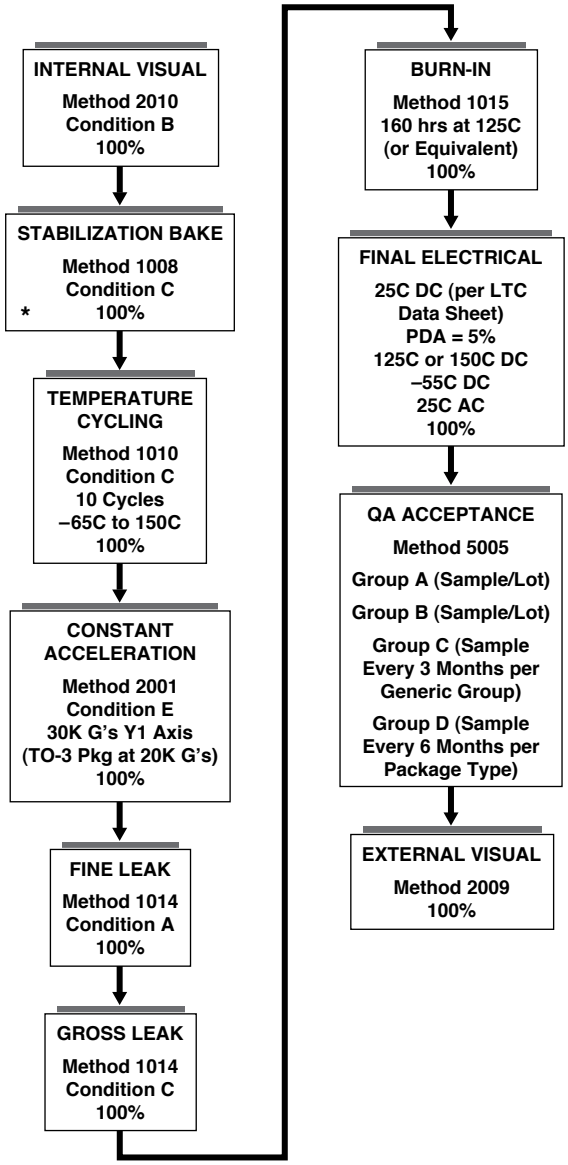


Table 2. Screening Flow per MIL-STD-883, Method 5004



* Product dependent, LTC imposed

Table 3. Reliability Qualification Test Guidelines for Plastic Packages

TEST	METHOD	CONDITIONS	FULL RELEASE DURATION	SAMPLE SIZE	FULL RELEASE S/S SERIES & ACC NO.
High Temperature Bias Operating Life (Op-Life)	JESD22 Method A108	Continuous Operation at Max Rated Supply Voltage. T_A = 125°C to 150°C	1000 Hours to 2000 Hours	77	3%, Acc = 0
Temperature Cycle with JEDEC Preconditioning (JEDEC/TC) (Notes 1, 2)	JESD22 Method A113 Method A104 Condition C	T_A = –65°C to 150°C, >10 Minutes Dwell Time	1000 Cycles to 2000 Cycles	77	3%, Acc = 0
Thermal Shock with JEDEC Preconditioning (JEDEC/TC) (Notes 1, 2)	JESD22 Method A113 Method A106 Condition D	See JEDEC Preconditioning Below. Liquid-to-Liquid, –65°C to 150°C, >5 Minutes Dwell Time	1000 Cycles	77	3%, Acc = 0
Autoclave with JEDEC Preconditioning (JEDEC/PCT) (Notes 1, 2)	JESD22 Method A113 Method A102	See JEDEC Preconditioning Below. T_A = 121°C, 100% RH, 2 Atmospheres	336 Hours	77	3%, Acc = 0
Highly Accelerated Stress Test (HAST) with Preconditioning (JEDEC/HAST) (Notes 1, 2)	JESD22 Method A113 Method A110	See JEDEC Preconditioning Below. T_A = 130°C, 85% RH, 2.3 Atmospheres	96 Hours to 192 Hours	77	3%, Acc = 0
High Temp Storage	JESD22 Method A103	150°C or 175°C	1000 Hours to 2000 Hours	45	5%, Acc = 0
Power Cycling	MIL-STD-883 Method 1006	Power Cycled On/Off, Case Temperature 60°C to 120°C	50,000 Cycles	45	5%, Acc = 0
Scanning Acoustic Microscopy (SAM)	J-STD-035	C-Mode. Before and After Preconditioning (Note 2)	N/A	77	3%, Acc = 0
X-Ray Inspection Radiography (XRAY)	MIL-STD-883 Method 2012	Top View. Side View as Needed	N/A	22	10%, Acc = 0
Other Test and Inspection as Applicable					

Note 1: These tests are conducted with an Infra Red (IR) reflow preconditioning to simulate board soldering conditions.

Note 2: JEDEC Preconditioning is performed per J-STD-020 on surface mount packages only and is comprised of the following:

5 Cylces Temp Cycle –65°C to 150°C (Optional)
24 Hours Bake 125°C
Moisture Preconditioning 168 Hours 85°C/85% RH (MSL1)
CSAM (C-Mode Scanning Acoustic Microscopy)
3 Times Reflow 260°C (245°C for LGA, BGA)
CSAM (C-Mode Scanning Acoustic Microscopy)
Electrical Test

Table 4. Quick Reaction Reliability (QR2) Monitor Program

TEST	METHOD	CONDITIONS	FULL RELEASE DURATION	SAMPLE SIZE	FULL RELEASE S/S SERIES & ACC NO.	FREQUENCY
Package Separation Visual Inspection	N/A	30X Magnification	N/A	45	5%, Acc = 0	Daily
X-Ray Inspection Radiography (XRAY)	MIL-STD-883 Method 2012	Top View Only	N/A	45	5%, Acc = 0	Daily
Solder Shock Test (SDRSHK)	N/A	3 Hrs Autoclave Preconditioning, 1 Time Solder Immersion 245°C	10 Seconds	25	10%, Acc = 0	Weekly
JEDEC Surface Mount Precondition	J-STD-020	85°C/85% RH, IR at 260°C (245°C for LGA, BGA), CSAM	168 Hours, 3 Times IR	45	5%, Acc = 0	Weekly
Temperature Cycle (JEDEC/TC) (Note 1)	JESD22 Method A104 Condition C	Air-to-Air, –65°C to 150°C, >10 Minutes Dwell Time	100 Cycles	45	5%, Acc = 0	Weekly
Thermal Shock (JEDEC/TS) (Note 1)	JESD22 Method A106 Condition D	Liquid-to-Liquid, –65°C to 150°C, >5 Minutes Dwell Time	100 Cycles	45	5%, Acc = 0	Weekly
Autoclave (Pressure Pot without Bias) (PPT) (Note 1)	JEDEC Spec 22 Method A102	Continuous Storage at T_A = 121°C, 100% RH, 2 Atmospheres	24 Hours	45	5%, Acc = 0	Weekly
High Temp Bake (BAKE)	N/A	175°C	500 Hours	45	5%, Acc = 0	Weekly
Operating Life Test (Op-Life)	JESD22 Method A102	Continuous Operation at Max Rated Supply Voltage, T_A = 125°C to 150°C	168 Hours or Equivalent	45	5%, Acc = 0	Monthly
Highly Accelerated Stress Test (JEDEC/HAST) (Note 1)	JESD22 Method A110	Continuous Operation at Max Rated Supply Voltage, Min Supply Current T_A = 130°C, 85% RH, 2.3 Atmospheres	48 Hours	45	5%, Acc = 0	Monthly
DPA Construction Analysis	LTC Spec	LTC Spec	LTC Spec	5	LTC Spec	Monthly
SEM Inspection of Wire Bonds	LTC Spec	LTC Spec	LTC Spec	LTC Spec	LTC Spec	Daily in Assembly
Scanning Acoustic Microscopy (CSAM)	J-STD-035	C-Mode. Before and After Preconditioning (Note 1)	LTC Spec	LTC Spec	LTC Spec	Daily in Assembly
Bond Crater Test (BCT)	LTC Spec	LTC Spec	LTC Spec	LTC Spec	LTC Spec	Daily in Assembly

Note 1: JEDEC Preconditioning is performed per J-STD-020 on surface mount packages only and is comprised of the following:

5 Cylces Temp Cycle –65°C to 150°C (Optional)
24 Hours Bake 125°C
Moisture Preconditioning 168 Hours 85°C/85% RH (MSL1)
CSAM (C-Mode Scanning Acoustic Microscopy)
3 Times Reflow 260°C (24°C for LGA, BGA)
CSAM (C-Mode Scanning Acoustic Microscopy)
Electrical Test

Table 5. Long-Term Reliability Monitor Program

TEST	METHOD	CONDITIONS	FULL RELEASE DURATION	SAMPLE SIZE	FULL RELEASE S/S SERIES & ACC NO.
Operating Life Test (Op-Life)	JESD22 Method A108	Continuous Operation at Max Rated Supply Voltage, T_A = 125°C to 150°C	1000 Hours to 2000 Hours	77	3%, Acc = 0
Highly Accelerated Stress Test (JEDEC/HAST) (Note 1)	JESD22 Method A110	Continuous Operation at Max Rated Supply Voltage, Min Supply Current T_A = 130°C, 85% RH, 2.3 Atmospheres	96 Hours to 192 Hours	45	5%, Acc = 0
Temperature Cycle (JEDEC/TC) (Note 1)	JESD22 Method A104 Condition C	Air-to-Air, -65°C to 150°C, >10 Minutes Dwell Time	1000 Cycles to 2000 Cycles	77	3%, Acc = 0
Thermal Shock (JEDEC/TS) (Note 1)	JESD22 Method A106 Condition D	Liquid-to-Liquid, –65°C to 150°C, >5 Minutes Dwell Time	1000 Cycles	77	3%, Acc = 0
Autoclave (Pressure Pot without Bias) (JEDEC/PPT)	JESD22 Method A102	Continuous Storage at T_A = 121°C, 100% RH, 2 Atmospheres	336 Hours	77	3%, Acc = 0

Note 1: JEDEC Preconditioning is performed per J-STD-020 on surface mount packages only and is comprised of the following:

5 Cylces Temp Cycle –65°C to 150°C (Optional)
24 Hours Bake 125°C
Moisture Preconditioning 168 Hours 85°C/85% RH (MSL1)
CSAM (C-Mode Scanning Acoustic Microscopy)
3 Times Reflow 260°C (245°C for LGA, BGA)
CSAM (C-Mode Scanning Acoustic Microscopy)
Electrical Test

Table 6. Group C per MIL-STD-883C Method 5005

TEST	METHOD	CONDITIONS	TEST DURATION	SAMPLE SIZE	SAMPLE SIZE SERIES ACC NO.
Group C-1 Operating Life Test (Op-Life)	MIL-STD-883 Method 1005	Continuous Operation at Max Rated Supply Voltage T_A = 125°C or T_A = 150°C	 1000 Hours 184 Hours	45	5%, Acc = 0

Table 7. Group D per MIL-STD-883 Method 5005

TEST	METHOD	CONDITIONS	TEST DURATION	SAMPLE SIZE	SAMPLE SIZE SERIES ACC NO.
Group D-1 Physical Dimensions	MIL-STD-883 Method 2016	N/A	N/A	15	15%, Acc = 0
Group D-2 Lead Integrity	MIL-STD-883 Method 2004	Condition B2 (Lead Fatigue)	N/A	45 (Leads)	5%, Acc = 0
Group D-3 Thermal Shock Temperature Cycle Moisture Resistance Hermeticity Visual Exam End Point Electricals	MIL-STD-883 Method 1011 Method 1010 Method 1004 Method 1014 Method 1004/10	 Condition B as a Minimum Condition C	 15 Cycles 100 Cycles	15	15%, Acc = 0
Group D-4 Mechanical Shock Vib. Variable Frequency Constant Acceleration Hermeticity Visual Exam End Point Electricals	MIL-STD-883 Method 2002 Method 2007 Method 2001 Method 1014 Method 1010/11	 Condition B Condition A Condition E (Y1 Only)	N/A	15	15%, Acc = 0
Group D-5 Salt Atmosphere Hermeticity Visual Exam	MIL-STD-883 Method 1009 Method 1014 Method 1009	 Condition A	 24 Hours	15	15%, Acc = 0
Group D-6 Internal Water Vapor	MIL-STD-883 Method 1018	 <5000ppm	N/A	3	0
Group D-7 Adhesion of Lead Finish	MIL-STD-883 Method 2025	N/A	N/A	15	15%, Acc = 0
Group D-8 Lid Torque	MIL-STD-883 Method 2024	 (Glass Frit Seal Only)	 N/A	5	N/A, Acc = 0

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LT 0216 • PRINTED IN USA