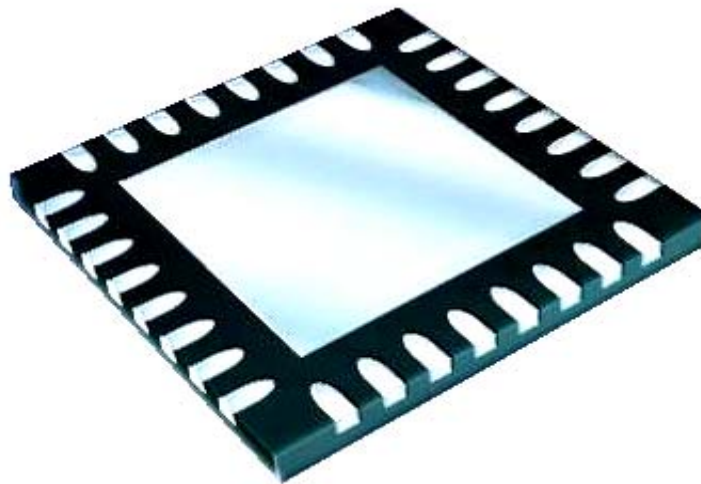


# APPLICATION NOTE

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## Comprehensive User's Guide



# MLP

## Micro Leadframe Package

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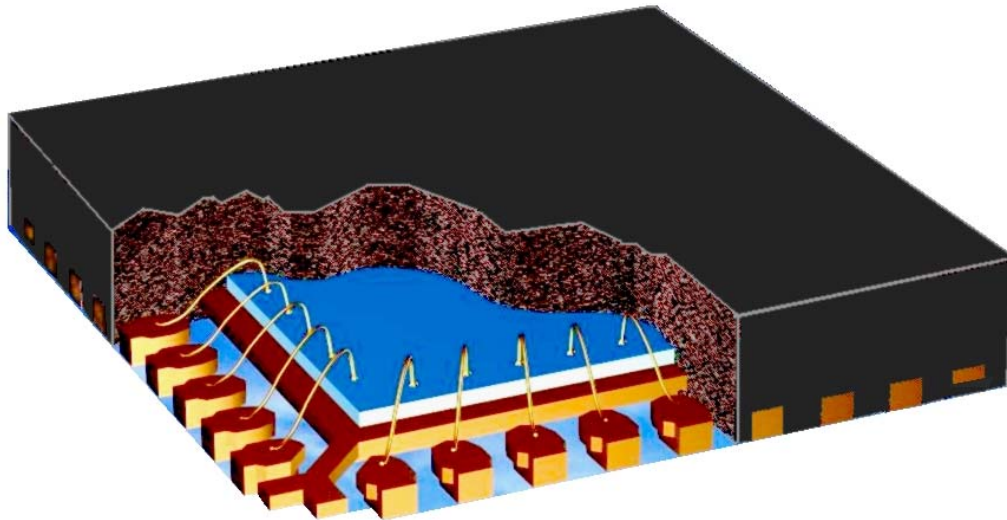
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## 1.0 The Carsem Micro Leadframe package (MLP)

### 1.1 Introduction

During recent years Carsem has conducted research on next-generation Chip-Size Packaging (CSP). The MLP is a near CSP plastic encapsulated package using conventional copper lead frame technology. This construction benefits from being a cost effective advanced packaging solution which helps to maximise board space with improved electrical and thermal performance over traditional leaded packages.



**Isometric Cutaway View of an MLP Component  
Figure 1-1**

The MLP is available in a number of formats. The smallest being the MLP Micro (MLPM) with body sizes ranging from just 2x1mm to 3x3mm. (Body thickness is 0.90mm) The MLPM is individually molded and mechanically singulated from a matrix leadframe. MLP Micro complies to Jedec Outline MO-229.

The MLP Quad (MLPQ) and Dual (MLPD) are molded in one solid array. Individual units are singulated using a saw. Body sizes range from 3x3mm and above. (Body thickness is available in 0.90mm or 0.75mm.). MLPQ complies to Jedec Outline MO-220.

All MLP's are leadless packages where electrical connections are made thru lands on the bottom surface of the component. These lands are soldered directly to the pc board. The standard MLP has an exposed die attach pad which enhances the thermal and electrical characteristics enabling high power and high frequency applications. Power handling capabilities of MLP vs comparable

gullwing packages are shown in Table 1-2. (MLP can handle >2x the power of other SMT packages.)

**Table 1-2 Power Handling Capabilities of MLP vs Comparable Gull Wing Packages**

MLP		GULL WING PKGS	
pkg size	power rating	pkg size	power rating
3X3-10L	1.7	MSOP-10L	0.6
4X4-20L	1.9	TSSOP-20L	0.8
5X5-32L	2.0	TQFP-32L	0.9
7X7-48L	2.6	TQFP-48L	1.2

NOTE: Maximum Power Ratings are calculated from  $\Theta_{ja}$  values listed in Appendix A.

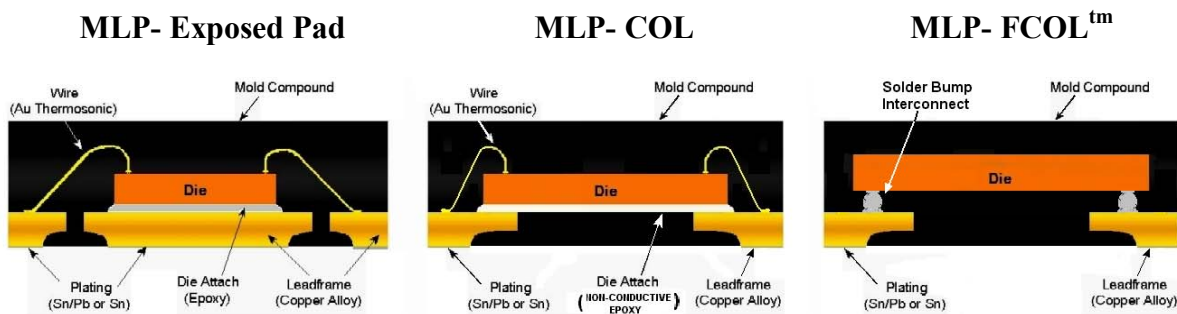
PCB used for simulating power rating of MLP complies to JESD 51-5.

PCB used for simulating power rating of Gullwing packages complies to JESD 51-7.

Operating Conditions-  $T_j = 150^\circ\text{C}$ ,  $T_a = 80^\circ\text{C}$

In addition to Exposed-Pad MLP, Carsem offers two other MLP configurations: COL & FCOL. Chip On Lead (COL) technology eliminates the die attach pad and places the die on extended lead fingers using electrically insulating but thermally conductive epoxy. This enables a larger die to be assembled in the same package using conventional wire bonding.

For even greater die to package size ratio, Flip Chip On Leadframe (FCOL™) can increase the silicon size to a true Chip Scale Package (CSP). Figure 1-3 shows crosssections of all three MLP configurations.



**MLP Typical Crosssections  
Figure 1-3**

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## 2.0 Manufacturing Considerations

### 2.1 SMT Process

Many factors contribute to a high yielding PCB assembly process. A few of the key focus areas and their contributing factors are highlighted in Table 2-1.

**Table 2-1. General Guidelines for Assembly Quality**

Solder Paste Quality	Uniform viscosity and texture. Free from foreign material. Solder paste should be used before the expiration date. Shipment and storage temperatures are maintained at the proper temperature. Paste is protected from drying out on the solder stencil.
PCB Quality	Clean, flat, plated or coated solder land pad area. Attachment surface must be clean and free of solder mask residue.
Placement Accuracy	Tight tolerances are not usually required. CSP packages can self-center itself as long as a major portion (more than 50 percent) of the lead finger is in contact with the solder paste covered land area on the board. Alignment marks (fiducials) on the PCB are helpful for verifying correct placement of parts.
Solder Reflow Profile	The solder reflow profile will be dependent on PCB design, PCB thickness, type of components, component density, and the recommended profile of the solder paste being used. A reflow profile will need to be developed for each PCB type using various CSP packages. Refer to the reflow profile in the solder reflow section (5.2).

## 3.0 PCB DESIGN GUIDELINES

### 3.1 PCB Design Guidelines

One of the key efforts in implementing the MLP package on a pc board is the design of the land pattern. The MLP has rectangular metallized terminals exposed on the bottom surface of the package body. Electrical and mechanical connection between the component and the pc board is made by screen printing solder paste on the pc board and reflowing the paste after placement. To guarantee reliable solder joints it is essential to design the land pattern to the MLP terminal pattern. Figure 3-1 illustrates typical MLP terminal and body dimensions.

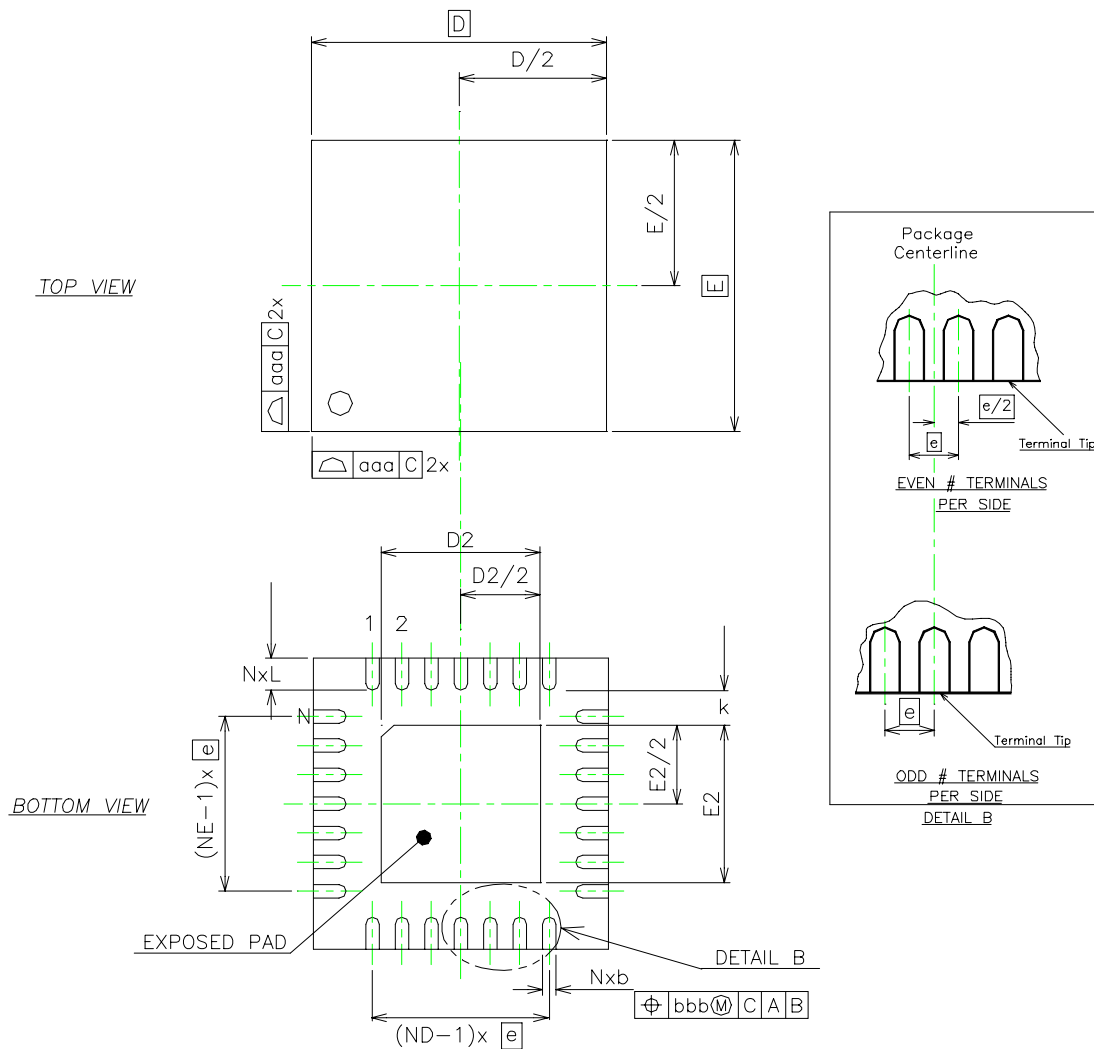
### 3.2 Land Pad Styles

There are two basic designs for PCB land pads for the MLP: Copper Defined style (also known as Non Solder Mask Defined (NSMD)) and the Solder Mask Defined style (SMD). The industry has had some debate of the merits of both styles of land pads, and although we recommend the Copper Defined style land pad (NSMD), both styles are acceptable for use with the MLP package.

NSMD pads are recommended over SMD pads due to the tighter tolerance on copper etching than solder masking. NSMD by definition also provides a larger copper pad area and allows the solder to anchor to the edges of the copper pads thus providing improved solder joint reliability.

### 3.3 Land Pad Design

IPC-SM-782 is an industry standard specification for determining PCB land patterns. Since the MLP is a new package style, it is recommended that this application note should be used in conjunction with evolving QFN guidelines in IPC-SM-782 in designing optimum PCB land patterns.



**Typical MLP Body and Terminal Dimensions**  
**Figure 3-1**

Figure 3.1 identifies the various MLP dimensions required to design a matching PCB land pattern. Since most packages are square with  $D = E$  and the leads are along the E direction for dual packages, the side view dimensions ( $D$ ,  $k$ ,  $D2$  &  $L$ ) are used to determine the land length on the motherboard PCB/substrate. The PCB land pattern dimensions to be established are shown in Figure 3-2.

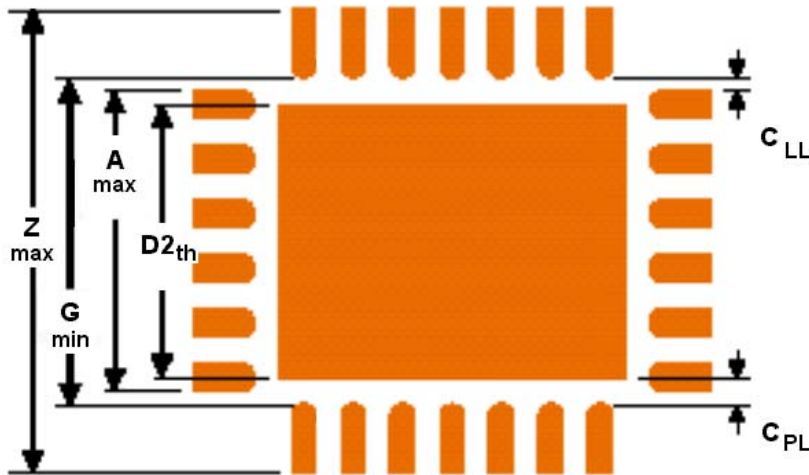
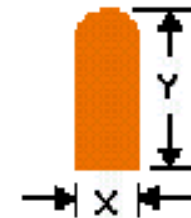


Figure 3-2

### PCB Land Pattern and Dimension Definitions



Terminal Detail

Symbol	Description
Z <sub>max</sub>	Terminal Landing Pattern - O.D.
G <sub>min</sub>	Terminal Landing Pattern - I.D.
X	Terminal Land Width
Y	Terminal Land Length
C <sub>LL</sub> *	Minimum distance between two perpendicular lands in any corner
C <sub>PL</sub> *	Minimum distance between Central paddle to inside edge of terminal land
Note:	Clearance dimensions CLL and CPL are defined to prevent solder bridging

### 3.3 Design of PCB Land Pattern for Package Terminals

As a general rule, the PCB lead finger pad (Y) should be designed 0.2-0.5mm longer than the package terminal length for good filleting. The pad length should be extended 0.05mm towards the center line of the package. The pad width (X) should be a minimum 0.05mm wider than the package terminal width (0.025mm per side), refer to Figure 3-3. However, the pad width is reduced to the width of the component terminal for lead pitches below 0.65mm. This is done to minimize the risk of solder bridging.

Consequently, Z<sub>min</sub> should accommodate the maximum pkg length or width (D or E), profile tolerances of the pkg body (aaa=0.15mm typ), plus the recommended extensions (Y1) (fig. 3-3) for fillet on both ends of the package (0.2mm x 2). In other words **Z<sub>min</sub> = D bsc + aaa + 2(Y1) = D + 0.15mm + 0.4mm.**

### PC Board Land Pattern Geometry for MLP Terminals

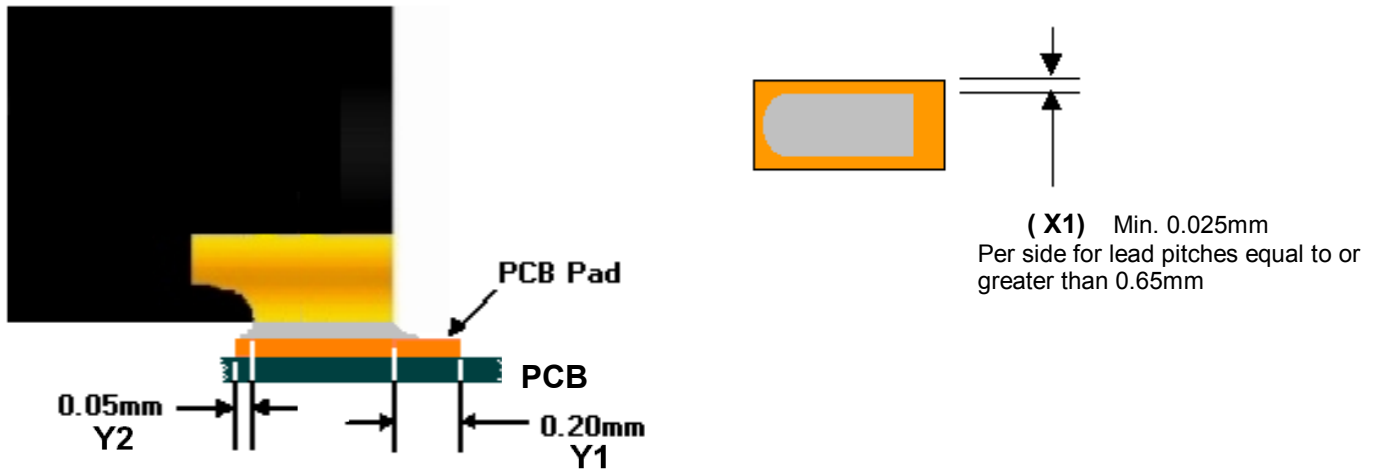


Figure 3-3

#### 3.4 Exposed Pad PCB Design

The construction of the Exposed Pad MLP enables enhanced thermal and electrical characteristics. In order to take full advantage of this feature the exposed pad must be physically connected to the PCB substrate with solder. (Reference figures 3-1,3-2, 3-3)

The thermal pad ( $D_{2th}$ ) should be greater than  $D_2$  of the MLP whenever possible, however adequate clearance ( $C_{pl} \geq 0.15mm$ ) must be met to prevent solder bridging. If this clearance cannot be met, then  $D_{2th}$  should be reduced in area. The formula would be:  $D_{2TH} > D_2$  only if  $D_{2TH} \leq G_{min} - (2 \times C_{pl})$

Figure 3-4 is an example of a PCB Land Pattern for a 3x3-16L with an Exposed pad ( $D_2$ ) of 1.45mm.

$$Z_{min} = D + aaa + 2(0.2)$$

(where pkg body tolerance  $aaa=0.15$ )  
(where 0.2 is outer pad extension)

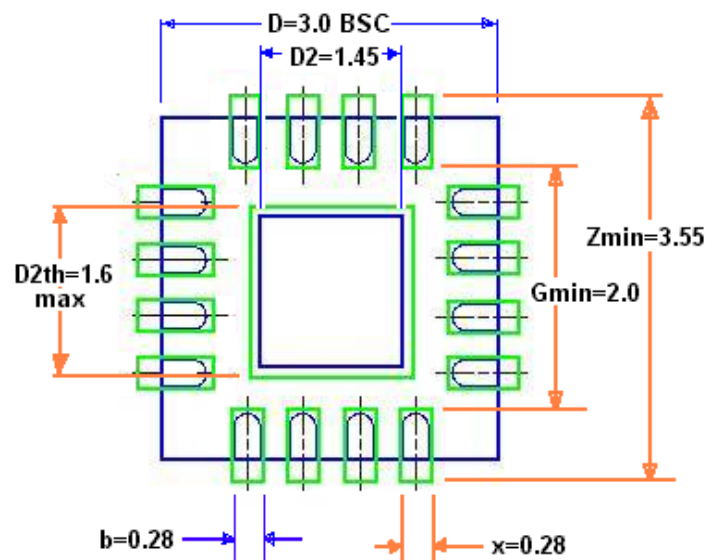
$$G_{min} = D - 2(L_{max}) - 2(0.05)$$

(where 0.05 is inner pad extension)  
( $L_{max}=0.45$  for this example)

$$D_{2th \text{ max}} = G_{min} - 2(C_{pL})$$

(where  $C_{pL}=0.2$ )

In this case, there is adequate clearance for  $D_{2th}$  to be greater than  $D_2$ .

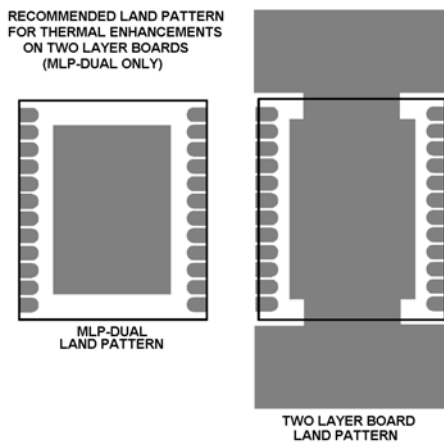


**MLP Dimensions for 3x3-16L- Blue**  
**(Corresponding Land Pattern - Green)**  
Figure 3-4

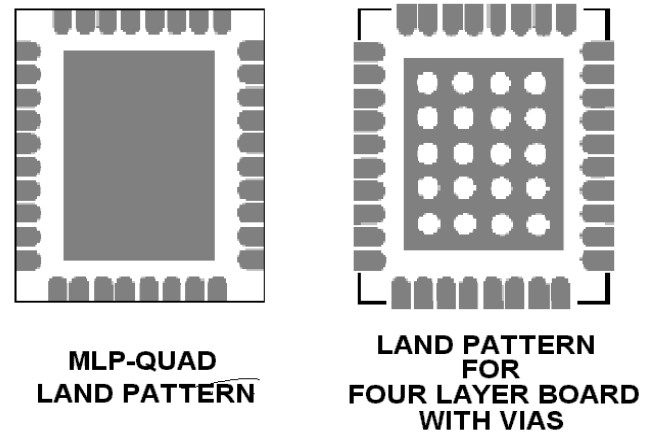


### 3.4.1 Thermal Pad Via Design

Most thermal data ( $\Theta_{ja}$ ) for MLP is based on a 4 layer PCB incorporating vias which act as the thermal path to the layers. (Ref: Jedec Specification JESD 51-5). Two layer boards have no vias, thus any heat sinking must be accomplished in the same plane as the metal traces. This will typically require an increase in the pc board area. Also note that 2 layer heat sinking is only practical for packages with terminals on two sides. There is no routing room when using a pkg configured with leads on all 4 sides. See figures 3-5 & 3-6 below.



**Thermal Routing for Two Layer PCB**  
Figure 3-5

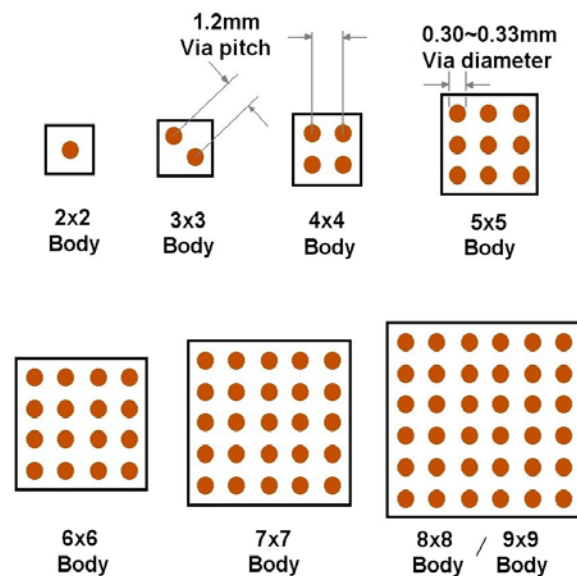


**Thermal Routing Vias for 4 Layer PCB**  
Figure 3-6

Based on thermal performance it is recommended to use 4 layer pcb's with vias to effectively remove heat from the device. (See Table 3-8 for the thermal advantages of 4 layer boards with vias vs 2 layer non-via boards.) Additional thermal performance information is located in Tables 3.9, 3-10 and Appendix 1.

Typical thermal vias have the following dimensions:  
1.2mm pitch, 0.3mm diameter

Vias should be plugged to prevent voids being formed between the exposed pad and PCB thermal pad due to solder escaping by the capillary effect. This can be avoided by tenting the via during the solder mask process. The via solder mask diameter should be 100  $\mu\text{m}$  larger than the via hole diameter. Trials have shown that via tenting from the top is less likely to produce voids between the exposed pad and the pcb land. Figure 3-7 shows typical via layouts for MLP.



**Suggested Thermal Via Layout for MLP - Figure 3-7**

Table 3-8

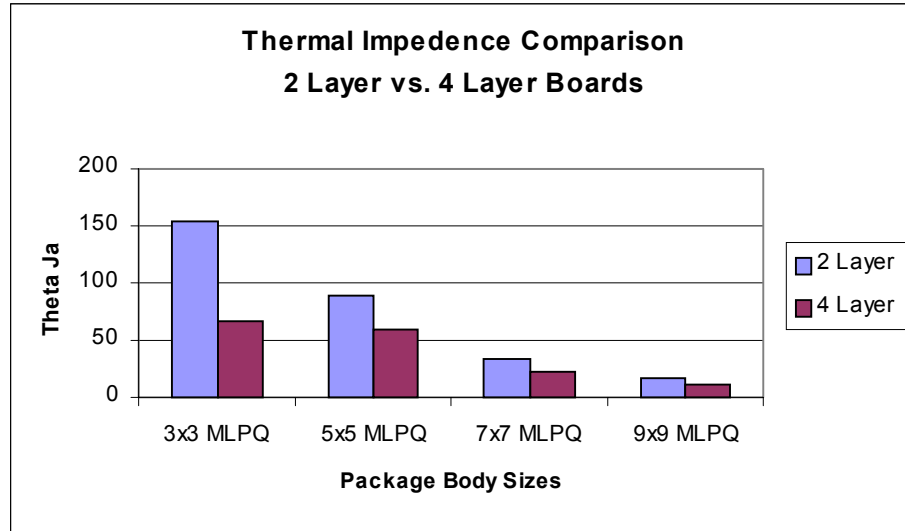


Table 3-9

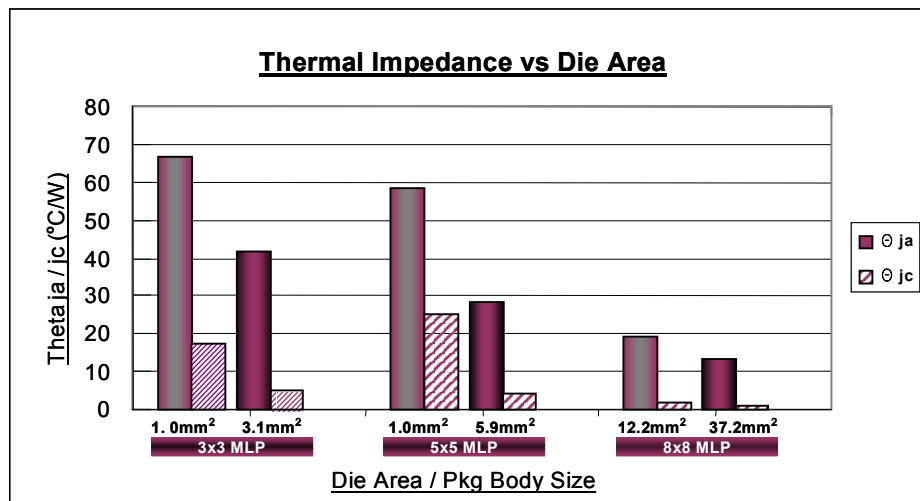
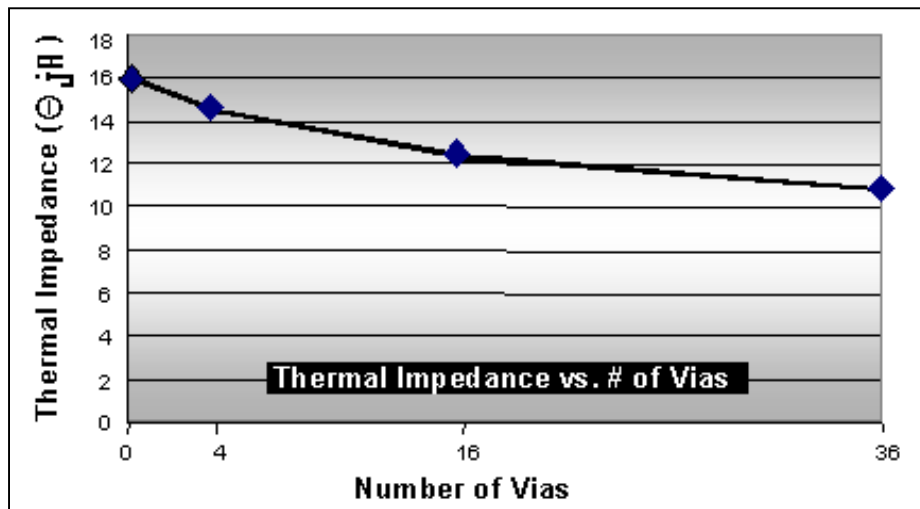


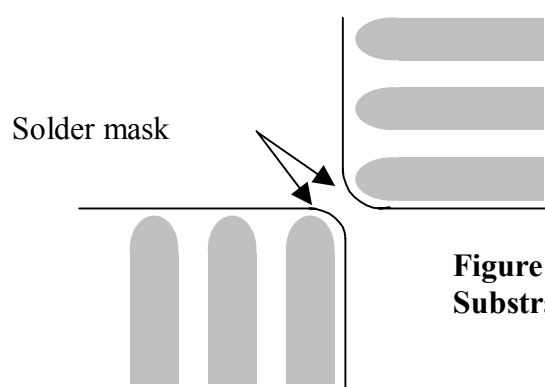
Table 3-10



### 3.5 Solder Mask

As described at the beginning of this section, Non Solder Mask Defined (NSMD) is recommended over Solder Mask Defined style (SMD) to produce good solder joint reliability.

The solder mask can be designed around each individual lead finger for lead pitches 0.65mm and above. Solder mask openings should be between 60 to 75  $\mu\text{m}$  larger than the lead finger pad size. For lead to lead pitch of 0.5mm it is recommended to design the solder mask around all pads on each side. In order to maximise the solder mask between adjacent sides it is necessary to round the inner corner on each row. This will ensure sufficient solder mask in the corner of the PCB footprint design. Refer to Figure 3.5



**Figure 3.5**  
**Substrate/PCB Solder Mask**

### 3.6 Surface Finishes

There are a variety of surface finishes commonly available. The key factor in selecting an acceptable surface finish is to ensure that the land pads have a "uniform" coating. Irregular surface plating, uneven solder paste thickness and crowning of the solder plating can reduce overall surface mount yields. Bare Copper with an Organic Solderability Preservative (OSP) coating, electroless nickel/immersion gold, or electroplated nickel/gold finishes have shown to provide an acceptable land pad surface. One type of surface finish that should be avoided is referred to as a dry-film process. This is because the copper undercut effect caused during the dry film removal prevents optimal sidewall wetting during the reflow process.

Of the coating and plating options available, Ni/Au is the most versatile providing the gold thickness is controlled. Typically, 5 $\mu\text{m}$  Nickel and between 0.05 and 0.1 $\mu\text{m}$  gold to prevent brittle solder joints . The advantage of plating over OSP's: i) shelf life, ii) permanent coverage of copper vias and other features not exposed to a solder process iii) contamination resistance. A controlled assembly process for MLP soldering relies on a flat uniform attachment site. Achieving this will allow for greater control of solder paste print uniformity.

## 4.0 SOLDER PASTE SCREEN PRINTING PROCESS

### 4.1 Solder Paste

The quality of the paste print is an important factor in producing high-yield assemblies. A Type 3 or 4, low residue, no-clean solder paste (Sn63/Pb37) is commonly used in mounting CSPs, however water soluble flux materials are widely used as well. Suggested solder reflow parameters for this solder paste are detailed later in section 5.2 of this document. Special SMD specific solder pastes are being marketed by paste vendors that minimize voiding in the solder joint.

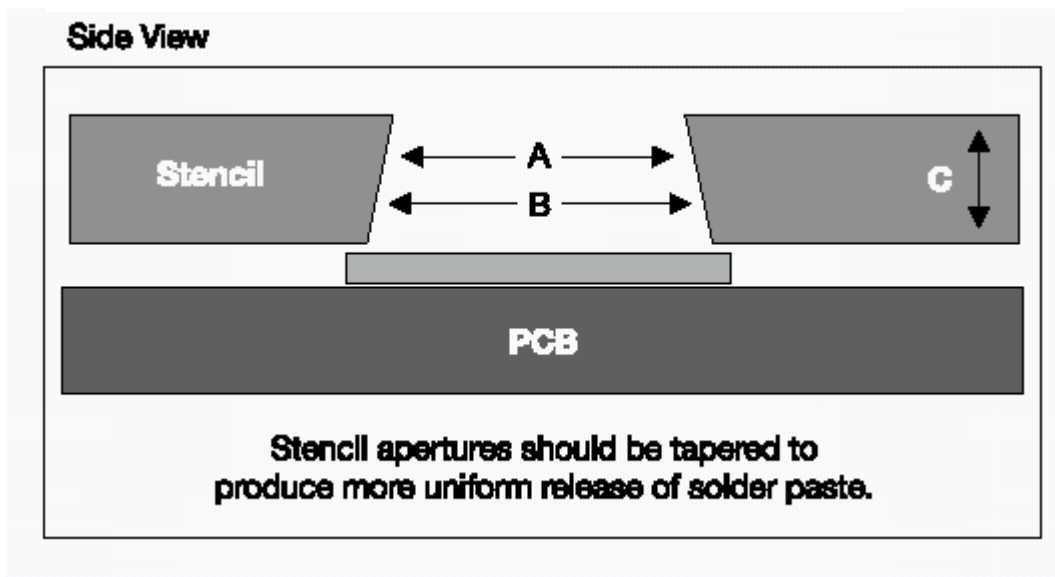
### 4.2 Solder Stencils

The formation of reliable solder joints is a necessity. The contrast between large exposed pad and small lead fingers of the MLP can present a challenge in producing an even solder line thickness. To this end, careful consideration must be applied to the stencil design

The stencil thickness, as well as the etched pattern geometry, determines the precise volume of solder paste deposited onto the device land pattern. Stencil alignment accuracy and consistent solder volume transfer is critical for uniform reflow-solder processing.

Stencils are usually made of brass or stainless steel, with stainless steel being more durable. Apertures should be trapezoidal to ensure uniform release of the solder paste and to re-duce smearing. Hence dimension  $A < B$ . Refer to Figure 4-1

Figure 4-1. Solder Stencil Dimensional Details



The solder joint thickness for MLP lead fingers should be 50 - 75 $\mu$ m.

Thickness of the stencil (C) are usually in the 100 $\mu$ m to 150 $\mu$ m (0.004" to 0.006") range. The actual thickness of a stencil is dependent on other surface mount devices on the PCB.

A squeegee durometer of 95 or harder should be used. The blade angle and speed must be fine-tuned to ensure even paste transfer. An inspection of the stenciled board is recommended before placing parts as proper stencil application is the most important factor with regards to reflow yields further on in the process.

As a guide it is recommended to use a stencil thickness of 125 $\mu$ m (5mils) for MLP components.

### 4.3 Lead finger stencil design

The stencil aperture is typically designed to match the PCB/substrate pad width 1 to 1. For fine pitch components of 0.5mm and below it may be necessary to reduce the stencil aperture length by 20%. This is necessary to aid solder paste printing as a PCB pad of 0.25mm leaves just 0.15mm spacing between pads.

Lead finger stencil dimensions will depend on the specific MLP lead finger dimensions. Given a 0.5mm pitch device with 0.28mm wide pads a stencil thickness of 0.125mm is needed. To get a good print the pad length should be reduced by up to 20% at each end with the width remaining the same.

The area ratio of the stencil is critical in order for the printing to get good paste release. For very small apertures where the area ratio is less than 0.66 the stencil must be nickel formed. This type of stencil has superior release characteristics over stencils that have been produced by laser. Nickel formed stencils with area ratios down to 0.57 are typically used in the PCB industry.

The Aspect Ratio relates to the manufacture of stencils. Stencil manufacturers will require the Aspect Ratios to be greater than 1.5. Reference IPC-7527.

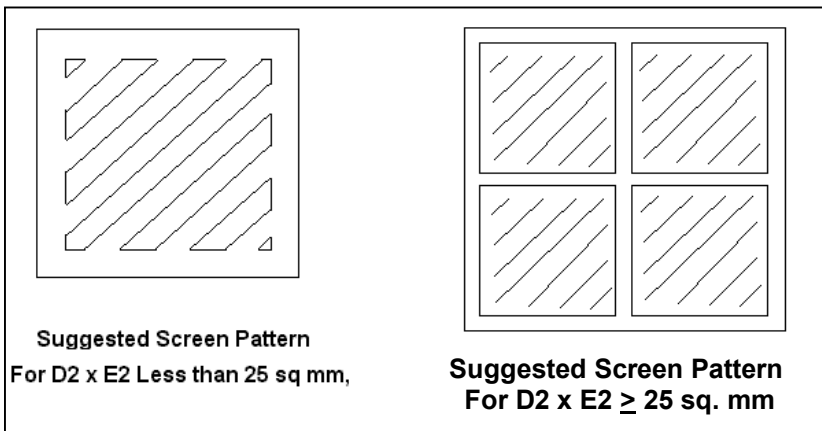
AREA RATIO = Area of Aperture Opening / Aperture Wall Area

ASPECT RATIO = Aperture Width / Stencil Thickness

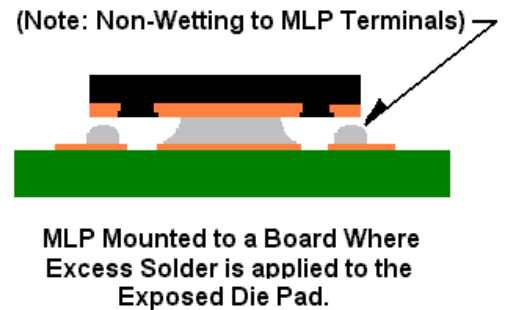
### 4.4 Exposed Pad Stencil Design

The MLP package is thermally and electrically efficient. This is enabled by the exposed die attach pad on the under side of the package which must be soldered down to the PCB or mother board substrate.

It is good practice to minimise the presence of voids within the exposed pad inter-connection. Total elimination is difficult but the design of the exposed pad stencil is key. Figure 4-2 shows some suggested screen print patterns. For exposed die pad sizes less than 25 mm<sup>2</sup>, a single slotted square pattern is recommended. For larger areas, a matrix of squares will minimize voids and normalize the standoff height for the exposed pad and the terminals. (If large exposed pads are screened with excessive solder, the device may "float", thus causing a gap between the MLP terminal and the pcb land metalization. See Figure 4-3.) The proposed stencil designs enables out-gassing of the solder paste during reflow as well as regulating the finished solder thickness.



**Exposed Pad Stencil Design**  
**Figure 4-2**



**Excessive Exposed Pad Solder**  
**Figure 4-3**

## 5.0 PACKAGE TO BOARD ASSEMBLY PROCESS

### 5.1 Placement and Alignment

The pick and place accuracy governs the package placement and rotational (theta) alignment. This is equipment/process dependent. Slightly misaligned parts (less than 50 percent off the pad center) will automatically self-align during reflow (see Figure 5-1).

Grossly misaligned packages (greater than 50 percent off pad center) should be removed prior to reflow as they may develop electrical shorts, as a result of solder bridges, if they are subjected to reflow

There are two popular methods for package alignment using machine vision:

Package silhouette—the vision system locates the package outline

Terminal recognition—Some vision systems can directly locate on the metalization terminal pattern

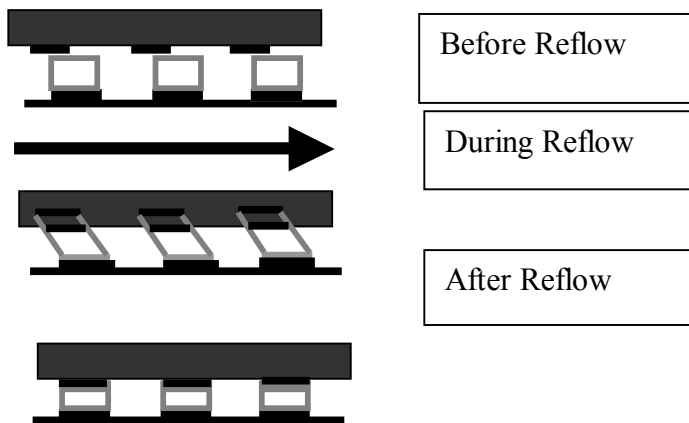
Both methods are acceptable for MLP placement. The terminal recognition type alignment tends to be more accurate, but is also slower since more complex vision processing is required of the pick and place machine. The package silhouette method allows the pick and place system to run faster, but is generally less accurate.

Both methods are acceptable, and have been successfully demonstrated by major pick and place equipment vendors, and contract PCB assembly houses.

## 5.2 Solder Reflow

There are no special requirements necessary when reflowing MLP components. As with all SMT components, it is important that profiles be checked on all new board designs. In addition, if there are multiple packages on the board, the profile should be checked at different locations on the board. Component temperatures may vary because of surrounding components, location of the device on the board, and package densities.

To maximize the self-alignment effect of an MLP (see Figure 5-1), it is recommended that the maximum reflow temperature specified for the solder paste not be exceeded. A good guide is to subject the PCB to a temperature ramp not exceeding 4°C per second.



**Figure 5-1**  
**Package Self-Alignment at Reflow**

The reflow profile guidelines are based on the temperature at the actual solder pad to PCB land pad solder joint location. The actual temperature at the solder joint is often different than the temperature settings in the reflow/ rework system due to the location of the system thermocouple placement used to monitor the temperature. The furnace needs to be profiled using thermocouples at various locations on the PC Board. A thermocouple should be placed on one of the largest and smallest components on the PCB. It is suggested that the peak temperature differential between the smallest and largest package be 10 °C or less for average size pc boards.

For standard Sn/Pb solder, the profile should ramp at a rate of 3 °C /sec to 125 °C for preheat, followed by a ramp to 235°C for actual reflow of the solder, and finally cool down at a rate of no greater than 6 °C /sec. Reference Jeduc/IPC Standard J-STD-20a for reflow recommendations.

Carsem has tested and qualified MLP's for a maximum of three reflow operations. This allows one reflow operation per side of the PCB (assuming the use of a double-sided PCB), and one rework operation if necessary.

Carsem qualification also includes board level reliability data per the IPC-782 standard. Initial temp cycle data at -40 °C/+100 °C has so far proven successful up to 2000 cycles. This data is continuously being updated, and was therefore not included in this applications note. (Contact your account representative for updated Board Level Reliability data.)

### 5.3 PCB Cleaning

If a low residue, no-clean solder paste is used, PCB cleaning is not required, and has little effect on an MLP. With the elimination of materials containing CFC's, most companies have moved to a no-clean or aqueous flux-based system. "No clean" fluxes and solders simply mean that there are no harmful residues left on the board that could cause corrosion or damage to the components if left on the board. This residue has sometimes been shown to be a collection point for outside contamination on the board surface. Because there are so many different types of no-clean solder pastes available, application specific evaluations should be performed to identify if any remaining residue still needs to be removed from the boards in final production.

### 5.4 Inspection

Inspection of an MLP on a PCB is typically accomplished by using transmission type X-ray equipment. In most cases, 100 percent inspection is not performed. Typically, X-ray inspection is used to establish process parameters, and then to monitor the production equipment and process. Transmission X-ray can detect bridging, shorts, opens, and solder voids. There are many different types of X-ray inspection equipment available and functionality varies. X-ray inspection system features range from manual to automated optical inspection (AOI). Different systems also provide single or multiple dimensional inspection capabilities.

Visual inspection systems are also being adopted for MLP, especially in the area of rework. Please refer to Section 6 of this document.

As explained in the section 5.2 of this guide, an MLP will self align to the land pad using surface tension during the solder reflow process. As a result, it is very unlikely that an MLP will be marginally misaligned. If misalignment does occur, it is likely to be by an entire pad. This effect makes it possible to do a gross visual alignment check after the reflow. Visual checks can be aided by the use of PCB fiducial marks as well as being useful for manually placing units during any rework.

### 6.0 Rework

MLP rework procedures are an adaptation (and in some cases a simplification) of Ball Grid Array Package rework procedures. The basic elements of this procedure are as follows:

- 1- Pc board preheat
- 2- Reflow of component solder
- 3- Vacuum removal of component
- 4- Cleaning and prep of pcb lands
- 5- Screening of solder paste
- 6- Placement and reflow of new component
- 7- Inspection of solder joints



## PC Board Preheat

It is recommended to bake the pcb for approx 4 hours at 125°C prior to rework in order to drive off residual moisture that could cause other component failures during the rework reflow process. Once the pcb has finished the baking process, the pcb under rework is then placed in the rework holder and heated again to a temperature of 125 °C. Localized heating of the area under rework is recommended.

## Reflow / Removal of the Component from the PCB

Specialized vacuum collets come in contact with the rework component. These collets incorporate a hot gas shroud that heats up the part to a temperature required for reflowing the solder interconnects. Once the solder reflows, the vacuum collet lifts the unit from the pcb. The collet size and hot gas flow should be optimized to keep the heat flow localized.

## Cleaning and Prep of the PCB Land

The pcb can be cleaned and prepared using conventional tools and processes currently used for gullwing packages. Removal of excess solder using a hot iron, a small scraping tool and solder wick is typical. Place the solder wick under the scraping mechanism to remove the solder from the land area.

## Screen Printing of Solder Paste

Based on some of the tight geometries used on today's pcb's, it is difficult to screen print a pcb that is nearly 100% populated with components. Hence the approach of screen printing the solder paste directly onto the new component has been adopted. It is recommended to use a type 3 or 4 no-clean solder paste. The layout of the stencil should follow the guidelines stated in Section 4.

## Placement and Reflow of Component

The placement of the new MLP component should be done with a split field vision system. See Figure 6-3. The image of the screen printed component and the pcb land pattern are superimposed during the placement operation, thus making the placement easier to align with the terminal footprint.

The reflow of the new component should be done with a localized gas shroud similar to that used during the component removal operation. The profile used for the reflow should have ramp rates and peak temperatures that follow the guidelines specified in Jecdec J-Std-20a. (*Preheat @ 125°C / Reflow @ 235°C*)

Figure 6-1



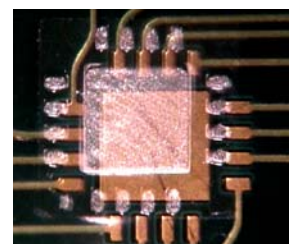
Vacuum Collet Tool  
(courtesy of Metcal)

Figure 6-2



Manual Screen  
Printing

Figure 6-3



Split Field  
Vision System  
(Courtesy of Metcal)

## Inspection of Reworked Solder Joints

Inspection techniques for MLP closely resemble those techniques used for Ball Grid and Land Grid Components. Visual inspection of solder joints from overhead (z-plane) is not possible for these packages. Thus, the use of z-plane X-ray or high precision camera system capable of viewing parallel to the x-y plane is necessary. See Figure 6-5 shows equipment used for x-y visual inspection.

## Rework Equipment for MLP

Rework systems for MLP are based on well established rework systems created for Ball Grid Array packages. The concept is not new, however equipment refinements have been made in order to adapt the equipment to handle MLP.

**An example of a well established rework system is the Metcal APR-5000. (Figure 6-4).** This System contains the essential hardware and automated software features necessary for reworking MLP packages. This system takes up less than 6 sq ft of manufacturing floor space.

Closed-loop, computer-controlled time, temperature and airflow parameters help to guarantee process control and repeatability. The system software manages the reflow profile: pre-heat, soak, ramp, reflow and cooling. In addition, board temperature can be monitored using three integrated flying thermocouples, and real time adjustment can be made to all parameters while the profile is running.

A variety of "off the shelf" vacuum collets and solder screens are available from Metcal. Please reference [www.Metcal.com](http://www.Metcal.com) for open tools and for custom tooling requirements.

Capable of handling boards up to 9" x 10" (229mm x 254mm) with a placement accuracy to 0.001"(0.025mm) and interconnection pitches as low as 0.012" (0.3mm), the APR-5000 Array Package Rework System is optimum for reworking smaller assemblies such as cell phones and laptop computers.



METCAL APR-5000  
Rework System  
Figure 6-4

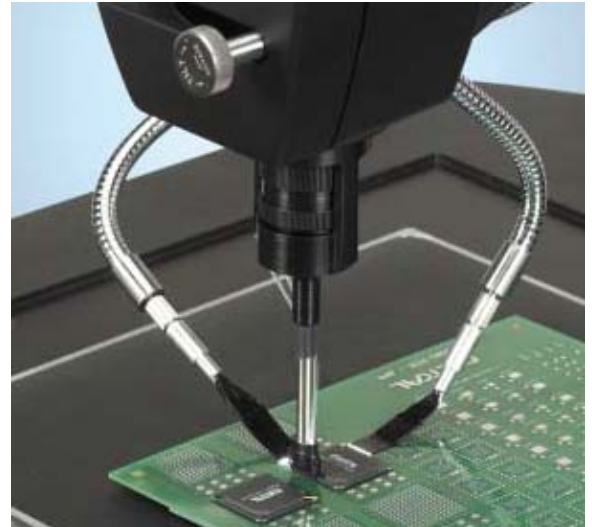
*(Photo of APR-5000 courtesy of METCAL)*

### Optical Inspection Equipment for MLP

The **Metcal VPI-1000 Optical Inspection System** is a good example of inspection equipment sophistication.

Unique to the VPI-1000 Optical Inspection System is the placement of the lens, which is within the mirrored tip. This unique design allows operators to inspect under an array package with a standoff height as low as 0.002” (0.05mm). And the special, durable tip requires just 0.043” (1.1mm) of space between components to achieve optimal inspection. With a simple turn of the lens adjustment ring, the operator can easily check for bridging, cold solder joints, shorts and other process-related failures that X-ray inspection may not see.

Figure 6-5



Example of Specialized  
Vision System for Viewing  
X-Y planes under MLP, BGA,  
and LGA Components.

*(Photo of VPI-1000 courtesy of METCAL)*

### Appendix 1

Appendix Table 1 - Comparative Thermal Impedance Data - MLP vs Gullwing Packages

		<b>MLP</b>				<b>Comparable Gullwing Package</b>					
		Body Size	I/O	**Die Area	Thermal Data $\Theta_{ja}$	Thermal Data $\Theta_{jc}$	Package Type	I/O	**Die Area	Thermal Data $\Theta_{ja}$	Thermal Data $\Theta_{jc}$
		<b>Dual</b>		2x2	6	0.38	99.7	53.2	SC70	5	0.13
	3x3		6	3.03	41.4	5.2	SOT23	6	0.97	96.1	62.2
	5x6		8	2.26	36.4	8.0	SOIC	8*	1.74	45.3	28.4
<b>Quad</b>		3x3	16	1.03	66.8	17.5	QSOP	16	2.30	112.0	39.0
		4x4	24	1.23	47.0	14.4	TSSOP	24	6.45	84.0	16.0
		5x5	32	5.93	28.2	4.0	TQFP	32	2.30	76.0	19.0
		6x6	36	16.4	18.9	1.7	TSSOP	38	6.45	75.0	13.0
		7x7	48	8.4	22.2	2.2	TQFP	48	2.30	57.0	13.0
		8x8	56	36.8	13.1	0.8	MQFP	52	6.45	61.0	20.0
		9x9	64	50.3	10.7	0.6	TQFP	64	25.80	46.0	7.2

\*\*Die area in sq. mm.
 \* 4 leads fused to die attach pad