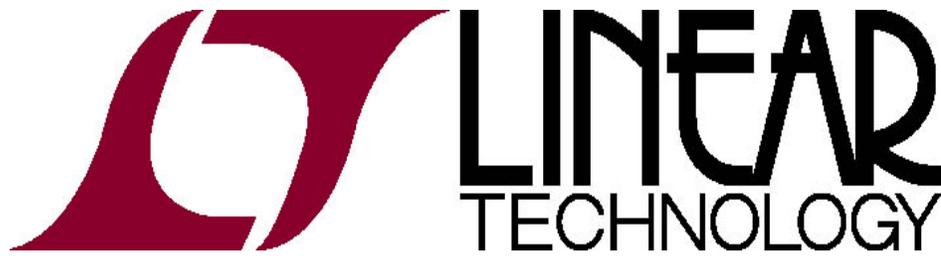


# **Application Notes for Thermally Enhanced Leaded Plastic Packages**



<b>1.0</b>	<b>Introduction</b>	<b>1</b>
<b>2.0</b>	<b>PCB Design Requirements</b>	<b>3</b>
	<b>2.1 Thermal Via Design</b>	<b>3</b>
<b>3.0</b>	<b>Board Mounting Guidelines</b>	<b>4</b>
	<b>3.1 Stencil Design</b>	<b>4</b>
	<b>3.2 Assembly Process Flow</b>	<b>6</b>
<b>4.0</b>	<b>Reflow Guidelines</b>	<b>6</b>
<b>5.0</b>	<b>Rework Process</b>	<b>6</b>

# 1.0 Introduction

Thermally/electrically enhanced leadframe packages offered by LTC include MSOP exposed pad, TSSOP exposed pad, SOIC exposed pad and LQFP exposed pad etc. those packages have exposed paddle on the bottom of package to provide the efficient heat removal path as well as electrical grounding to the PCB board. The package structure provides an extremely low thermal resistance path between the device junction and the exterior of case. The fig 1 is the typical example of cross-section and thermal performance from exposed pad leaded package.

Fig 2 and Fig 3 show the bottom view of exposed pad SSOP 38L and exposed pad 7x7 48L LQFP.

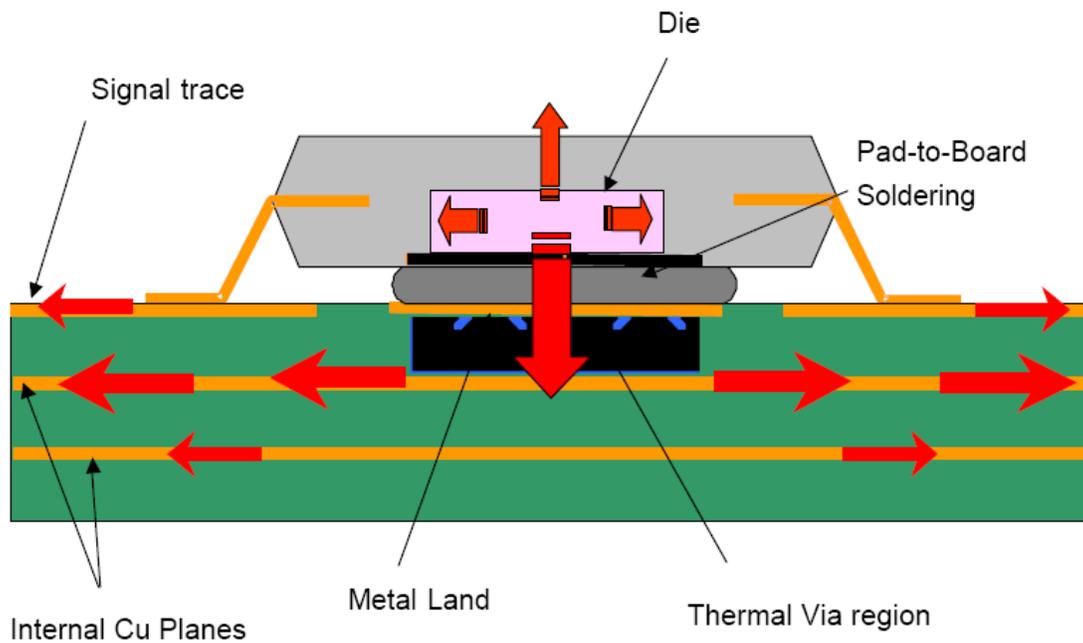


Fig. 1 Cross-section of exposed pad pkg with heat transfer

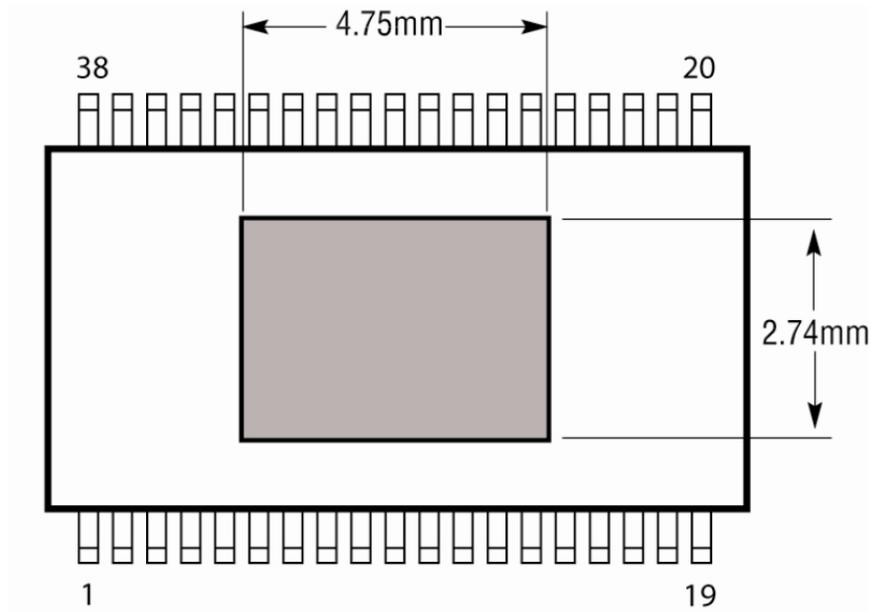


Fig 2. Example: 38L TSSOP exposed pad pkg bottom view

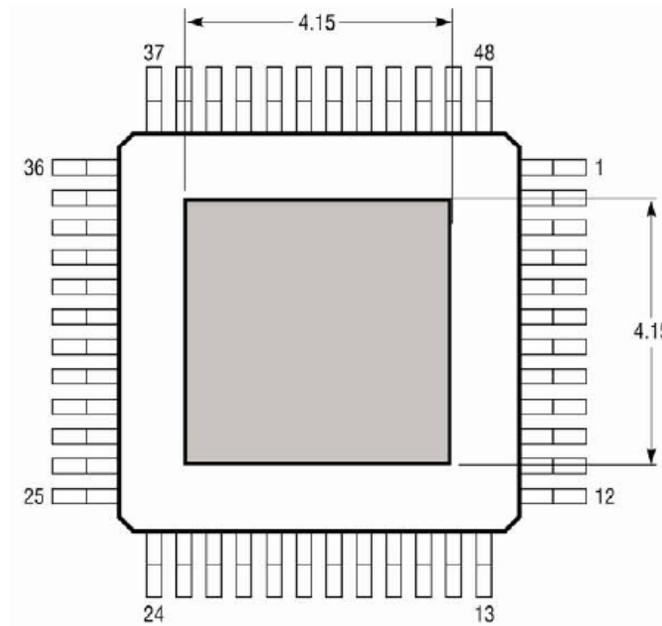


Fig 3. Example: 48L LQFP exposed pad package bottom view

## 2.0 PCB design Requirement

In order to efficiently remove the heat from the package and improve the electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad on the package, as shown in Figure 4. The solderable area, as defined by the solder mask, should be at least the same size/shape as the exposed pad area on the package. A clearance of at least 0.25mm should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

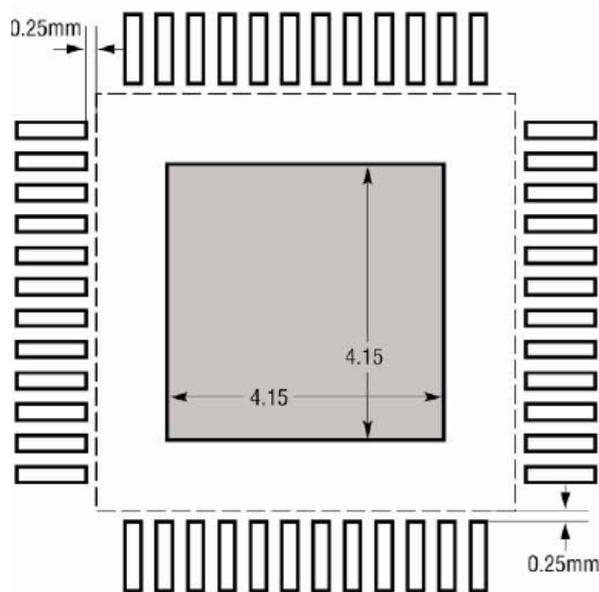


Fig 4. Example: LQFP exposed pad land pattern

## 2.1 Thermal via design

As the land pattern on the PCB provides a means of heat transfer/electrical grounding from the package to the board through a solder joint, thermal vias are recommended in order to effectively conduct heat from the surface of the PCB to the ground plane(s). These vias act as heat conduits. The number of vias are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed.

It is recommended to use 4 layer PCB board with vias to effectively remove the heat. Typical thermal vias have the following dimensions: 1.2mm pitch,

0.3mm diameter or smaller. It is desirable to avoid any solder wicking inside the via during soldering process, if the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PWB to avoid solder wicking inside the via.

These recommendations are to be used as a guideline only. Check respective product datasheet to verify which signal, power or ground plane the device should be soldered to.

### **3.0 Board Mounting Guidelines**

The following are general recommendations for mounting exposed pad leadframe devices on the PCB. This is basic requirement and it is recommended that the process should be developed based on past experience in mounting standard, non-thermally/electrically enhanced packages.

#### **3.1 Stencil Design**

For maximum thermal/electrical performance, it is required that the exposed pad on the package be soldered to the land pattern on the PCB. This can be achieved by applying solder paste on both the pattern for lead attachment as well as on the land pattern for the exposed pad. While for standard (non-thermally/electrically enhanced) leadframe based packages the stencil thickness depends on the lead pitch and package coplanarity, the package standoff must also be considered for the thermally/electrically enhanced packages to determine the stencil thickness. For a nominal standoff of 0.1mm, the stencil thickness of 5 to 8mils (depending upon the pitch) is recommended. The aperture openings should be the same as the solder mask opening on the land pattern (i.e. 1:1). Since a large stencil opening may result in poor release, the aperture opening should be subdivided into an array of smaller openings, similar to the thermal land pattern shown in Figure 5 and Figure 6. The above guidelines will result in the solder joint area to be about 80 to 90% of the exposed pad/slug area.

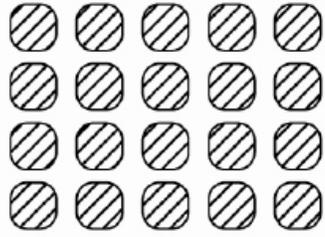


Fig 5. Recommended stencil design for TSSOP

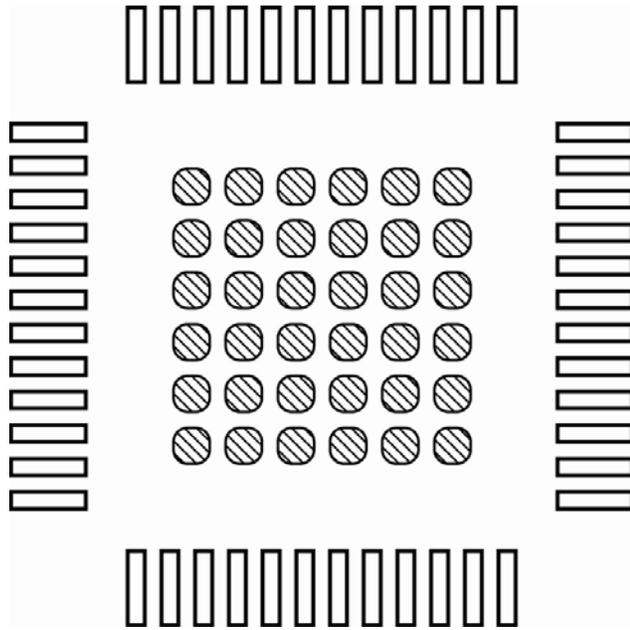
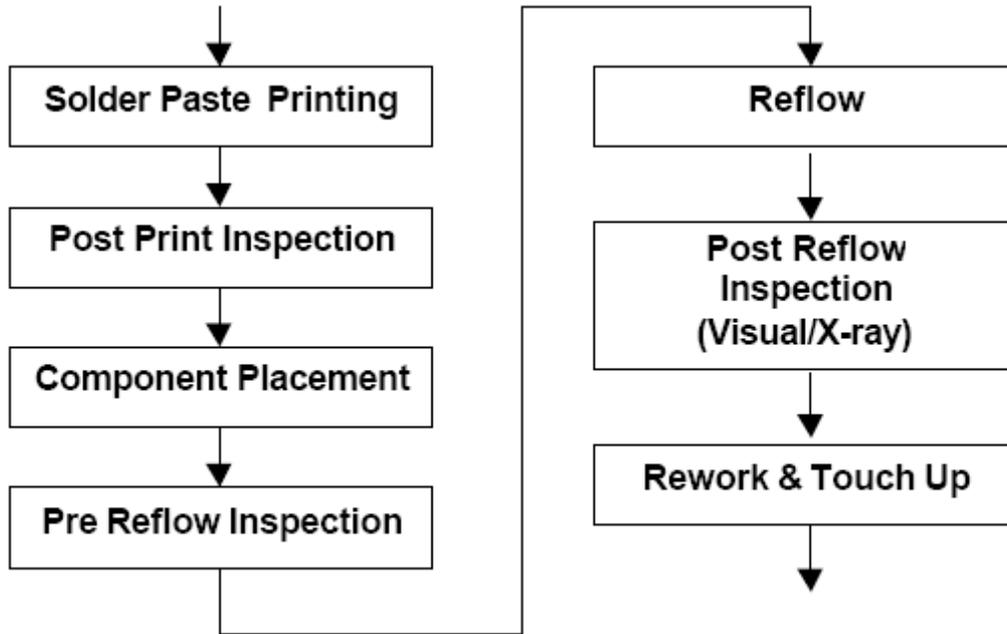


Fig 6. Recommended stencil design for LQFP

### 3.2 Assembly process flow

Thermally/electrically enhanced exposed pad package can follow the standard board mounting process. as shown in below.



### 4.0 Reflow Guidelines

The reflow profile for exposed pad packages need not be any different than the conventional, non-exposed pad packages. LTC recommends following the solder paste supplier's recommendation to optimize flux activity and also to achieve proper melting temperature of the alloy within the guidelines of J-STD-20 and not exceeding the devices moisture sensitivity level.

### 5.0 Rework

The traditional steps in rework or repair process can be identified as below:

- (1) Unsolder old component from the board
- (2) site redress and cleaning
- (3) solder paste apply
- (4) new component placement and attachment

To proper removal of the part, localized heating of the part using special nozzles is recommended, and avoid adjacent parts solder melting/reflow. Preheat of PCB at 70C from the bottom is recommended, the ideal reflow

profile should be the same as the one used for mounting the part and the reflow zone between 20-60 seconds, depending on the paste used.

Once the part is removed, site can be cleaned by vacuum desoldering or wick, after all residual solder removed, the site should be cleaned with appropriate solvent such as alcohol and a lint-free swab.

After site cleaning, a miniaturized stencil for individual component should be aligned to the site, use metal squeegee blade to apply the paste and paste should be applied in one pass, to avoid any inadvertent overprinting.

The new part should be placed on the site after paste application. And the alignment to be verified by high resolution monitor, then reflow to complete the part's attachment.