Rail-to-Rail Output Dual Comparator Resolves 150MHz Signals While Shifting from Analog to Digital Voltage Levels

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Introduction

The LT1715 is among the industry's fastest dual comparators, featuring a propagation delay of 4ns and a toggle rate of 150MHz. It is also versatile, offering separate input and output power supply pins that allow the analog input range to be completely independent of output logic levels. Internal hysteresis makes the LT1715 easy to use, even with noisy or slow moving input signals. Additional features include an input common mode range that is not only ground-sensing, but extends 100mV below the negative rail, as well as a high-current rail-to-rail output stage. The LT1715 uses little power—just 5.6mA per comparator on 5V dual supplies, or 4.6mA on a 3V single supply. To save space, both comparators fit in an MS10 package.

Circuit Description

Input Stage

Figure 1 shows a simplified schematic of the input stage, composed of a PNP differential pair with additional circuitry to improve both common mode and differential mode voltage ranges. First, the Schottky diodes at the emitters of the input devices protect them from reverse base emitter breakdown when the differential input voltage is large. Nominally, with inputs approximately equal, both PNPs are forward biased, their emitters are at equal potentials, and the Schottky diodes conduct equal currents. If a differential signal is applied, the emitters of the input transistors see a differential voltage as well, eventually turning off the Schottky diode on the lower-potential input when the differential signal reaches about two diode drops. At that point, since the current source in the cathode of the Schottky diode is larger than either of the input transistor current sources alone, the NPN input transistor will turn on to conduct current in addition to the current source for the PNP input device. This action limits the reverse-bias on the PNP input transistor to one NPN V_{BE}. An equally important benefit of the topology is that the higher of the differential inputs can swing above the common mode range without corrupting output polarity. Therefore, as long as one input remains within the common mode range, the other input is effectively rail-to-rail.

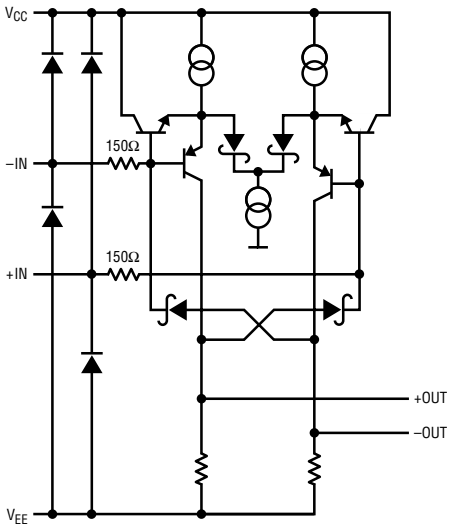

Figure 1. Input stage topology

The other pair of Schottky diodes prevent phase reversal when input voltages go below the input common-mode range. When one input is taken below the bottom rail with the other input remaining within the common-mode range, the transistor with the lower input voltage begins to saturate. At that point, the voltage on the gain resistor approaches the negative rail, potentially falling below the voltage on the opposing gain resistor. By tying the opposing gain resistor through a Schottky diode to the input, the opposing gain resistor's voltage will be pulled low with the falling input. Since the difference of the PNP V_{BE} and the Schottky diode drop is greater than the voltage on the gain resistor, the opposing collector will be pulled below the negative rail before the lower potential input transistor saturates and the voltage on its collector falls to the negative rail. The input stage therefore maintains the correct output polarity.

Table 1: Typical LT1715 specifications, T_A = 25°C

Parameter	Conditions	Value
Propagation Delay	Overdrive = 20mV	4ns
Maximum Toggle Frequency	V_{IN} = 100mV, V_{OUT} from <1V to >4V	150MHz
Input Supply Current	V_{CC} = 5V, V_{EE} = –5V	1mA
Output Supply Current	$+V_S$ = 5V	4.6mA
Input Supply Voltage	Full Temperature Range Limits	2.7V to 12V
Input Offset Voltage	V_{CC} = 5V, V_{EE} = –5V, V_{CM} = 1V	0.4mV
Input-Referred Hysteresis	V_{CC} = 5V, V_{EE} = –5V, V_{CM} = 1V	3.5mV

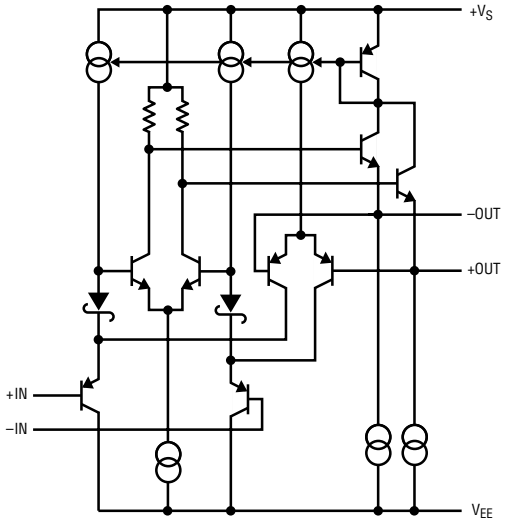

Figure 2. Gain stage topology

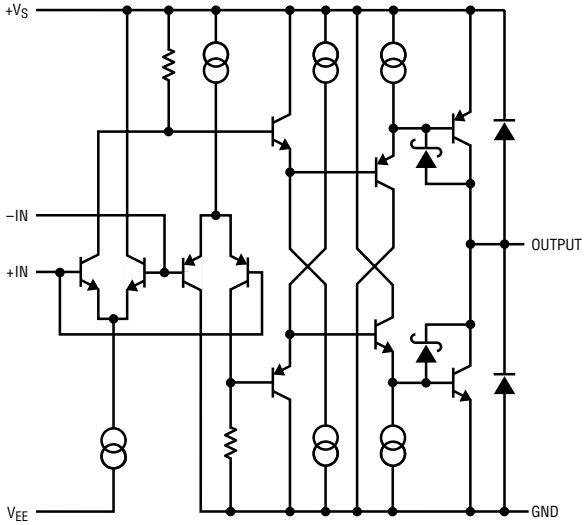

Figure 3. Output stage topology

Gain and Hysteresis Stage

The gain stage, shown simplified in Figure 2, is primarily composed of an NPN differential pair. A pair of PNP emitter followers buffers the signal from the input stage, after which a pair of Schottky diodes level shifts the signal to avoid saturating the differential pair's current source. At the differential pair's collectors, the signal is buffered through another pair of emitter followers before entering the output stage. Hysteresis is created by steering a current, based on the output polarity of the gain stage, to the emitter followers at the input of the stage, changing their forward bias voltage. Since the current for the hysteresis is mirrored from the same source as the emitter follower legs, the amount of voltage hysteresis is very accurately controlled.

Output Stage

Figure 3 shows a simplified output stage schematic. First, the differential signal from the gain stage is split into two independent drive signals using two complementary differential pairs, one referenced to each rail. Both upper and lower signals are then level shifted one diode further from the rail through an emitter follower, and then buffered through a second emitter follower for current gain to the output device. The output transistors are in a common emitter configuration for rail-to-rail output swing, with Schottky clamps to prevent saturation. Lastly, reverse biased ESD diodes at the output protect the circuit from ESD strikes.

Split Supply Flexibility

The LT1715 has separate supply pins for the input and output stages that allow flexible operation, accommodating separate voltage ranges for the analog input and the digital output. Of course, a single 3V or 5V supply may be used by connecting $+V_S$ and V_{CC} together and by connecting V_{EE} to GND. The following rules must be adhered to in any configuration:

$$2.7V \le (V_{CC} - V_{EE}) \le 12V$$

$$2.7V \le (+V_S - GND) \le 6V$$

$$(+V_S - V_{EE}) \le 12V$$

$$V_{EE} \le GND$$

Although the ground pin need not be tied to system ground, most applications will use it that way. Figure 4 shows several valid configurations. The final one is less common, but may be useful as a level translator; the input stage is run from –5.2V and ground while the output stage is run from 3V and ground. In this case the common mode input voltage range does not include ground, so it may be helpful to tie V_{CC} to 3V. Conversely, V_{CC} may also be tied below ground, as long as the above rules are not violated.

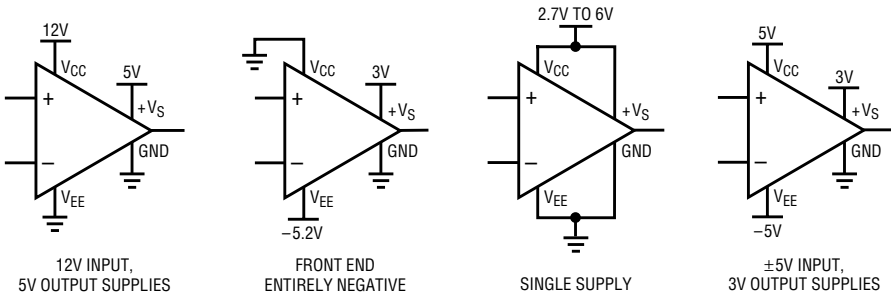

Figure 4. Variety of power supply configurations

Blazing Speed

Toggle rate is not always specified for a comparator and may not be needed in all applications. However, in fast clock and data transceivers, peak detectors and crystal oscillators, the ability of the part to toggle from rail to

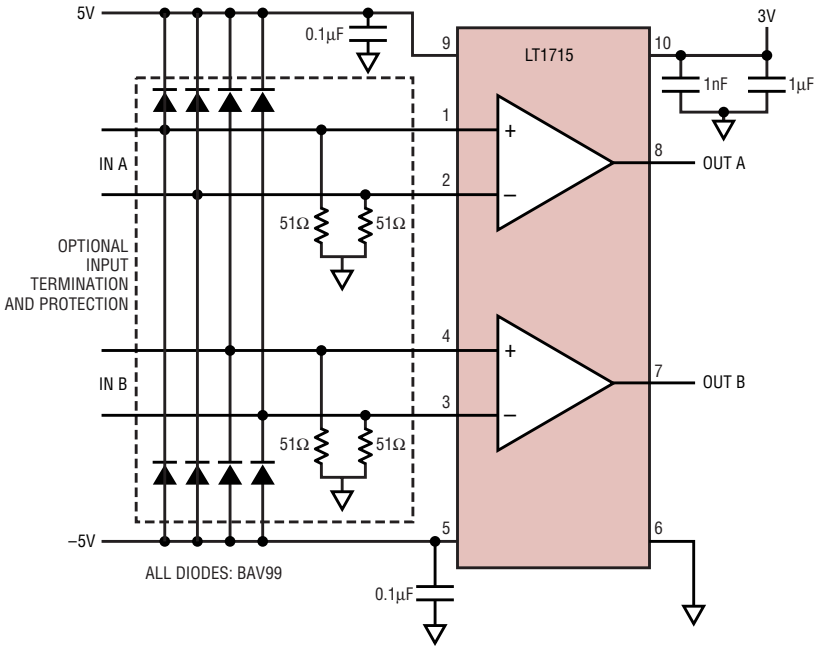

Figure 5. 100MHz dual differential line receiver

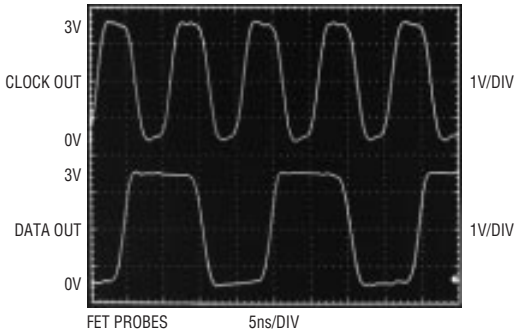

Figure 6. Line receiver response to 100MHz Clock, 50MHz data, both with 25mV$_{P-P}$ Inputs

rail quickly is very important. While designers often use the rise and fall times or the propagation delay of a comparator to approximate the maximum toggle frequency, this calculation is usually overly optimistic, especially in rail-to-rail output designs. The LT1715 was designed to maximize toggle rate, and can typically be used up to 150MHz as stated in the data sheet.

Applications

Dual Differential Line Receiver

The high speed and flexibility of the LT1715 make it ideal for line receiver or data recovery applications. The well-controlled offset and hysteresis combined with the fast propagation delay and high frequency toggle rate allow this circuit to accurately receive a wide variety of input signals. The flexibility of the power supplies allows the output logic to conform to almost any standard—ECL, PECL, TTL, etc.—without wasting power and with minimal external resistors. Figure 5 shows a complete receiver with almost 9V of input common mode range and a 150MHz capable 3V LVCMOS compatible output. Figure 6 shows the clean output waveforms resulting from 25mV$_{PP}$, sinusoidal clock and data inputs at 100MHz and 50MHz, respectively.

Shown at the inputs of the LT1715 are termination resistors for terminating 50Ω coaxial cable as well as fast clamp diodes—recommended when data lines are at risk of large ESD strikes.

Fast, Accurate Peak Detectors

Peak detectors that work well at high frequency are surprisingly difficult to make. The requisite comparator needs significant output current drive, high slew rates, and the ability to pulse on and off rapidly to accurately place charge on a sampling capacitor. Figure 7 shows the LT1715 in a closed loop peak detector. The fast 1N5711 Schottky diode and 2kΩ limiting resistor are placed inside the feedback loop so that their drops do not affect the DC accuracy of the output voltage. The diode turns on only when the output of the LT1715 is higher than the output sampling capacitor, at which point the LT1715 slews the capacitor high, current limited by the 2kΩ series resistor. Without this current limiting, the current drive capabilities of the LT1715 combine with propagation delay and hysteresis to give the output a positive DC offset resulting from overshoot. When the capacitor voltage has exceeded the input signal by the LT1715's hysteresis band, the output of the LT1715 slews to the bottom rail, turning off the diode. In this state, the PNP input topology of the LT1715 is highly beneficial—the non-inverting input is less than the inverting input, so the PNP inverting input transistor is off (the lightly biased NPN protection device will sink under 6µA if on), leaving the sampling capacitor to be drained only by the 1MΩ pull down resistor. Figure 8 illustrates the accuracy of the closed loop detector for both 1V$_{PP}$ and 4V$_{PP}$ ground-centered input sinusoids. With the input supply connected to split supplies, there is no need for diode clamping of an input signal that goes below ground since the comparator is not overdriven. Therefore, high impedance is maintained at the input to the detector and there is no recovery penalty for increasingly negative signals. Simultaneously, the output stage benefits from being separately connected to a 5V single supply. In this configuration, the output need only slew from ground, and not from

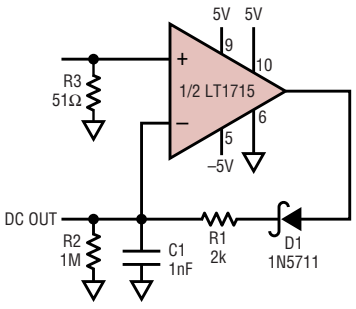

Figure 7. High frequency positive peak detector

V_{EE} on each pulse, significantly improving high frequency performance. Figure 9 shows the impressive linearity created by the very high speed of the comparator. Even when output accuracy drops to 80% at 100MHz, the LT1715 still has linearity to within a few percent over a broad range of amplitude. This linearity allows the user to scale the output to retrieve the actual input amplitude even at frequencies where the detector has significant error, so long as the frequency of the signal is known.

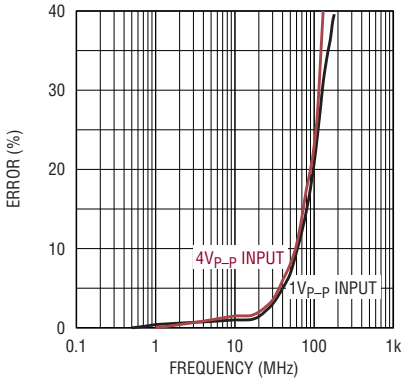

Figure 8. Percent error vs frequency

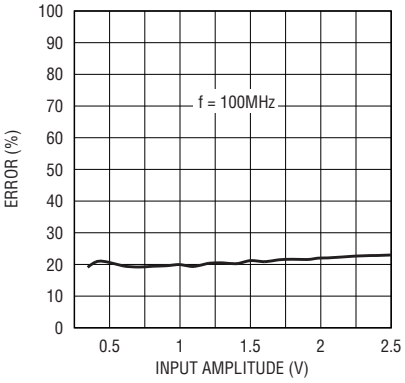

Figure 9. Percent error vs input amplitude at 100MHz

Rail-to-Rail Pulse Width Modulator

In applications where a high frequency variable PWM generator is needed, the LT1715 provides a small and simple solution, as shown in the circuit of Figure 10. The top comparator, U1A, acts as a ramp generator. Biasing resistors R1 and R2 and a 7:1 positive feedback ratio through R3 set the positive input to approximately 2.5V±250mV. The inverting RC feedback creates a relaxation oscillator by tripping the comparator into the opposing output state each time it passes through the ±250mV positive input voltage. The 880kHz triangle wave created on C1 is then passed to the inverting input of the second comparator, U1B. The input signal to be modulated, referenced from 0V to 5V, is first divided to match the 2.5V ±250mV ramp input, and then the duty cycle is set with the second comparator acting as a threshold detector.

The linearity of the pulse width modulated signal can be ascertained by placing a low frequency filter at the output to eliminate switching noise. This demodulates the signal, which can then be viewed and compared with the original input signal. Measured with a spectrum analyzer and a 1KHz reference signal, this circuit's distortion products are better than –70dB (.03%) for small input amplitudes. Figure 11 shows the impressive distortion figures versus the amplitude of the 1KHz sinusoid. As the amplitude of the input increases, a larger fraction of the imperfect RC-decay triangle wave is used, increasing error. At input amplitudes beyond $4V_{PP}$, higher order distortion begins to dominate as the output swing of the LT1715 begins to reach its limits.

Conclusion

The versatility and ease-of-use of the LT1715 dual comparator allow it to solve a wide variety of system design problems. Its fast 4ns propagation delay, 150MHz toggle rate, and flexible supply configuration make the LT1715 shine in applications where many comparators fall short.

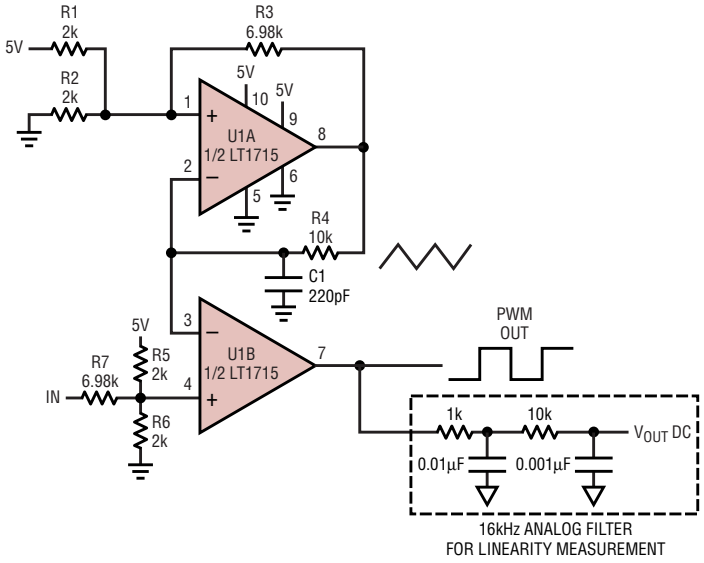

Figure 10. Rail-to-rail 1MHz pulse width modulator

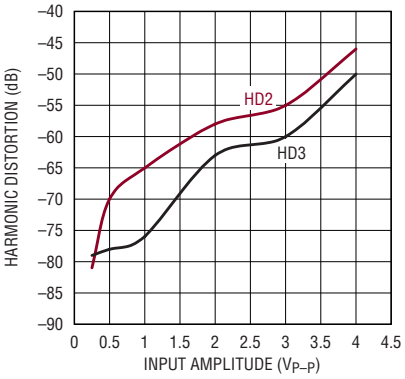

Figure 11. Demodulated PWM distortion vs input amplitude