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Versatile, Low Noise, Active Filter Offers Repeatable Performance to 10MHz

by Nello Sevastopoulos

Introduction

The increasing speeds and dynamic ranges of modern communication and control systems make for filter requirements that can be challenging to satisfy. Some relief is offered by signal converters with high sampling rates, which can alleviate the need for selective filters, but even so, some sort of band limiting is still required. To add to the challenge, an active filter can now be expected to provide amplification along with band limiting to eliminate components in the signal path.

“...the performance of the LT1568 is precisely repeatable from device to device, making it possible to manufacture filters in volume without the need for costly production trimming.”

Some wireless systems face yet another problem. Even though the use of oversampling converters has significantly simplified filtering, signal sub-harmonics from neighboring systems can intrude on a converter's allowed bandwidth, and in the end, totally redefine the filtering requirement.

To solve this problem without adding complex circuitry, the simple lowpass filter originally placed in front of the converter must perform band rejection with repeatable depth from unit to unit in high volume production.

The LT1568 meets these challenges by offering an astonishingly simple-to-use, but extremely versatile filter. It requires only a few external passive components to satisfy complex filtering requirements, including band rejection. Most important, though, is that the performance of the LT1568 is precisely repeatable from device to device, making it possible to manufacture systems in volume without the need for costly production trimming.

Device Description

Figure 1 shows a block diagram of the LT1568. The part is configured as dual 2nd order matched building blocks, which can be used in a variety of ways for different applications. The two filter blocks can be interconnected to obtain 4th order or higher filter transfer functions with an optional notch.

Each individual filter block uses two low noise ($1.5\text{nV}/\sqrt{\text{Hz}}$ input voltage noise) operational amplifiers, where one op amp is configured as an integrator (with capacitor C1 connected in its feedback loop) and the other

continued on page 3

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Issue Highlights

Our cover article introduces the LT1568, a simple-to-use, but extremely versatile, active-RC filter building block. It requires only a few external components to meet complex high frequency filtering requirements, including selective band rejection. The performance of the LT1568 is precisely repeatable from device to device, making it possible to manufacture systems in volume without the need for costly production trimming.

This issue also features the third article in a 3-part series about Powered Ethernet devices. The first two articles covered PSEs (Power Sourcing Equipment) and PDs (Powered Devices), while this third part covers the issues regarding detection and classification of PDs.

The remaining feature articles cover a host of exciting new devices in the Linear Technology lineup, including:

The LTC2600, LTC2610 and LTC2620 are octal 16-, 14- and 12-bit, serial-input, 2.5V–5.5V single-supply, rail-to-rail voltage-output digital-to-analog converters. Each device packs an unprecedented number of features and unmatched performance into a tiny package.

The LT1950 is a current mode DC/DC controller designed to reduce size and improve performance in forward, SEPIC, flyback and boost converters. The LT1950 offers several programmable features, including switching frequency, slope compensation, leading edge blanking and adaptive maximum duty cycle clamping. Programming is remarkably simple, allowing converter solutions to be easily optimized for high performance, low cost and small component size.

LT3010 is a high voltage, micropower, low dropout linear regulator in a thermally enhanced 8-lead MSOP package. It can provide up to 50mA of output current from input supplies ranging from 3V to 80V. Dropout voltage on the LT3010 is only 300mV when delivering up to 50mA of output current. The LT3010 operates on only 30 μ A of quiescent current. It can be

put into a low-power shutdown state, bringing quiescent current down to 1 μ A.


The LT6700-1, LT6700-2 and LT6700-3 are micropower, dual comparators that include an internal 400mV reference and are optimized for core (V_{CC}) operation on single supply voltages from 1.4 to 18V. This family offers Over-The-Top[®] capability for both the inputs and outputs from V_{EE} to 18V above V_{EE} , regardless of V_{CC} . These parts keep the pin-count to a minimum by internally committing one of the inputs of each comparator section to the production-trimmed 400mV reference—the different dash-number designations denote different comparator connections. These comparators all include a built-in input hysteresis of 6.5mV nominal, a feature that simplifies design by minimizing external component count. The comparator outputs are open-collector types, allowing them to form convenient wired-AND logical connections or individually drive up to 40mA loads.

The LTC2414 and LTC2418 are 8- and 16-channel, No Latency $\Delta\Sigma^{\text{TM}}$ ADCs in the Linear Technology's high accuracy ADC family. Each combines a large number of inputs and extremely high accuracy, making it possible to acquire data from a variety of sensors directly with a single device. There are no complex tradeoffs between common mode voltages, large or small input ranges and temperature drift concerns. These devices are available in the 28-pin narrow SSOP package.

The LTC5508 is a very wide bandwidth RF power detector that can be used in RF applications that cover a wide range of frequencies and power levels. This device exhibits excellent sensitivity and temperature stability over an input frequency range of 300MHz to 7GHz and an input power range of –32dBm to 12dBm. The operating current is less than 600 μ A, and in shutdown mode, the quiescent current is less than 2 μ A. The LTC5508 is packaged in an SC70


LTC in the News...

On April 15, Linear Technology Corporation announced its financial results for the 3rd quarter of fiscal year 2003 ended March 30. According to Robert H. Swanson, Chairman of the Board and CEO, "This was a good quarter for us as we grew sales 6% and profits 8% over the previous quarter. We continue to be strongly profitable as demonstrated by our 39% return on sales. We focus our efforts on unique, high-performance analog intensive, market opportunities often in the newest generation end user products. This enables us to achieve good financial results during these difficult economic and geo-political times. However, accurately forecasting short-term results remains a challenge. Nevertheless, we had good momentum in the March quarter and consequently estimate that sales and profits for the June quarter will grow sequentially in the mid to high single digits, 5% to 8%."

The Company reported net sales of \$153,750,000 and net income of \$60,622,000 for the quarter ended March 30, 2003. Diluted earnings were \$0.19 per share. A cash dividend of \$.06 per share was paid on May 14, 2003 to stockholders of record on April 25, 2003. 

package, and requires only one or two external components.

Starting on page 29 are three new Design Ideas, including a redundant, hot swappable power system using standard power modules, and a way to double the output current capability of a standard buck converter.

At the back are six New Device Caméos. See www.linear.com for complete device specifications and applications information. 

LT1568, continued from page 1

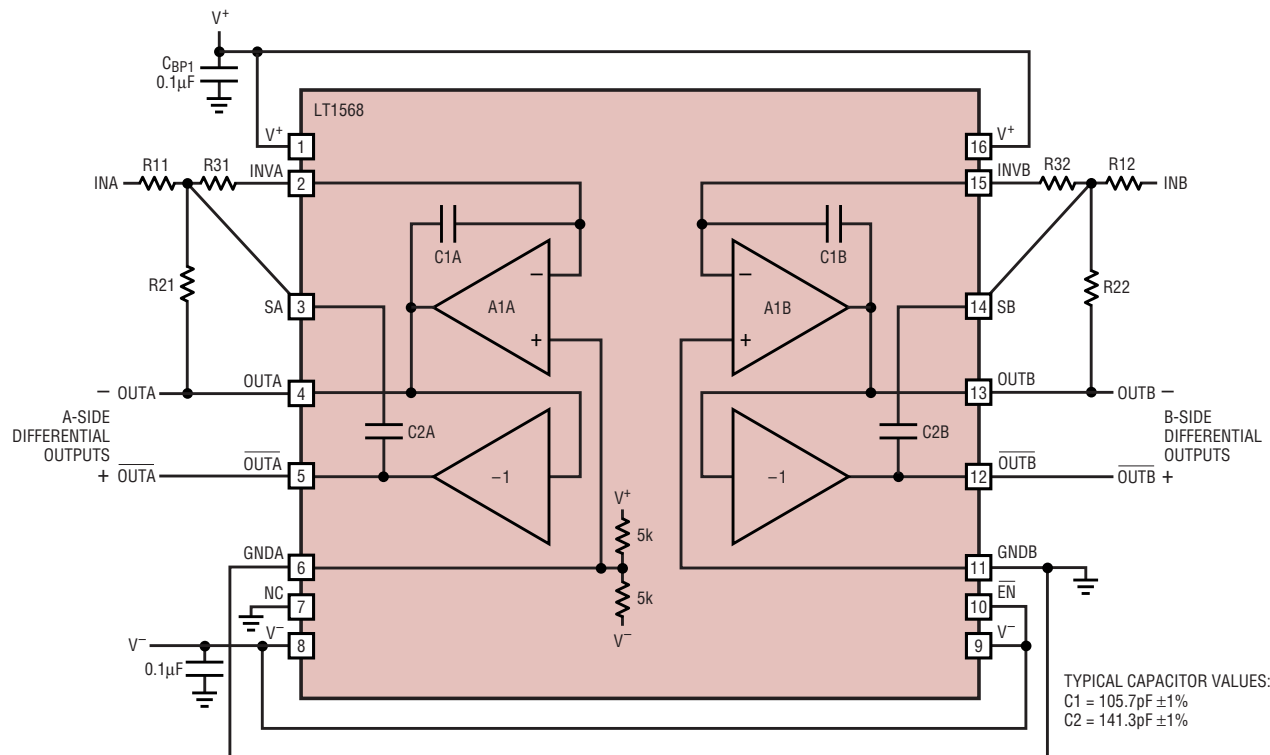


Figure 1. LT1568 block diagram. The configuration of external components shown is for a dual 2nd order lowpass filter.

one is connected as an inverter. The inverter senses the output signal and drives the bottom plate of capacitor C2. The inverter op amp output is pinned out, and it can be used in applications requiring differential outputs or an output with phase reversal. This simple building block, when used with a few external passive components, can provide various 2nd order or 3rd order filter functions. A simple case is shown in the block diagram of Figure 1, where a few resistors are the only external components required to make a dual lowpass filter.

One of the features of this device is repeatable AC performance from part to part. This is achieved by trimming the internal C1 and C2 capacitors to a better than 1% tolerance, and by trimming the gain bandwidth product (GBW) of the internal op amps. Thus, any small error caused by the finite speed of the LT1568 active circuitry is highly predictable.

Application Examples

The LT1568 is extremely versatile, due in part to its generic internal architecture. The values of the exter-

nal resistors for a few classical filter responses are given in the LT1568 data sheet.

The resistor values for a wide selection of filter responses can be determined by using the *LT1568 Design Guide* spreadsheet, available at www.linear.com. (See the sidebar on page 5.)

Dual 2nd Order Lowpass Filter

The topology of the LT1568 building blocks is well suited for lowpass filter responses of arbitrary values of Q, cen-

ter frequency (f_0), and passband gain (H_0). The extremely low noise characteristics of the LT1568 allow voltage gain to be taken with filtering, thus eliminating the need for pre-amplification. These parameters are uniquely defined by the value of three external resistors, R1, R2 and R3, respectively, as shown in Figure 2. Note that each section can provide a differential or single-ended output signal.

These resistors have equal values for a unity passband gain 2nd order Butterworth lowpass filter ($Q = 0.707$):

$$R1 = R2 = R3 = 1.28\text{k}\Omega \cdot (1\text{MHz}/f_c)$$

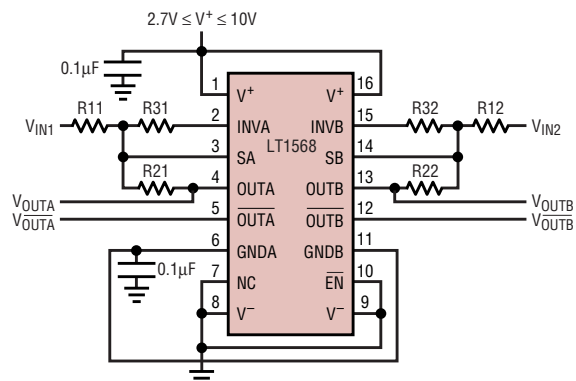


Figure 2. Dual 2nd order lowpass filter (single supply operation)

Table 1. Recommended resistor values

Filter Type	f _{CUTOFF} *	Gain (V/V)	R11, R12 (Ω)		R21, R22 (Ω)		R32, R33 (Ω)	
			Calculated	1%	Calculated	1%	Calculated	1%
2nd Order Butterworth, Lowpass	1MHz	2	899.9	909	1.799k	1.78k	906.5	909
	2.5MHz	√2	420.2	422	594.2	590	430.9	432
	5MHz	1	248.7	249	248.7	249	250.5	249
2nd Order ±0.25dB Ripple, Lowpass	650kHz	4	772.4	768	3.089k	3.09k	614.8	619
	2.3MHz	2	287	287	573.9	576	255	255
	7MHz	1	122.9	124	122.9	124	119.9	121

*For butterworth lowpass responses the cutoff frequency (f_{CUTOFF}) is the -3dB frequency, while for the ±0.25 ripple Chebyshev responses the cutoff frequency is the ripple bandwidth.

This expression can be used for cutoff frequencies up to 10MHz. For instance, for a 2.5MHz cutoff frequency, all three resistors should be 512Ω (or 511Ω, standard resistor value). Unequal values of these three resistors allow gains other than unity, and all other response types, unity gain or not.

For the sake of completeness a simple analysis of the 2nd order circuit is illustrated here. The filter gain, center frequency and Q, Figure 2, can be easily calculated when the internal op amps are assumed to be ideal:

$$H_0 = \text{DC GAIN} = -\frac{R_2}{R_1}$$

$$\omega_0 = 2\pi f_0 = \frac{1}{2\pi\sqrt{C_1 \cdot C_2 \cdot R_2 \cdot R_3}}$$

$$Q = \frac{\omega_0}{1/C_2(R_1 \parallel R_2 \parallel R_3) - 1/(C_1 \cdot R_3)}$$

Given the values for center frequency f₀, Gain H₀, and Q, the expressions above can be manipulated to solve for R1, R2, R3:

$$R_3 = \frac{1}{Q} + \sqrt{\frac{1}{Q^2} + 1.008(H_0 + 1)}$$

$$R_3 = \frac{1}{2(H_0 + 1)\omega_0 C_1}$$

$$R_2 = \frac{1}{R_3 \cdot C_1 \cdot C_2 \cdot \omega_0^2}$$

$$R_1 = \frac{R_2}{H_0}$$

$$C_1 = 105.7\text{pF}, C_2 = 141.3\text{pF}$$

For applications where f₀ • Q • H₀ ≤ 2MHz for the second order lowpass

section, the algorithm illustrated above can be used to calculate resistor values.

For applications above 2MHz the resistor values can still be calculated with this simple algorithm but it may produce responses that will deviate from an ideal textbook filter response. This is a result of the finite GBW of the internal op amps. Nevertheless, as the low noise op amps and the internal capacitors of the LT1568 are trimmed, these higher frequency responses still remain repeatable from part to part.

The LT1568 Design Guide corrects for the finite GBW of the LT1568 internal op amps.

Table 1 shows a sample of recommended resistor values for a 2nd order Butterworth response and for a 2nd order ±0.25dB Chebyshev responses. Arbitrary values of gains are chosen. The range of cutoff frequencies and gain the LT1568 can provide is dictated by the spread of the values of the external resistors.

The lowest recommended center frequency is dictated by the value(s)

of the required external resistors. High external resistor values add to the overall output DC offset of the filter. For instance a 200kHz, 2-pole Butterworth response dictates R11 = R12 = R13 = 6.4k. The output DC offset created by these resistor values is 9.6mV, assuming I_{BIAS} = 0.5μA for the high speed internal op amp.

For lowpass responses, the recommended set of center frequency, Q, and Gain, should obey the following:

$$f_0 \cdot Q \cdot H_0 \leq 10\text{MHz}$$

with Q ≤ 5 and f₀ ≥ 0.1MHz

4th Order, All Pole, Lowpass Filter

The two identical sections of the LT1568 can be cascaded to create a 4th order lowpass filter response as shown in Figure 3. Each 2nd order section of the filter should still comply with the f₀, Q and Gain limitations described above. To find the value of the center frequency, f₀'s, and Q's for the desired lowpass function use FilterCAD™, available for download from www.linear.com.

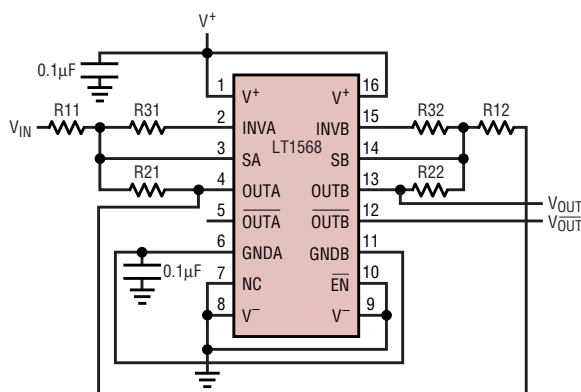


Figure 3. 4th order lowpass filter (single supply operation)

Example: design a lowpass filter that processes signals from DC to 5MHz, and provides an attenuation of 25dB or more to signals above 10MHz. The ripple of the 5MHz passband should not exceed $\pm 0.5\text{dB}$ (or 1dB peak-to-peak) and, the passband gain should be 3dB, or 1.414V/V. Note, for all-pole 4th order filters, the attenuation at twice cutoff cannot get much better than 24dB to 30dB. Figure 4 shows the theoretical response of a Chebyshev lowpass filter with a 0.6dB peak-to-peak ripple. A lower ripple, 0.6dB_{P-P} ripple vs 1dB_{P-P}, is deliberately chosen as a guard-band for external resistor tolerances and PC board parasitics.

Note, for a Butterworth response instead of the Chebyshev response, in order to maintain the stated passband and stopband specifications, a 6th order filter would be required with a -3dB filter cutoff frequency of 5.86MHz. Hence, a Chebyshev design can save components and cost.

The values of the two center frequencies and the values for the corresponding Q 's of the 0.6dB_{P-P} Chebyshev lowpass filter can be easily obtained through FilterCAD and are shown in Figure 4.

Table 2 shows the calculated resistor values to be used in conjunction with the LT1568 filter shown in Figure 3. For this particular exercise the LT1568 Design Guide was used with the Custom Filter Design feature of the spreadsheet.

Adding a Stop-Band Notch

Sometimes, the gain roll-off of an all-pole lowpass filter is insufficient

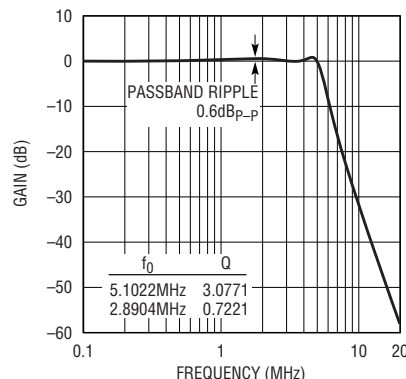


Figure 4. Frequency response for 4th order Chebyshev filter

Retrieving and Using the LT1568 Design Guide Spreadsheet

LT1568 Design Guide spreadsheet is available at www.linear.com. This Microsoft Excel® spreadsheet determines the external component values for a variety of responses, including:

- ☐ Single/Dual 2nd Order Butterworth Lowpass
- ☐ Single/Dual 2nd Order Bessel Lowpass
- ☐ Single/Dual $\pm 0.25\text{dB}$ Ripple Lowpass
- ☐ Single/Dual 3rd Order Butterworth Lowpass
- ☐ Single/Dual 3rd Order Bessel Lowpass
- ☐ 4th Order Butterworth Lowpass
- ☐ 4th Order Bessel Lowpass
- ☐ 4th Order $\pm 0.25\text{dB}$ Lowpass
- ☐ 4th Order Elliptic Lowpass
- ☐ Single/Dual 2nd Order Bandpass
- ☐ 4th Order Narrow-band Bandpass
- ☐ 4th Order Wide-band Bandpass
- ☐ Custom Response with Arbitrary $f_0/Q/\text{Gain}$ Values

The external component values for other responses can be determined as long as you know the center frequency or frequencies, Q or Q_s , and gains. FilterCAD (also available, free of charge from www.linear.com) can be used to find these parameters. Then, simply plug these parameters into the LT1568 Excel Spread Sheet to calculate the required resistor values.

To retrieve the LT1568 Design Guide spreadsheet, go to www.linear.com and open the LT1568 data sheet (type "LT1568" in the search text box). Click the link to the LT1568 Design Guide spreadsheet to open it (or, right-click the link and choose Save Target As to save the spreadsheet to your computer).

to reject a specific frequency outside the system passband. This can happen when an interfering signal, although outside the system cutoff frequency, is still close enough to affect performance. A seemingly simple solution to this problem is the addition of a notch in the filter's transition band, which, before the arrival of the LT1568, was easier said than done.

The unique architecture of the LT1568 allows the addition of a notch by simply adding an external capacitor between the summing node of the first stage and the summing node of the second stage, as shown in Figure 5. Also, for this notch topology, the lowpass sections should be cas-

caded via the inverting output ($\overline{\text{OUTA}}$) of the first section. This proprietary technique is described in detail in the LTC1562 data sheet (also available at www.linear.com.)

Capacitor C_N and resistor R12 are the only external passive components affecting the accuracy and repeatability of the notch frequency—the notch frequency is inversely proportional to the square root of the product of C_N and R12.

As very low tolerance resistors are readily available, so the burden for frequency accuracy lies on the tolerance of C_N . For instance, if C_N has a $\pm 5\%$ tolerance, the notch variability is approximately $\pm 2.5\%$, so a capacitor

Table 2. Resistor values for 4th order Chebyshev

R11		R21		R31		R12		R22		R32	
Calculated	1%	Calculated	1%	Calculated	1%	Calculated	1%	Calculated	1%	Calculated	1%
463.6	464	463.6	464	121.5	121	356.3	357	534.5	536	355.5	357

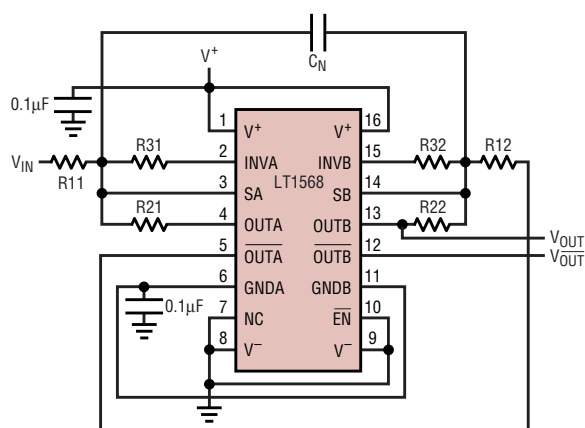


Figure 5. Adding a notch to the 4th order lowpass filter (single supply operation)

Table 3. Component values for lowpass filter with stopband notch, Type 1 (Figure 6), $f_c = 2.5\text{MHz}$

R11 = R21 (Ω)	R31 (Ω)	R12 = R22 (Ω)	R32 (Ω)	C_N (pF)
374	549	698	221	47

with 2% tolerance is recommended to reduce the variability to ~1%.

The *LT1568 Design Guide* can be used to calculate the external component values required to reliably produce this type of filter response. Use the Fixed Filter Response section. This design offers a choice of two types of lowpass filters with a stopband notch:

- Type 1: A 4th order lowpass with $\pm 0.25\text{dB}$ passband ripple and a notch such that the attenuation at $1.35\times$ filter cutoff is $>20\text{dB}$.
- Type 2: Same passband as type 1 but the notch is moved to a higher frequency such that the minimum attenuation at $2\times$ filter cutoff is at least 36dB .

Figure 6 illustrates the two types of filters. Both filters are normalized to a 1MHz cutoff.

It is recommended that the maximum frequency of the notch remain below 10MHz .

For example, for a lowpass filter with 2.5MHz cutoff frequency and an attenuation of better than 20dB at 3.5MHz , a Type 1 filter (from Figure 6) is chosen and the component values of Figure 5 are derived using the *LT1568 Design Guide* spreadsheet, and are shown in Table 3.

Simple and Repeatable Bandpass Filters

The LT1568 makes it possible to produce accurate selective bandpass filters in volume, until now a daunting, if not impossible, task. This is another result of its innovative topology and its carefully trimmed internal components. The LT1568 also makes the basic design of a bandpass filter extremely easy. Simply replace R_1 , the input gain- and Q -setting resistor of the filter shown in Figure 2, with a capacitor, C_{IN} , as shown in Figure 7. This simple exchange transforms the

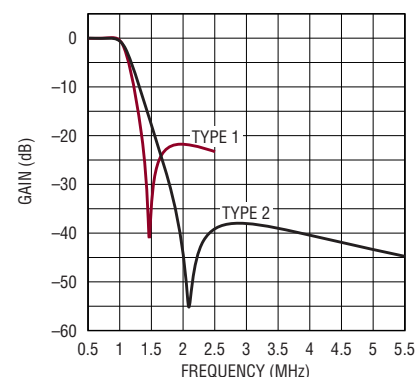


Figure 6. Frequency response for the two types of lowpass filters with a stopband notch

2nd order lowpass into a 2nd order bandpass filter.

The center frequency of the bandpass function depends on the product $R_2 \cdot R_3 \cdot C_1 \cdot C_2$, just as in the lowpass case, but it also depends on the ratio of C_{IN}/C_2 . In selective bandpass filters, more than any other parameter, the center frequency must be accurate from part to part. Low tolerance resistors are readily available, but low tolerance capacitors are not—a potential, but hardly insurmountable problem. The solution is in the choice of C_{IN} such that the ratio C_{IN}/C_2 is kept low.

For the circuit shown in Figure 7, the center frequency of each 2nd order section—assuming the LT1568 uses theoretically ideal op amps—is:

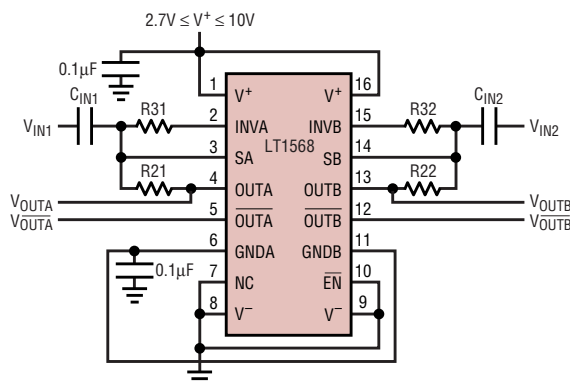


Figure 7. Bandpass configuration

Table 4. Component values for bandpass configuration

f_0	C_{IN1}, C_{IN2}	R21, R22 (Ω)	R21, R22 (Ω)
500kHz	39pF	2.74k	1.87k
5MHz	39pF	249	182

$$f_0 = \frac{1}{2\pi\sqrt{R_2 \cdot R_3 \cdot C_1 \cdot C_2}} \cdot \frac{1}{\sqrt{1 + \frac{C_{IN}}{C_2}}}$$

The problem is that C_{IN} is an external capacitor with a much greater error tolerance than the internal trimmed capacitors, C_1 and C_2 . Thus the effect of the error contributed by C_{IN} (which can reasonably be $\pm 5\%$) must be reduced to control the center frequency. The center frequency error introduced by C_{IN} is:

$$\Delta f_0 = \pm \frac{0.5\epsilon}{1 + \frac{C_2}{C_{IN}}} \%$$

where ϵ = tolerance of C_{IN} in percent

If $C_{IN} = 100\text{pF} \pm 5\%$ so that $C_{IN}/C_2 = 0.7077$ ($C_2 = 141.3\text{pF}$), then the center frequency error due to C_{IN} is approximately $\pm 1.04\%$. If $C_{IN} = 150\text{pF} \pm 5\%$ so that $C_{IN}/C_2 = 1.06$, the center frequency error due to C_{IN} is $\pm 1.28\%$. This shows that, although the LT1568 bandpass topology requires the use of a relatively high tolerance component—external capacitor C_{IN} —as long as the ratio of C_{IN}/C_2 is within certain bounds, the tolerance of the external capacitor C_{IN} does not substantially degrade the accuracy of the filter center frequency. This is hardly a limitation on the design of effective filters, because the topology does not benefit from high C_{IN}/C_2 ratios.

The expressions for Q , and gain ($H_{0(BP)}$) of the 2nd order bandpass section of Figure 7 are:

$$Q = \sqrt{\frac{R_2 \cdot C_2 \left(1 + \frac{C_{IN}}{C_2}\right)}{R_3 \cdot C_1 \left(1 - \frac{C_2}{C_1}\right) + 1}}$$

$$H_{0(BP)} = \frac{R_2 \cdot C_2}{R_3 \cdot C_1} \cdot \frac{\frac{C_{IN}}{C_2}}{\left[\frac{R_2}{R_3} \left(1 - \frac{C_2}{C_1}\right) + 1\right]}$$

At first glance, the above expressions appear problematic because they both depend on C_{IN}/C_2 . If, however, the internal capacitors C_1 and C_2 are substituted with their actual values, 105.7pF and 141.3pF respectively, and

if the ratio R_2/R_3 is replaced with “ r ” ($r = R_2/R_3$), these design equations simplify to:

$$f_0 = \frac{1}{2\pi \cdot R_3 \cdot (122.21\text{pF}) \sqrt{r \left(1 + \frac{C_{IN}}{C_2}\right)}}$$

$$Q = \frac{\sqrt{1.337r \left(1 + \frac{C_{IN}}{C_2}\right)}}{1 - 0.337r}$$

$$H_{0(BP)} = \frac{1.337 \cdot \frac{C_{IN}}{C_2}}{\frac{1}{r} - 0.337}$$

When r is eliminated in the above equations for Q and $H_{0(BP)}$, a new expression linking Q and $H_{0(BP)}$ to C_{IN}/C_2 can be derived and plotted. This is shown in Figure 8, in which the relation of C_{IN}/C_2 versus Q is plotted for a few values of the gain, $H_{0(BP)}$. It can be seen that the bandpass structure of Figure 7 is useful for C_{IN}/C_2 ratios between 0.1 and 2, values low enough to keep tolerances in check.

Note, once the ratios of C_{IN}/C_2 and of R_2/R_3 are fixed, the filter center frequency scales with the value of resistors R_2 and R_3 (that is, up to the point where the finite nature of the op amps adds a predictable error).

500kHz Bandpass Example

As an example, design a unity gain 500kHz 4th order narrowband bandpass filter that is synthesized by cascading two identical 2nd order sections, as described above. Set the Q of each 2nd order section of this

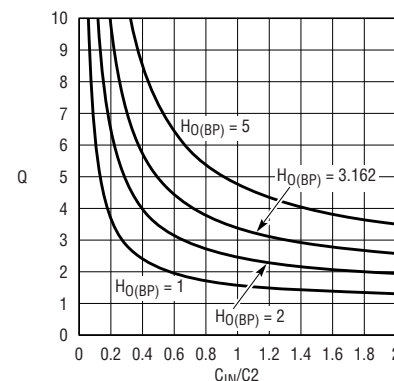


Figure 8. 2nd order bandpass filter Q vs C_{IN}/C_2 for various values of $H_{0(BP)}$

narrowband bandpass filter to 3, which yields an equivalent Q (Q_{EQUIV}) of approximately 4.6, a value determined from:

$$Q_{EQUIV} = \frac{Q_{2nd \text{ ORDER SECTION}}}{\sqrt{2^{1/n} - 1}}$$

Where n = number of cascaded 2nd order bandpass sections

For instance, for a 4th order bandpass filter:

$$n = 2$$

$$Q_{EQUIV} = 1.554 \cdot Q_{(OF \text{ SINGLE } 2nd \text{ ORDER SECTION})}$$

From Figure 8 a Q of 3 and unity gain yields:

$$(C_{IN}/C_2) = 0.276$$

$$C_{IN} = 0.276 \cdot 141.3\text{pF} = 39\text{pF}$$

Setting $H_{0(BP)} = 1$ and solving for r yields $r = 1.4164$.

Once r is known, given the desired center frequency f_0 , R_3 can be determined. For $f_0 = 500\text{kHz}$ and $R_3 = 1.937\text{k}\Omega$:

$$R_{3CALC} = 1.937\text{k}\Omega$$

$$R_{2CALC} = 1.4164 \cdot R_{3CALC} = 2.742\text{k}\Omega.$$

Figure 9 shows the measured responses for a 500kHz 4th order bandpass filter and for the same filter centered at 5MHz.

The Ever-Present Reality: Effects of Finite-GBW Op Amps

The finite GBW of the LT1568 internal op amps means that as the center frequency goes up, the actual center frequency of the filter deviates from the theoretical calculations. Here is a simple reality check: if the

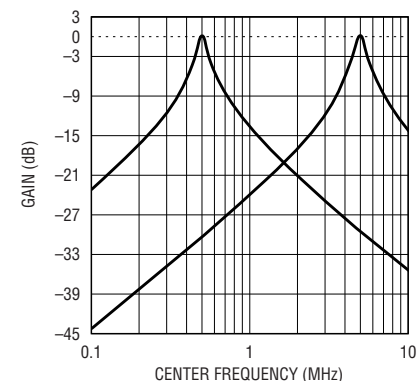


Figure 9. Frequency response for two 4th order narrow band filters with center frequencies at 500kHz and 5MHz

Table 4. Calculated and adjusted values of R3 for the circuit shown in Figure 7
($Q = 3$, $C_{IN} = 39\text{pF}$ and $H_{0(BP)} = 1$)

f_0	R3 _{CALCULATED}	Adjustment Factor R3 _{CALC} /R3 _{ADJ}	R3 _{ADJUSTED}
100kHz	9.68k	0.99	9.58
500kHz	1.936k	0.984	1.905
1MHz	968	0.978	947
5MHz	193.6	0.955	185

center frequency is 5MHz as in the previous example, at unity gain the center frequency $\cdot Q \cdot$ gain product is 15MHz. It would take improbable op amps with 1.5GHz GBW to accurately produce this type of performance.

Nevertheless, reality does not make the LT1568 any less usable as a bandpass filter. The op amps in the LT1568 *always* have the same GBW product, from part to part and lot to lot. This makes the discrepancy between theory and reality measurable, predictable and repeatable. A filter designer can easily compensate for this discrepancy in the design stage by simply choosing the values of resistors R2 and R3 that achieve the desired center frequency. No adjustment or trimming is necessary in production once the design is proven.

Table 4 shows the calculated and adjusted resistor values for four different center frequencies for the bandpass filter in the previous example. Figure 10 shows the deviation between theory and reality for $Q=3$ and $Q=6$. Because the LT1568 is consistent from device to device, the results shown in Figure 10 can be applied to any LT1568-based bandpass filter with excellent results. (Note that cascading two identical second order sections with these Q 's produces 4th order functions with respective Q_{EQUIV} 's of 4.65 and 9.3.)

Odd Order Lowpass Responses

The input resistor (R11) of the basic lowpass function shown Figure 2 can be split into two series resistors, R11

and R41 in Figure 11. This allows for an external capacitor (C_R) to be connected between the two resistors and ground, as shown in Figure 11. C_R transforms the basic 2nd order lowpass building block of the LT1568 into a 3rd order lowpass function.

The LT1568 can now be used as a dual 3rd order matched lowpass filter or as a single 5th or 6th order lowpass filter.

Unfortunately, the interaction of C_R with the remaining passive components of the circuit is quite complex, so an old fashioned paper design of the 3rd order lowpass function is cumbersome. The circuit of Figure 11 cannot be treated as a cascade of a single pole and a 2-pole filter.

Thankfully, the *LT1568 Design Guide* takes care of the otherwise intractable math. Given the values of the real pole and the center frequency and Q of the complex lowpass pole, the program calculates the values of R1, R2, R3, R4 and C_R that form a third order lowpass response.

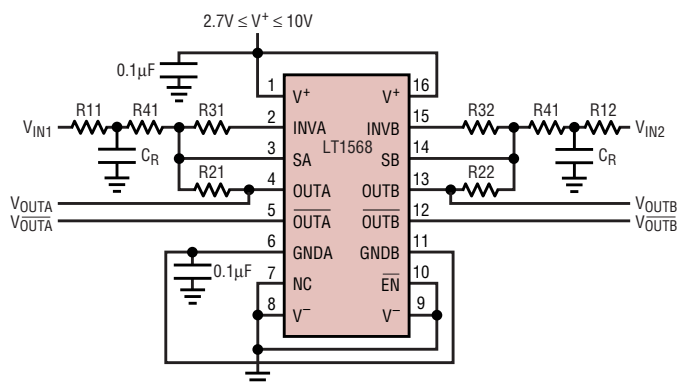


Figure 11. 3rd order lowpass function

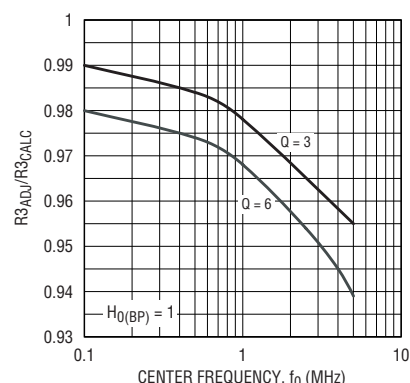


Figure 10. In the bandpass filter shown in Figure 7, the actual value for R3 required to achieve a specific center frequency deviates from the theoretically calculated value as the center frequency increases. Use this chart to determine the required value of R3 based on the desired center frequency.

Conclusion

The LT1568 offers the versatility and compactness demanded by the latest applications. It can be used as a simple dual matched 3rd order lowpass filter in I/Q applications, or it can be used as a sharp and accurate bandpass filter. The ability to add a notch in the filter transition band adds selectivity without adding complexity. Careful trimming of its active and passive components gives the LT1568 unprecedented predictability and repeatability, which can save significant costs in the volume production of high frequency devices.

Acknowledgements:

The author gratefully acknowledges the contributions of Philip Karantzalis and Tim Regan of Linear Technology's Signal Conditioning/Analog Filters Applications Group.

New Power for Ethernet—Detection and Classification (Part 3 of a 3-Part Series)

by Dave Dwelley

Introduction

The familiar RJ45 jack has been under the office desk now for better than a decade, and has served well as the data conduit to computers and devices with NICs (network interface cards). Now the IEEE 802.3af committee is extending the Ethernet standard to provide 48V DC power from these same RJ45 jacks, possibly relegating countless AC adaptors (wall warts) to the recycle bin.

This is a great leap forward, though it is not without pitfalls. For instance, what's to prevent legacy (non-ethernet-power-enabled) devices from burning up when a DC voltage that they were never designed to see appears on the wire?

The solution lies in the detection protocol that underlies 802.3af, which prevents a PSE (Power Sourcing Equipment) from applying power unless the device at the end of the wire is positively identified as an Ethernet-power-ready PD (Powered Device). This final article in a three-part series on Powered Ethernet covers detection and classification of PDs. Parts 1 and 2 covered PSEs and PDs, respectively, and are available at www.linear.com.

PD Detection

The fundamental defining characteristic of a PD is the $25k\Omega$ signature impedance it must present to the wire when probed with voltages below 10V (Figure 1). Legacy network connections typically are open circuits or have a 150Ω common-mode termination network between their terminals. $25k\Omega$ is chosen to be well away from both of these impedances, to minimize the chance of false detection.

Before a PSE is allowed to apply power to the line, it must check for this signature resistance with a power-limited probing source. Typically, a PSE will use one of three probing strategies: force a small current on the line and

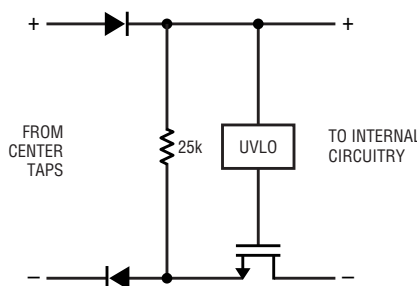


Figure 1. Simplified PD detection signature circuitry

measure the resulting voltage; force a small voltage on the line and measure the resulting current; or connect a voltage source to the line through a known resistance and calculate the result from the resistive divider.

“Linear Technology has several product families available that implement detection, classification, and power delivery for both PSE and PD systems.”

A PD need only present a valid signature when its terminal voltages are between 2.8V and 10V—a valid PD will pull a maximum of $550\mu A$ under these conditions. Under all circumstances, the PSE must limit the voltage while probing an open port to 30V or less, and limit the current while probing a short

to 5mA or less. To keep its internal circuitry from corrupting the signature, a PD typically includes a UVLO (Under Voltage Lock Out) circuit to disconnect everything but the signature circuitry from the line below 30V.

To be considered a valid signature, the PD must look like $25k\Omega \pm 5\%$ in parallel with 120nF or less of capacitance. The PSE, in turn, must accept a somewhat wider range of $19k\Omega$ to $26.5k\Omega$ to account for parasitic series and parallel resistances in the system. The PSE must reject anything below $15k\Omega$ or above $33k\Omega$, or anything with $>10\mu F$ across its terminals. Finally, if a PD decides for some reason it doesn't want power, it must make its signature resistance fall below $12k\Omega$ or rise above $45k\Omega$ to be sure it doesn't get detected. Figure 2 shows a diagram showing the resistance accept and reject bands.

PD Detection Details

The PD signature impedance is allowed to have a voltage offset of up to 1.9V (typically caused by up to two protection diodes in series), and a current offset of up to $10\mu A$ (typically caused by leakage in the PD). These terms complicate the PSE resistance measurement, since a single V-I point measurement will not account for these errors. As a result, the PSE is required to take at least two different V-I points, separated

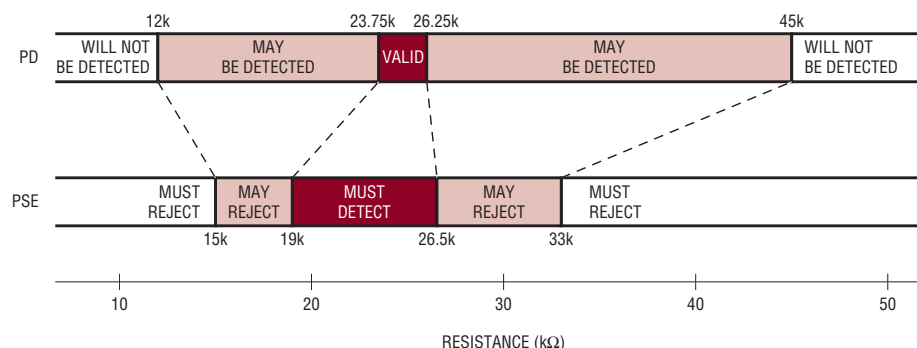


Figure 2. Detection resistance bands

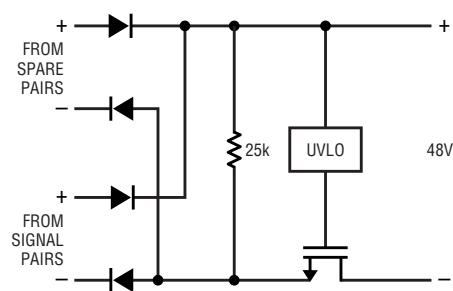


Figure 3. Diode-OR on power inputs

by at least 1V at the PD. It then must calculate the difference between the two points to find the true resistive slope, subtracting out voltage and current offsets.

CAT-5 cable is also known as UTP, for Unshielded Twisted Pair. The data pairs are twisted together, providing effective protection from interference, but the pair-to-pair common mode signal that the PSE-PD link works on are not twisted or shielded, and provide virtually no rejection of interfering signals. Since CAT-5 cable is typically run in ceilings, walls, and other spaces where AC wiring is also present, 50/60Hz noise can be significant. The PSE must be able to successfully detect the 25kΩ signature with this line noise present, which it typically does by integrating several detection points or timing the detection points to be synchronized with the line frequency. The entire detection process must take less than one second from the time the PSE is first connected to the port to the time power is applied, limiting the total integration time during detection to a few hundred milliseconds.

We know from Part 2 of this series (*Linear Technology V12N4*, December 2002, pg. 9) that a PD has two possible power inputs: the signal pairs and the spare pairs. A PD must be prepared to accept power from either pair, which means it must present the detection signature simultaneously at each input. However, the PD is not allowed to receive power at both inputs simultaneously, even in unusual wiring configurations where live PSE ports appear at both inputs at the same time. The simplest way for a PD to meet these requirements is to diode-OR the two inputs into a single signature resistor (Figure 3). This has the advantage of

automatically selecting power from the active input, as well as disabling the signature at the second input when the first is powered.

The only time this scheme causes trouble is when both inputs are detecting simultaneously. In this case, the diodes alternately select one and then the other input as the detection probing signals rise and fall. This can corrupt the signature at each input to the point where neither PSE detects successfully. To avoid this problem, the 802.3af spec requires that a PSE powering the spare pairs remain idle for at least two seconds after a failed detection (open circuit excepted) to allow the signal pair PSE to retry successfully.

PD Classification

Once the PSE has successfully detected a PD, it can optionally ask the PD how much power it will draw. This second classification signature provides a way for the PSE to estimate how much power it needs to allocate to a particular port, since not all PDs draw the full 12.95W allowed by 802.3af. If the PSE has a large enough power supply to provide full power to all ports simultaneously, it can skip the classification step. If (more commonly) it has limited power available, it must keep track of how many PDs are connected and what their power classification levels are, and stop accepting PDs when the power budget is exhausted.

The classification signature is checked by forcing voltage across, or current into, the PD to push it into the 15V-to-20V classification signature band. Since we have already established that there is a valid PD

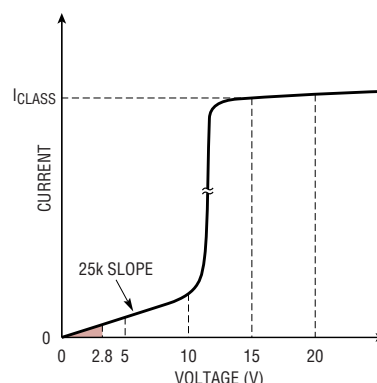


Figure 4. V-I characteristics of classification signature

connected, this additional voltage and current is unlikely to cause damage. In the classification signature band, the PD must behave like a constant current source, with a parallel impedance of 19kΩ or higher. The PSE measures this current and compares it to a set of fixed values that determine what class the PD falls into. Table 1 shows the available classes. The voltage source used during classification must be limited to 100mA to avoid damaging a malfunctioning PD, and it must not be connected for more than 75ms to keep PD power dissipation under control. Figure 4 shows how the PD current behaves as the system transitions from Detection mode to Classification mode.

Power Classes

PDs come in four classes, with a fifth reserved for future use. Classes 1 to 3 designate quarter, half, and full power PDs, respectively, as shown in Table 1. Class 0 is the default if a PD does not implement class signature circuitry; a 25kΩ signature resistor all by itself will land in the Class 0 current range.

continued on page 14

Table 1. IEEE 802.3af Power Classes

Class	PSE Minimum Output Power	PD Maximum Input Power	Nominal Classification Signature Current
0	15.4W	12.95W	<5mA
1	4.0W	3.84W	10.5mA
2	7.0W	6.49W	18.5mA
3	15.4W	12.95W	28mA
4	Reserved (Treat as Class 0)		40mA

16-, 14- and 12-Bit Octal Voltage-Output DACs Set New Standards for Performance and Packaging Density

by Victor P. Schrader

Introduction

The LTC2600, LTC2610 and LTC2620 are octal 16-, 14- and 12-bit, serial-input, 2.5V–5.5V single-supply, rail-to-rail voltage-output digital-to-analog converters. Each device packs an unprecedented number of features and unmatched performance into a tiny package. Here are just some of the impressive features and performance specifications:

- ❑ Eight buffered DACs in a 16-Lead Narrow (0.150") SSOP package—a new board-density benchmark.
- ❑ Guaranteed monotonic over temperature.
- ❑ Maximum offset error is $\pm 9\text{mV}$ over temperature, compared to $\pm 20\text{mV}$ to $\pm 60\text{mV}$ for competitive devices.
- ❑ Supply current is just $250\mu\text{A}$ per DAC at 3V. Individual-channel (or global) power down to $1\mu\text{A}$ (max).
- ❑ Ultralow DC Crosstalk between DACs ($<10\mu\text{V}$ change on the measured DAC for a 4V output step on a second DAC) for truly independent control.
- ❑ 0V to V_{REF} output range includes supply and ground.
- ❑ DAC outputs are guaranteed to source and sink 7.5mA minimum, even at $V_{\text{CC}} = 2.5\text{V}$ (15mA at 5V).
- ❑ Load Regulation error for the 16-bit LTC2600 is typically 0.3LSB per milliamp of load current. The best of any competitive device is 6.5LSB per milliamp—over 20 \times higher.
- ❑ The LTC2600, LTC2610 and LTC2620 settle to $\pm 1\text{LSB}$ in $10\mu\text{s}$, $9\mu\text{s}$ and $7\mu\text{s}$ respectively.
- ❑ Low-frequency noise is just $15\mu\text{V}$ peak-to-peak.
- ❑ Hardware $\overline{\text{CLR}}$ function resets all eight DAC outputs to zero scale, clears all registers and returns any powered-down channels to normal operation.
- ❑ Pin-compatible 12-, 14- and 16-bit family.

Figure 1 shows a simplified block diagram of these devices.

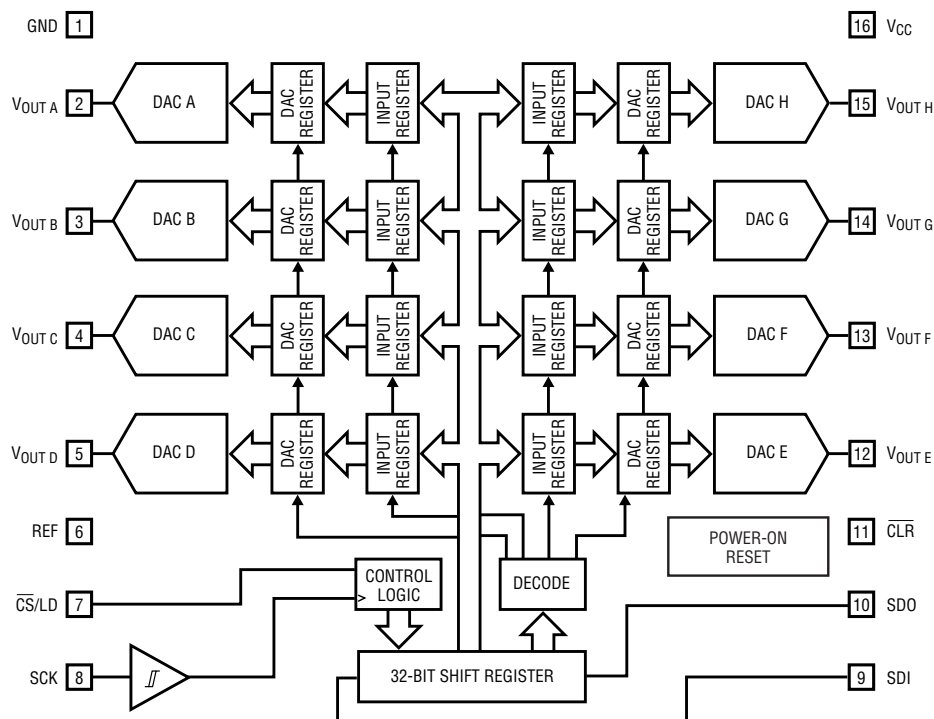


Figure 1. The LTC2600, LTC2610 and LTC2620 include eight DACs and eight high-performance buffer amplifiers. The 3-wire serial interface uses a 3-byte (24-bit) instruction word, with optional 1-byte extension, to control the devices in command-address-data format.

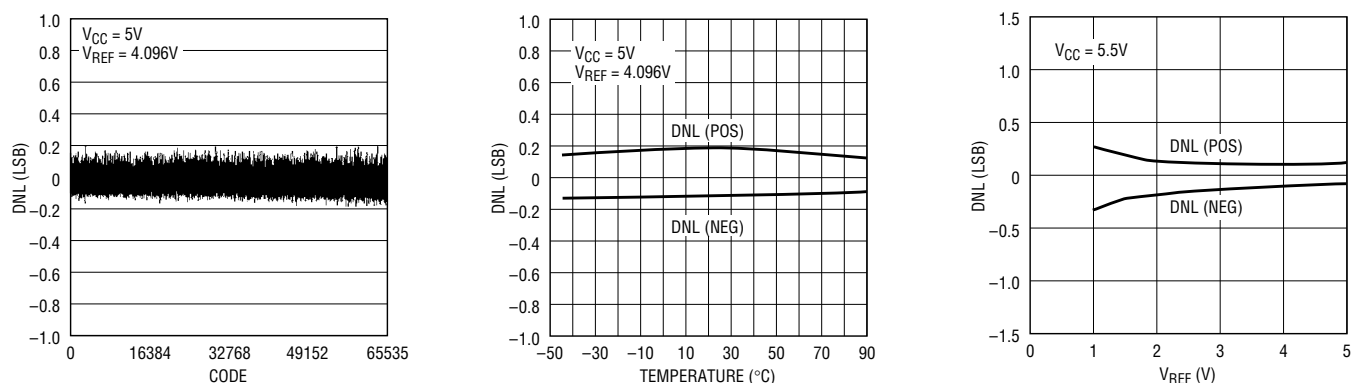


Figure 2. The excellent differential nonlinearity of the LTC2600 guarantees its monotonicity. Linear Technology's proprietary voltage interpolation architecture is used on all three devices for its efficiency and good DNL performance.

Performance

Patented Architecture Guarantees Monotonicity

The LTC2600, LTC2610 and LTC2620 use Linear Technology's proprietary, inherently monotonic voltage interpolation architecture.

This architecture provides compact size and excellent DNL. The DNL of the 16-bit LTC2600 is typically $\pm 0.2\text{LSB}$, while that of the 14-bit LTC2610 is less than $\pm 0.08\text{LSB}$. And the DNL of the 12-bit LTC2620 is typically less than $\pm 0.04\text{LSB}$. Moreover, linearity of the 16-bit LTC2600 is guaranteed starting at code 256, whereas its closest competitor starts at code 485, ignoring linearity below that code; and many others start their linearity measurements at code 896 or even higher.

Some competitors further foreshorten the transfer curve by exempting a band of the highest codes as well. The

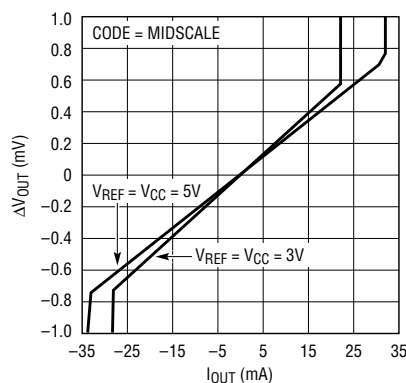


Figure 3. LTC2600 family load regulation. Output voltage is normalized to $I_{\text{OUT}} = 0\text{mA}$. Note source/sink symmetry, lack of a crossover bump at 0mA, clean transitions to current limiting, and the small amount of degradation from the 5V to the 3V case. Slopes (rise/run) show DC output impedances.

LTC2600, by contrast, is guaranteed to the upper code limit, i.e. code 65,535. The LTC2610 and LTC2620 are guaranteed to the same nominal voltage levels as the LTC2600, using the 14- and 12- bit equivalent codes.

Linearity is stable with respect to temperature and reference voltage. DNL vs temperature and DNL vs V_{REF} are shown in Figure 2. Changes in V_{CC} have at least an order of magnitude less effect on linearity than do changes in temperature or V_{REF} .

Ultralow DC Crosstalk: Change One Output without Having to Readjust the Others

The ultralow crosstalk of these parts ($<10\mu\text{V}$ change on the measured channel for a 4V output change on a second channel) means that they truly behave as independent DACs.

Compare this to the competition: A 2V step on the second channel changes the measured channel's output by $200\mu\text{V}$, or 40 times greater! Adjusting one output means having to go through all eight again.

Outstanding Output Compliance Minimizes Load Regulation Errors

Load regulation is an error source that is not usually given much attention in DACs. It can, however, easily dominate the total error of the converter.

The proprietary amplifier topology used in the LTC2600 series achieves very high gain (for good load regulation) and excellent stability (easily drives up to 1000pF capacitive load) together with improved low-voltage output drive: the DAC outputs are guaran-

teed to maintain load regulation with an output impedance of just 0.03Ω (0.15Ω max), even while sourcing or sinking 7.5mA on a 2.5V supply. A plot of the change in output voltage vs load current is shown in Figure 3. The drive capability is highly symmetrical, even at low supply voltages.

To illustrate the importance of load regulation, consider the voltage output error caused by changing the load resistance from $2\text{k}\Omega$ to $10\text{k}\Omega$. For any DAC in the LTC2600 family, at $V_{\text{CC}} = 5\text{V}$ and $V_{\text{REF}} = 4.096\text{V}$, the change in output will be:

$$(4.096\text{V}/2\text{k} - 4.096\text{V}/10\text{k}) \times 0.025\Omega = 41\mu\text{V}$$

—about two-thirds of a 16-bit LSB.

Compare that with the competition: the lowest DC output impedance of any competitor is 0.5Ω , and others are as high as 4.5Ω . While this doesn't sound like a lot, doing the calculation as above reveals that the induced error is between 13 and 118 LSBs (at 16 bits)—that is, $20\times$ to over $180\times$ the error of the LTC2600. This hidden source of error is significant.

Features

Easy-to-Use 3-wire Serial Interface Operates at Clock Rates Up To 50MHz

The LTC2600, LTC2610 and LTC2620 use a simple, versatile SPI™/QSPI™/MICROWIRE™-compatible interface that can be operated at clock rates of up to 50MHz . This allows all eight channels to be updated in just $4\mu\text{s}$,

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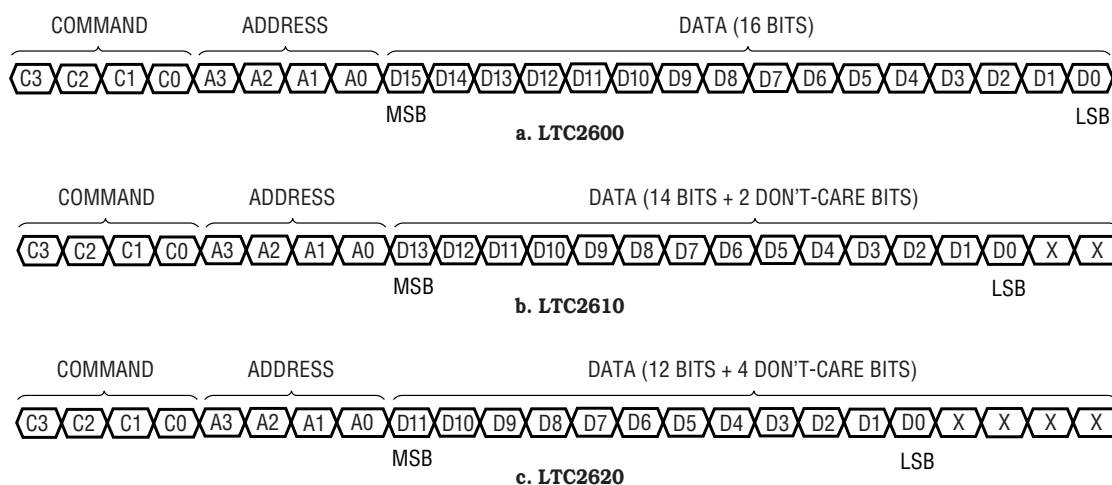


Figure 4. The LTC2600, LTC2610 and LTC2620 input words all use the same 4-bit Command and Address fields. The 16-bit Data fields are MSB-justified, with don't-care bits appended for the 14- and 12- bit parts.

that is, at a 250kHz rate. The devices use a double-buffered input architecture, and can easily be programmed to update individually or simultaneously with no penalty in update rate.

Control Additional DACs with No Additional Control Lines

Cascading additional serial devices by connecting the provided SDO pin to the SDI (Serial Data Input) pin of successive downstream devices saves even more board area, and conserves microprocessor outputs as well. Cascading, or daisy-chain operation, allows straightforward control of multiple serial devices with only three control lines.

The implementation of this feature is particularly attractive for optoisolator applications. Optoisolators are sometimes used when the DAC ground and microprocessor ground must be separated. But when used to drive a

daisy chain, the slow digital edges typical of optos, combined with trigger-voltage variations between serial devices, can result in shift-register timing problems and consequent data errors.

This problem is commonly addressed by adding an external Schmitt trigger to increase the clock signal edge rate. (The external Schmitt is needed even when the DACs have individual internal Schmitt inputs.) The LTC2600 family, however, has eliminated the need for the external Schmitt. Since the SDO output signal changes states on the nonactive (falling) clock edge, slow edge rates cannot cause data errors.

Flexible Input Word Allows Single-Channel or Global Software Control

These parts use a 24-bit instruction word composed of a 4-bit command field, a 4-bit address field, and a 16-bit

data word. Figure 4 shows instruction words for each of the three devices.

The command and address code definitions are shown in Tables 1 and 2. The 4-bit command code is used to specify single actions such as write, update or power down, along with a selection of important multiple actions. It is possible, for example, to write to one channel and update all eight channels in one instruction cycle, thus saving one instruction cycle in simultaneous-update routines.

The 4-bit address code is used to specify the channel to which the command will be applied. Any single DAC may be chosen. There is also an address for all eight channels, which is useful for initialization and error-recovery routines.

Table 2. Address definitions

Address(n)				DAC
A3	A2	A1	A0	
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	1	1	1	All DACs

Table 1. Command definitions. "n" represents the DAC that is to be acted upon. When any DAC output is updated, that channel also exits power down and returns to normal mode.

Command				Action
C3	C2	C1	C0	
0	0	0	0	Write to Input Register n
0	0	0	1	Update (Power-Up) DAC Register n
0	0	1	0	Write to Input Register n, Update (Power Up) All
0	0	1	1	Write to and Update (Power Up) n
0	1	0	0	Power Down n
1	1	1	1	No Operation

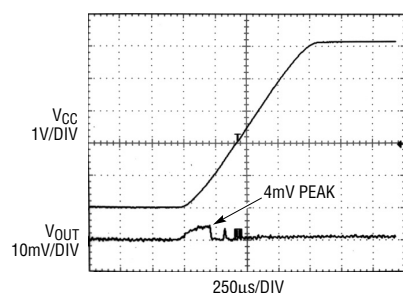


Figure 5. Power-on reset glitch. Note vertical scales. If V_{CC} is ramped 0V–5V in 1ms or more, then the DAC outputs stay below 10mV during startup.

All three parts use the same 16-bit data word. The data is MSB-justified, with don't-care bits added after the LSB for the 14- and 12- bit parts.

Power-On Reset Holds Outputs to Below 10mV During Startup

The LTC2600, LTC2610 and LTC2620 clear their outputs to zero scale, reset all internal registers and disable power-down mode when power is first applied, making system initialization consistent and repeatable. These devices contain circuitry that holds the DAC outputs to below 10mV during startup, an important feature in systems that drive RF amplifiers or transducers and need to stay off at startup. Figure 5 shows one of

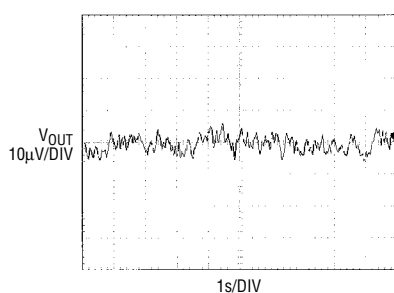


Figure 6. Output voltage noise, 0.1Hz to 10Hz. Measurement shows a typical value of 15µV peak-to-peak.

the DAC outputs as the LTC2600 is powered up.

Power-Down to 1µA Max—Any Combination of DACs


In power down mode, the buffer amplifiers, bias currents and reference inputs are all disabled, and draw essentially zero current. The DAC outputs are set in a high-impedance state, and the output pins are passively pulled to ground through individual 90kΩ resistors. Register contents are not disturbed during power-down.

Any channel or combination of channels may be placed in power down mode, reducing the total device supply-plus-reference current by approximately $\frac{1}{8}$ for each DAC turned

off. When all eight are off, supply current is typically 350nA at 5V (100nA at 3V). All eight DACs may be turned off with one instruction by using the All-DACs address.

Table 1 shows that DACs can be returned to normal operation by executing any command which includes a DAC update. The selected DAC is powered up and its voltage output is updated to the value stored in its input register. The time required to return to normal operation from power down mode is typically 5µs.

Conclusion

The LTC2600, LTC2610 and LTC2620 are the only available octal 16-, 14- and 12-bit DACs in Narrow (0.150 Inch) SSOP-16 packages. Yet in spite of their amazing density, these DACs actually raise the bar on performance, offering excellent 16-bit DNL, high update rate, exceptionally low cross-talk, outstanding output compliance and very low power dissipation. This combination allows the system designer to use board space efficiently and minimize production time spent in adjustment routines, while at the same time achieving first-rate system performance. 

Powered Ethernet, continued from page 10


The PSE interprets Class 0 as Class Unknown (which is usually treated as Class 3). Class 0 is typically reserved for extremely simple or low cost PDs where including classification circuitry is a burden. Class 4 is reserved for future use; a PSE that discovers a Class 4 PD should treat it as a Class 0.

The PD should place itself in the class that includes its peak current draw, even if the typical current draw is well below the class limits. For example, if a phone draws 2W when sitting idle but 8W when the ringer is ringing, it must class itself as a Class 3 (or Class 0) device even though typical power consumption is in the Class 1 range. A PD cannot change classes on the fly, since classification is only run once, right before power is applied.

Putting It All Together

Once a PSE has successfully detected and classified a PD, it then makes the decision whether to power it on. If the available power in the PSE is adequate to power the PD, the PSE turns on the power to the PD and begins monitoring the port for the Power Maintenance Signature, as described in Part 1 of this series (*Linear Technology V12N3*, December 2002, pg. 9). Once power is applied, the detection circuitry should be disabled, since the PD UVLO switch is now closed and the input impedance of the PD power supply circuitry typically swamps the 25kΩ signature impedance.

The PSE now has the whole picture: the detection sequence tells it that there is a real PD attached to the port; the classification routine tells it how much power that PD will draw so it can allocate its power supply resources

accordingly; and the Power Maintenance signature tells it that the PD is still present and operating normally. The PD, in turn, has a straightforward way to communicate to the PSE what it is, how much power it wants, and whether or not it wants that power to keep flowing. All of this goes on without affecting the data stream in any way. This allows both ends of the system to pick up or drop off power without affecting ongoing data transfers (assuming, of course, that the PD has an alternate power source). It also allows valid PSE and PD devices to be built with no data communications hardware at all—a significant cost savings for some applications. Most importantly, the detection protocol minimizes the chance of damaging a legacy Ethernet device, thus maintaining backward compatibility. 

Introduction

edge blanking and adaptive maximum duty cycle clamping. Programming is remarkably simple, allowing converter solutions to be easily optimized for high performance, low cost and small component size.

For instance, programmable adaptive maximum duty cycle clamping limits the transformer reset voltage under load and line transients, which allows the use of the smallest transformers, MOSFETs and output rectifiers for transformer-based



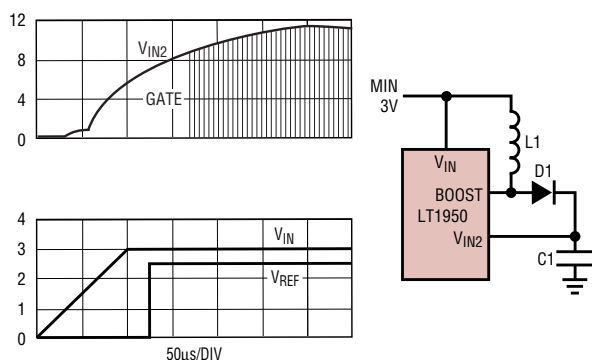


Figure 2. Low V_{IN} operation

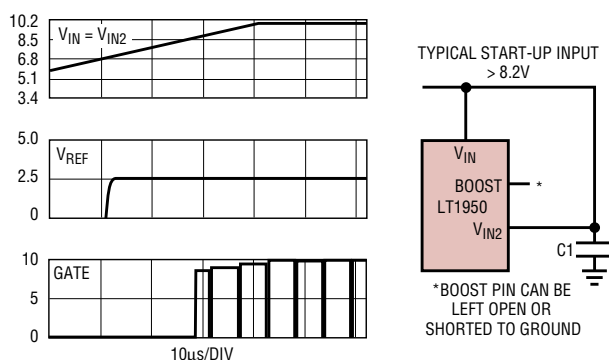


Figure 3. $V_{IN} = V_{IN2}$ operation

designs. This feature allows LT1950-based forward converters to use a single MOSFET topology with MOSFET utilization far beyond 50% duty cycle operation.

An LT1950-based forward converter can be used to replace power modules at a much lower cost with superior efficiency and transient response performance. The LT1950 supports both isolated and nonisolated outputs. Two forward converter applications are covered in this article (a synchronous 3.3V 20A isolated output and a non-synchronous 24V 5A isolated output). The LT1950 is available in a small 16-pin SSOP package.

Part Description

The LT1950 is a PWM controller with 3V to 25V input range. The converter uses a current mode topology, providing a fast transient response capability with very simple frequency compensation.

Figure 1 shows the key functions of the LT1950 in a block diagram. A $\pm 2\%$ accurate 1.23V reference at the error amplifier positive input allows

precision programming of the output voltage. A 2.5V reference output at the V_{REF} pin is capable of delivering up to 2.5mA externally. The SHDN pin has an accurate 1.32V threshold with current hysteresis, allowing precise programming of undervoltage lockout and shutdown.

The LT1950 switching frequency can be programmed between 100kHz and 500kHz using a single resistor from the R_{OSC} pin to ground. In addition, the part can be synchronized up to $1.5\times$ the programmed frequency. For slope compensation requirements, a default level is included inside the LT1950 with the SLOPE pin open circuit. To increase the slope compensation by as much as $3\times$, a resistor can be inserted between the SLOPE pin and V_{REF} pin. Conventional current mode controllers, without the ability to adjust slope compensation, limit the minimum usable inductance in continuous mode and lose the ability to optimize performance for various layouts. The LT1950 allows a larger range of inductance and the ability to

tailor slope compensation for optimal performance.

The LT1950 controls an external MOSFET switch at the GATE pin. Peak current is monitored via a power resistor in the source of the switch. The sense point is connected to the I_{SENSE} pin. The current sense threshold at the I_{SENSE} pin, proportional to the error amplifier output (COMP pin) voltage, controls the MOSFET peak switch current and provides cycle-by-cycle current limiting. A maximum I_{SENSE} threshold of 86mV (at 80% duty cycle) keeps power losses low. To avoid false tripping of the I_{SENSE} threshold due to noise generated during MOSFET turn on the LT1950 has built-in leading edge blanking. The blanking duration can be further extended by adding resistance from the BLANK pin to ground. The LT1950 has a 125mV override threshold at the I_{SENSE} pin to detect fault conditions that cause excessive MOSFET currents. In such cases the LT1950 defeats blanking and switches the external MOSFET off immediately.

The LT1950 can be configured to operate in low V_{IN} mode (Figure 2) or in $V_{IN} = V_{IN2}$ mode (Figure 3). Low V_{IN} mode allows input voltages as low as 3V, while still supplying 10V gate drive to the GATE pin. The main supply, V_{IN} , can operate as low as 3V. The regulated 2.5V V_{REF} , generated from V_{IN} , supplies the majority of the LT1950 control circuitry. The second supply, V_{IN2} , provides power for the output driver at the GATE pin. V_{IN2} can be generated from V_{IN} using an internal

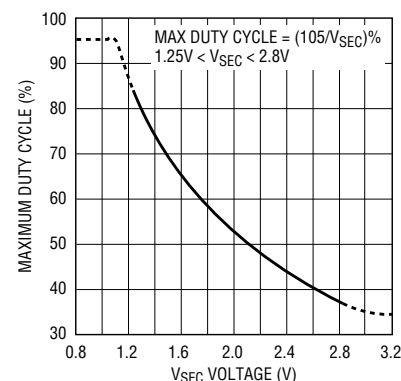


Figure 4. Programming the volt-second clamp using the V_{SEC} pin

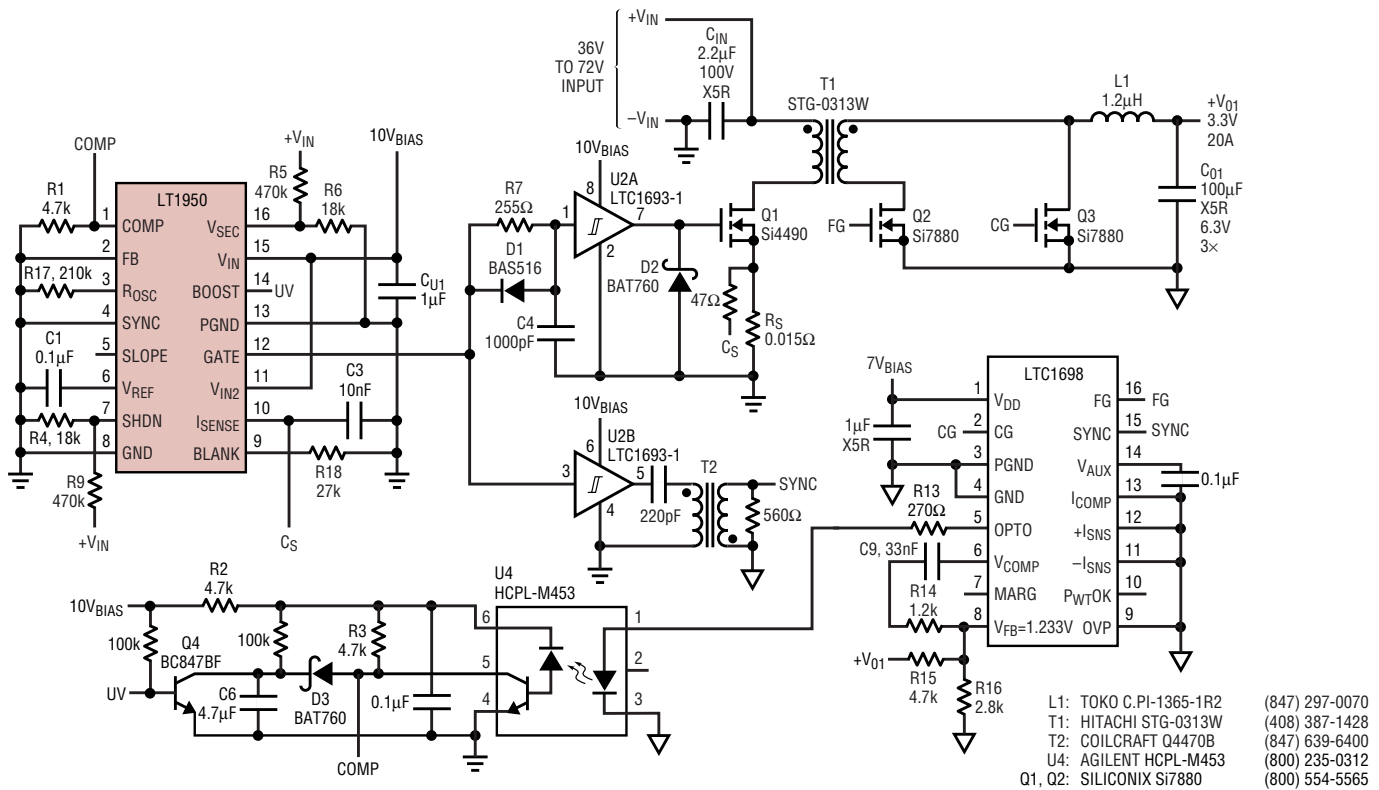


Figure 5. 36V to 72V input to 3.3V at 20A output synchronous forward converter

boost regulator at the BOOST pin (Figures 1 and 2).

The internal switcher, with fixed current limit and off time, regulates V_{IN2} between 10V and 11V. Hysteretic operation disables the switcher at 11V and re-enables it at 10V. Low V_{IN} operation is beneficial in SEPIC applications where input voltages will be above and below the output of the converter. At low input voltages, conventional PWM controllers can only drive logic level MOSFETs which can limit the maximum input and output

voltages allowable for the SEPIC application. The LT1950's ability to provide a 10V gate drive from a 3V input allows the use of standard MOSFETs with enough drive to achieve low $R_{DS(ON)}$ for maximum efficiency.

If low V_{IN} operation is not required V_{IN2} can be connected to V_{IN} with the BOOST pin open or shorted to ground. Minimum operational input voltage will be approximately 8V, since V_{IN2} must exceed the undervoltage lockout threshold to allow GATE switching.

Adaptive Maximum Duty Cycle Clamp

The LT1950 has an adaptive maximum duty cycle clamp which automatically reduces maximum switch duty cycle with increased system input voltage. This feature is critical in transformer-based designs because it controls the transformer volt-second product during switch off time ensuring proper transformer reset during each switch cycle and minimizing the reset voltage across the primary side switch. The maximum switch duty cycle at low system input voltage is initially set by a resistor divider from the system input

voltage to the V_{SEC} pin. Any increase in the system input voltage increases the V_{SEC} voltage causing a subsequent decrease in maximum switch duty cycle (as shown in Figure 4). Many forward converters have fixed maximum duty cycle clamps resulting in high reset voltages during load and line transients. Such converters attempt to solve the problem by using more robust power components leading to larger, more costly and less reliable solutions.

High Efficiency, Isolated 3.3V 20A Output, Synchronous Forward Converter

Figure 5 illustrates a synchronous forward converter that provides a highly efficient, 3.3V, 20A, isolated output from a 48V input. The single primary MOSFET topology keeps the solution simple.

The LT1950 adaptive maximum duty cycle clamp allows the power components in this solution to be operated at up to 75% duty cycle. This feature allows 50% better MOSFET, transformer and output rectifier utilization compared to typical forward

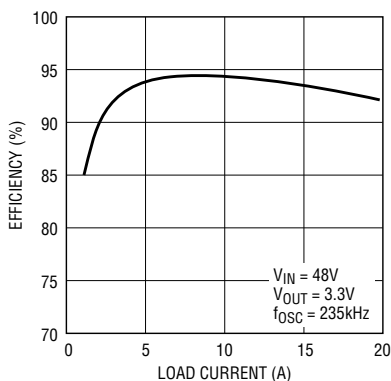


Figure 6. Efficiency vs load current for the LT1950-based synchronous forward converter shown in Figure 5

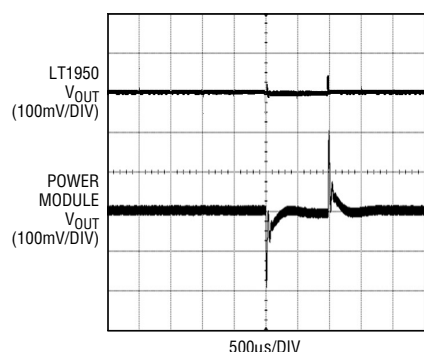


Figure 7. Comparison of the transient response for Figure 5's circuit and a competitor's power module (1µs load steps 0A to 3.3A)

converters which limit operation to 50% duty cycle.

The synchronous output rectifier MOSFETs are driven by the LT1698 which also serves as an error amplifier and opto coupler driver.

This LT1950-based converter offers several advantages over power module solutions including a significant cost savings. Peak efficiencies of 94% (as shown in Figure 6) and ultrafast transient response (Figure 7) are far superior to power module


solutions. In addition, the circuit uses only ceramic capacitors for improved reliability and low output ripple voltage. The advantage of system board thermal conduction means lower component temperature rise and higher efficiencies compared to power module solutions. The 7mm height allows dense packaging and higher currents are achievable through simple scaling of the power components.

High Efficiency, Isolated 24V 5A Output, Nonsynchronous Forward Converter

Figure 8 illustrates a nonsynchronous forward converter that provides a highly efficient, 24V 5A isolated output from a 48V input. This converter uses a single MOSFET topology and the LT1950's adaptive maximum duty cycle clamp to make a simple and highly optimized solution. Figure 9 shows that peak efficiencies of 92.8% are possible. The transformer and inductor are standard components. This quarter-brick-sized DC/DC converter (2.3" by 1.45") delivers over 125W and

is only 0.4" high. The 24V converter can be used as a front end (isolating) converter in telecom systems with multiple outputs. Once the isolation boundary is established by the 24V converter, buck converters such as LTC1778, LTC1628, LTC1735 and LTC1629 can be used to generate low voltage (1.5V, 1.8V, 2.5V and 3.3V), high current core voltages.

Conclusion

The LT1950 is superior to conventional PWM controllers because of its many simple-to-program features and minimal number of required external components. Its programmable switching frequency, slope compensation and leading edge blanking allow optimized solutions for a wide range of inductor values, MOSFET types and board layouts. The LT1950's programmable adaptive maximum duty cycle clamp allows LT1950-based forward converters to use a single MOSFET topology with the smallest component size, lowest cost and highest performance possible. The LT1950-based forward converter is an excellent replacement for power modules, due to its superior efficiency, transient response, lower cost and better thermal performance. 

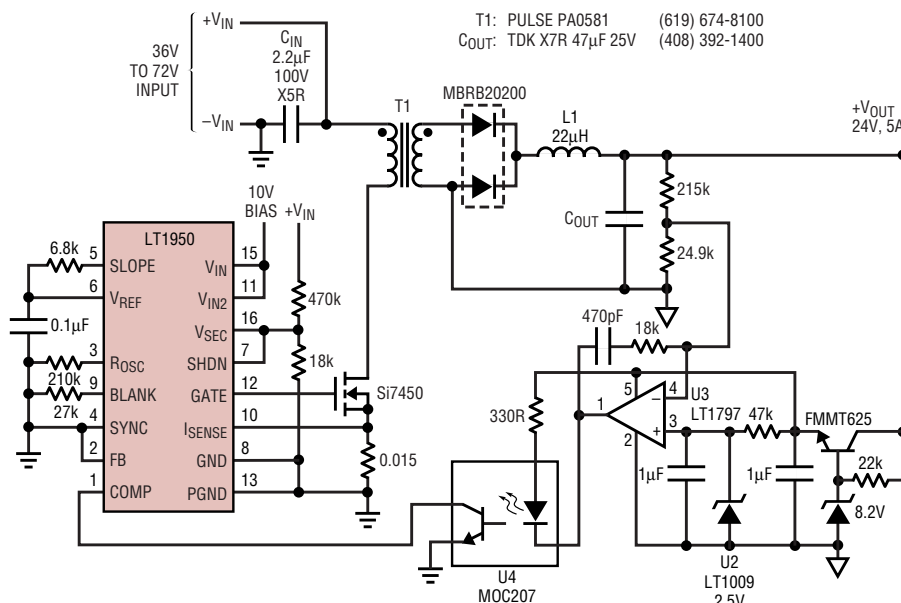


Figure 8. 36V to 72V input to 24V at 5A output nonsynchronous forward converter

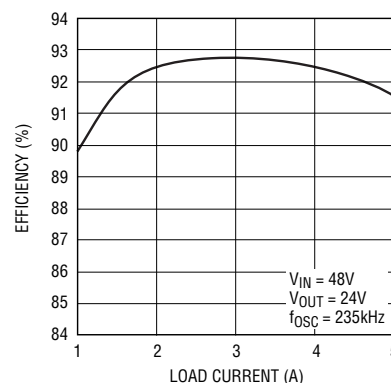


Figure 9. Efficiency vs load current for the LT1950-based nonsynchronous forward converter shown in Figure 8

Micropower Linear Regulator Provides Simple Solution for Low Power Circuits in High Voltage Industrial, Automotive or Telecom Applications

by Todd Owen

Introduction

Industrial, automotive, and telecom systems create harsh, unforgiving environments that demand robust electronics systems. High voltage transients are unpredictable and ride on fairly high 12V–48V rails. Under these challenging conditions, switching power supplies provide robust local low voltage/high current power from the high voltage rails, but switching power supplies are overly complex for the low power keep-alive circuits that typically run only a few milliamps of current. There are many such low current applications in automotive, industrial and telecom systems, such as monitoring circuitry, security systems, and other always-on circuits. For most of these applications, a wide input range linear regulator is a relatively simple and inexpensive solution. The LT3010 linear regulator fits the bill with its wide input range and myriad protection features.

The LT3010 is a high voltage, micropower, low dropout linear regulator in a thermally enhanced 8-lead MSOP package. It can provide up to 50mA of output current from input supplies ranging from 3V to 80V. Dropout voltage on the LT3010 is only 300mV when delivering up to 50mA of output current. The LT3010 operates on only 30 μ A of quiescent current. It can be put into a low power shutdown state

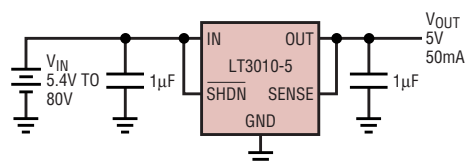


Figure 1. LT3010 typical application

by pulling the $\overline{\text{SHDN}}$ pin low, bringing quiescent current down to 1 μ A. For standard operation, the $\overline{\text{SHDN}}$ pin can be pulled as high as 80V (regardless of input voltage) or left open circuit.

Figure 1 shows how easy it is to use the LT3010 to design a low current supply running from a high voltage rail. The only external components required are input and output bypass capacitors, and the input bypass is not necessary if the device is located within 6" of the main supply bypass capacitor. Internal frequency compensation on the LT3010 stabilizes the output for a wide range of capacitors. A minimum of 1 μ F of output capacitance is required for stability, and almost any type of output capacitor can be used. Even small ceramic capacitors with low ESR can be used without the addition of series resistance as is common with other regulators.

Protection features abound in the LT3010, safeguarding itself and sensitive load circuits. Should the input voltage become reversed, whether from a backwards battery or fault on the line, no current flows in the LT3010

and no negative voltage is seen at the load. No external protection diodes are necessary when using the LT3010. With a reverse voltage from output to input, the LT3010 acts as though it has a diode in series with its output to prevent reverse current flow. For dual-supply applications where the regulator load is returned to a negative supply, the output can be pulled below ground by several volts while still allowing the device to start and operate. The LT3010 includes protection features found standard on linear regulators such as current and thermal limiting.

The Ideal Solution for Harsh Environments

The LT3010 provides an optimum solution for harsh conditions. Long wire runs for high voltage rails can have transient voltage spikes as loads are switched on and off. Most automotive applications run from a 12V rail, but newer cars are transitioning to 42V systems that can produce transients greater than 60V. Telecom applications typically run from a 48V supply that can go as high as 72V. Industrial applications can span even wider input voltage ranges. All of these applications can see transient input spikes more than 50% above nominal. There are other fault conditions on input and output terminals such as reverse input or reverse voltages from input to output that must also be considered.

Always-On Automotive Application

Figure 2 shows a typical automotive application for the LT3010. This is an always-on circuit that runs even when the ignition is off, common in modern cars that have many subsystems that remain powered when the engine is

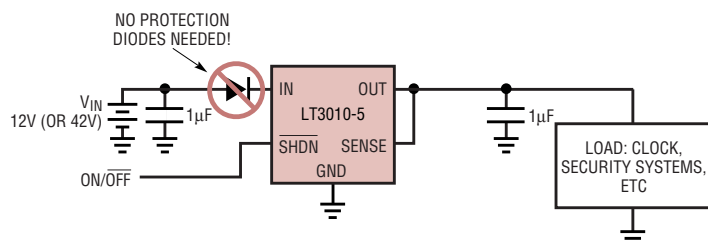


Figure 2. Typical automotive application

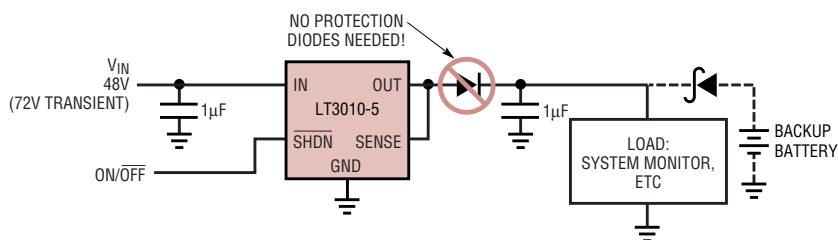


Figure 3. Typical telecom application

not running. To reduce battery drain, the total current from all subsystems must be in the range of milliamps. The micropower quiescent current of the LT3010 helps save the battery, and the LT3010 can be placed into the shut-down state whenever the section of circuitry it is driving is not needed.

The small size of the LT3010 and its associated external components keep board space, height, and weight to a minimum.

Power connections to the LT3010 can come directly from the battery or alternator, where input transients coming from a load dump can be stood off without concern over damaging the regulator or the load. Reversed battery connections are no problem because the LT3010 prevents reverse currents from being seen at the output of the regulator, thus protecting sensitive load circuits.

The imminent change from 12V to 42V systems is an important design consideration. The LT3010 simplifies the transition, reducing design time and costs, because no re-design is necessary when it is used—its 3V to 80V input voltage range is sufficient for both types of systems.

Robust Telecom Application

A typical telecom application using the LT3010 is shown in Figure 3. A 48V rail powers a keep-alive circuit for monitoring or other purposes. Low quiescent current is important here to reduce battery drain. A battery back-up keeps the output alive when a fault on the input occurs. Should a fault on the 48V rail occur, the battery back-up takes over. The internal protection of the LT3010 prevents current flow from the output back to the input, removing the need for protection diodes.

Size is a concern for all components, depending upon application constraints. Applications may require height clearances or board area constraints. The small MSOP package has a maximum height of 1.1mm. The ability to operate with small ceramic capacitors limits board area. The exposed pad of the package provides excellent thermal properties in tight spaces. The 48V input rail in telecom applications can have transient voltages as high as 75V. The LT3010 can handle these transients without the need for pre-regulation or protection devices. Lastly, the thermally enhanced 8-lead MSOP package eases thermal design. The LT3010 cannot run at maximum current and input voltage all the time, but the brief transients seen in this application pose no problem from a thermal standpoint.

Thermal Considerations

Operating at high input voltages requires appropriate thermal planning. There can be significant power losses at relatively low currents. The exposed pad 8-lead MSOP package significantly improves heat transfer from the die out of the package to the circuit board. This lowers the overall junction-to-ambient thermal resistance for a typical board to 30°C/W–40°C/W, down from 180°C/W–200°C/W for a standard 8-lead MSOP or 110°C/W–130°C/W for a MSOP package with a fused leadframe.

To illustrate some of the thermal issues, take an application for powering a local data collection unit from a 48V rail that will regularly experience transient spikes to 72V. The operating current of the unit is 5mA quiescent at 5V, though it increases to 50mA as the unit is polled to transmit its data. This is a typical application for

the LT3010, where low quiescent load current and input voltage occasionally give way to higher transient loads and supply spikes.

With 72V (transient spike voltage) in, 5V out, and a 50mA load current, power dissipation is $(72 - 5)V \cdot 50mA = 3.4W$. With a best-case layout, thermal resistance can be 30°C/W, leading to a temperature rise at the power-dissipating junction of over 100°C—too hot to operate the device at ambient temperatures above room temperature. Standard thermal calculations operating with worst-case input voltage and load current show excessive temperature rise and limited circuit utility.

This calculation is highly inaccurate because it requires a convergence of transient events, namely a spiking input voltage and the occasional rise in load current, events that account for only a tiny percentage of the operational life of the circuit. The average input voltage is from a 48V rail that occasionally spikes to 72V. Load current is a static 5mA load that only occasionally steps to the full 50mA when the unit is polled. In the end, typical conditions result in an average power dissipation that is less than 10% of the maximum power dissipation. This amounts to less than 10°C rise above ambient compared to the 100°C rise calculated above.

While many would breathe a sigh of relief and walk away from the calculations once they see this lower average dissipation, the transient power cannot be ignored. Attention must be paid to what the transient power levels are,

continued on page 38

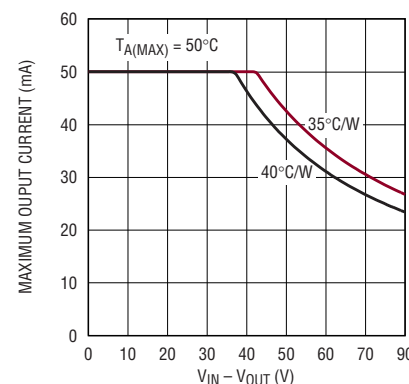


Figure 4. Maximum output current

Micropower Dual Comparators in SOT-23 Include 400mV Internal Reference

by Jon Munson and Dan Serbanescu

Introduction

The LT6700-1, LT6700-2 and LT6700-3 are micropower, dual comparators that include an internal 400mV reference and are optimized for core (V_{CC}) operation on single supply voltages from 1.4 to 18V. This family offers Over-The-Top[®] capability for both the inputs and outputs from V_{EE} to 18V above V_{EE} , regardless of V_{CC} . These parts keep the pin-count to a minimum by internally committing one of the inputs of each comparator section to the production trimmed 400mV reference—different dash-number designations denote different comparator connections. These comparators all include a built-in input hysteresis of 6.5mV nominal, a feature that simplifies design by minimizing external component count. The comparator outputs are open-collector types, allowing them to form convenient wired-AND logical connections or individually drive up to 40mA loads.

Figure 1 shows a comparison of these three devices. The LT6700-1 offers a configuration with both an inverting and noninverting input available, providing a means of forming

Table 1. LT6700-1, LT6700-2 and LT6700-3 Key Performance Characteristics

Parameter	Value (typical)
Rising-Input Threshold	400mV
Hysteresis	6.5mV
Input Bias Current	2nA
Output Low (On-State) Voltage	60 mV (3mA load, $V_{CC} = 1.6V$)
Output Leakage Current	1nA
Propagation Delay	25 μ s
Supply Quiescent Current	6 μ A

simple window-detection functions. The LT6700-2 offers the inverting inputs to both comparators, useful for oscillation or timing functions. The LT6700-3 provides both of the non-inverting inputs, particularly useful when increased hysteresis is implemented.

The LT6700-1, LT6700-2 and LT6700-3 are available in the popular SOT-23 6-lead package and typically draw a micropower supply current of 6 μ A. Additionally, the low supply-voltage capability of these devices makes

them ideal for use in portable battery-powered products.

Performance

Table 1 shows the key performance parameters of the LT6700-1, LT6700-2 and LT6700-3.

The internal reference of each part is trimmed in production such that for rising inputs, regardless of input polarity, the decision threshold is 400mV, which remains accurate to $\pm 2\%$ over the -40°C to $+85^{\circ}\text{C}$ temperature range. Figure 2 shows a distribution and variation of rising threshold versus

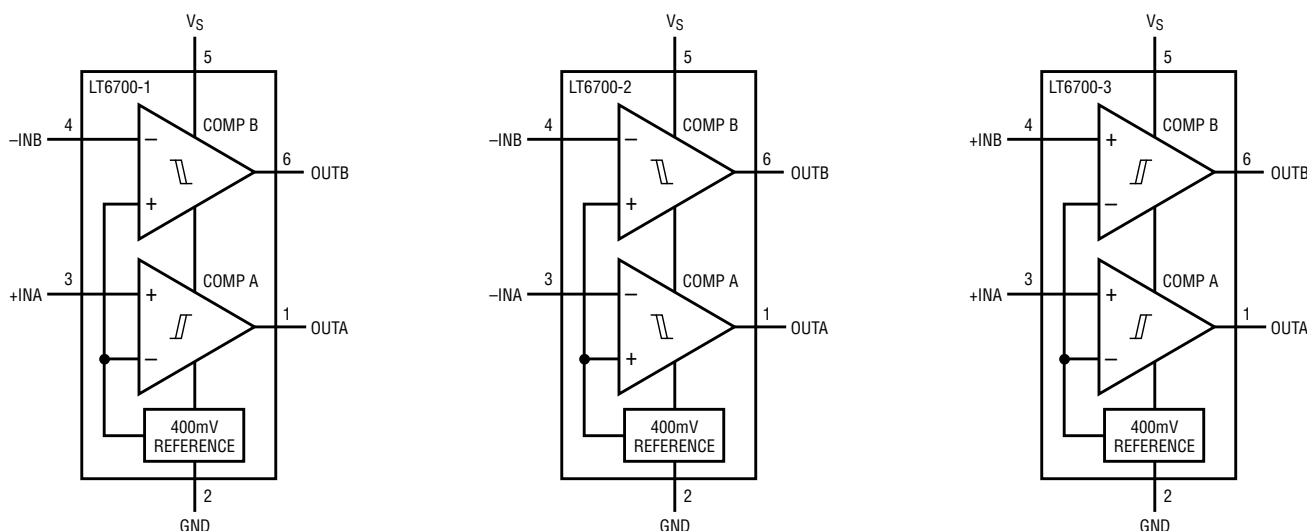


Figure 1. LT6700-1, LT6700-2 and LT6700-3 pin functions

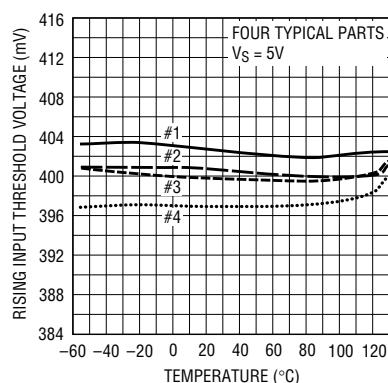


Figure 2. Rising input threshold voltage vs temperature

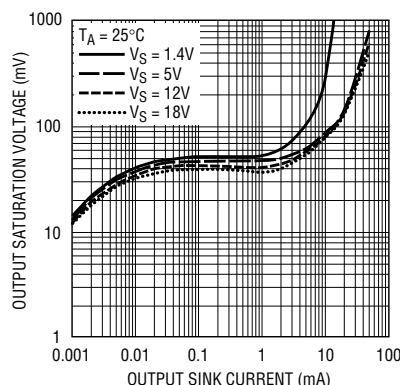


Figure 3. Output saturation voltage vs output sink current

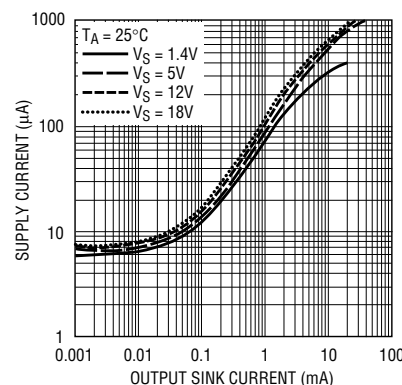


Figure 4. Supply current vs output sink current

temperature for a sampling of several different parts. The falling input threshold is typically 6.5mV below the rising input threshold (or about 393mV), established by the internal hysteresis mechanism. Hysteresis is provided to insure clean decision-making in the presence of noise at the inputs, and to reject supply-rail noise that might be induced by state-change load transients.

Even though it is implemented in a low power bipolar technology, the LT6700-1, LT6700-2 and LT6700-3 input bias currents are as low as the leakage found in many CMOS processes, less than 15nA worst-case (2nA typical). A special output design afforded by the bipolar technology avoids the usual CMOS constant on-resistance effect, keeping output voltages low even under heavy loads. Figure 3 shows how the output on-state voltage varies with load, where it can be seen that with V_S greater than 5V, a TTL low (0.4V) is achieved while sinking 40mA. In the off-state, the outputs become essentially open circuit and can handle up to 18V,

leaking just 1nA typically, even during Over-The-Top operation.

The quiescent supply current is typically 6μA for light output loading, as seen in Figure 4. Under conditions of heavy loading, additional supply current flows to provide the required output-transistor drive, reaching as high as about 10% of the output current.

Some Interesting Design Solutions

Flexible Window Comparator

The LT6700-1 is well suited to monitoring power supply voltages, as it can be readily configured to produce a window-function. Figure 5 shows a circuit for generating a logical 0 whenever V_{CC} is outside a normal operating range. In this example, when V_{CC} is near the normal operating voltage of 3.3V, neither output is low. The output is a logical 1 by virtue of the wire-AND connection of the outputs. If V_{CC} falls below about 3.1V, the noninverting comparator section pulls the output low, or if V_{CC} rises above about 3.4V, the inverting comparator section trips

and pulls the output low. The low supply-voltage capability of the LT6700 assures that the monitor functions correctly, even during serious under-voltage conditions of the supply.

Battery-Low Alarm with Flashing-LED Annunciator

Figure 6 shows a circuit that uses the LT6700-2 to sense a low charge state for Li-Ion rechargeable battery packs in portable products. The upper comparator section senses whether the battery is undervoltage, producing a logical 0 while the battery remains above about 3.5V. The low output of the upper comparator also prevents lighting of the white LED by forcing the condition of the lower comparator section to an off state.

When the battery voltage drops and the upper comparator signals an alarm condition, the LED is lit until it discharges the 22μF capacitor, which drops the input to the lower comparator after the time-delay of an RC network (1MΩ, 1μF, 154kΩ). The LED shuts off and remains off until a 3.0V charge develops on the 22μF capacitor, which raises the lower comparator input above threshold again. The cycle continues—it's a flashing LED.

Since the charge-rate of the 22μF capacitor depends on the supply voltage, the interval between flashes extends as the battery continues to discharge, thus indicating the relative state of discharge. At 3.0V the circuit completely ceases flashing the LED and settles into a minimum power-drain condition. The average current draw of the circuit is quite low (<50μA) even

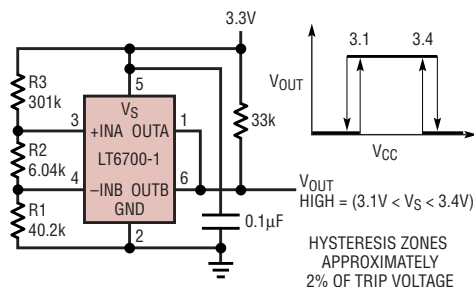


Figure 5. Power supply status-monitor

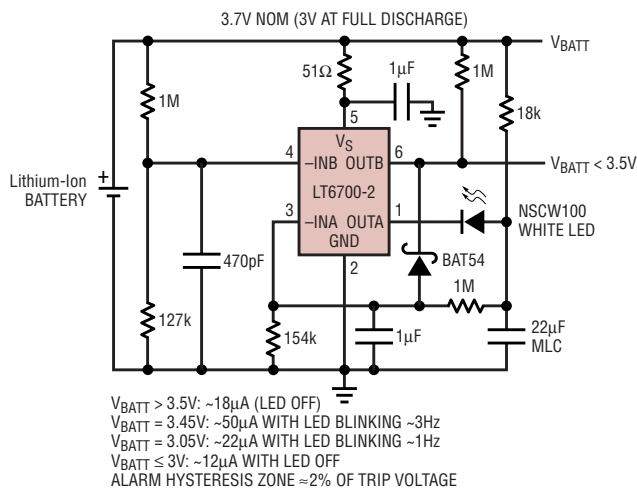


Figure 6. Micropower "battery-low" LED flasher and alarm

while the LED is flashing due to the small duty-factor and high efficiency of the LED. In this circuit, $I_{LED(PEAK)}$ is established at about 5mA by virtue of the 3.0V charge on the 22μF capacitor and the forward characteristic of the LED. This circuit also shows simple methods of avoiding comparator chatter that could occur from power-supply transients: namely the inclusion of extra decoupling components at a comparator input (470pF capacitor) and the supply connection (51Ω series resistor).

PowerPath™ Controller

Figure 7 shows the implementation of a simple PowerPath controller using an LT6700-3. This circuit provides the switching logic for managing power sourcing from either a 2-cell alkaline pack or an external 3.3V AC adapter (wall wart) supply. When the external input is above 3.1V, the upper comparator section signals that external power is available and drives the MOSFET to an off-state, thereby isolating the cells from the load and reducing the cell discharge


to a couple of microamps. The load is then powered from the wall wart through the Schottky diode. When the external voltage disappears, the upper comparator section changes state and the MOSFET is driven to an on-state, connecting battery power to the load with an insignificant voltage loss. During the brief interval that the comparator requires to initially change

state, the battery is able to furnish power to the load via the MOSFET body-diode, but if the load is sufficiently capacitive, stored energy can provide the load current through the switch-over transient period without any significant dip in voltage.

The lower comparator section provides a low battery warning flag, and functions regardless of the source of power engaged.

The low voltage operating range of the LT6700, and the use of a low threshold MOSFET (1V), insures correct operation, even through periods of deep battery discharge.

Conclusion

The LT6700-1, LT6700-2 and LT6700-3 provide the designer with a versatile set of ultracompact dual comparators that include an on-chip 400mV reference. These devices are ideal for use in portable battery-powered application because of their unique simplicity, low voltage operation, micropower performance, and easy-to-use SOT-23 footprint. 

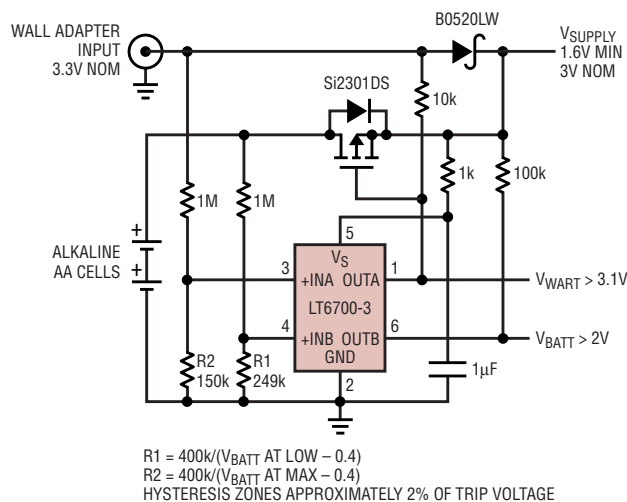


Figure 7. PowerPath controller

For more information on parts featured in this issue, see <http://www.linear.com/go/ltmag>

16-Channel 24-Bit No Latency Delta-Sigma ADCs Provide Efficient, Space-Saving, Flexible and Accurate Solutions for Data Acquisition

by Sean Wang

Introduction

The LTC2414 and LTC2418 are 8- and 16-channel No Latency $\Delta\Sigma$ ADCs in the Linear Technology's high accuracy $\Delta\Sigma$ family. Each combines a large number of inputs and extremely high accuracy, making it possible to acquire data from a variety of sensors directly with a single device. There are no complex trade-offs between common mode voltages, large or small input ranges and the temperature drift concerns. These devices are available in the 28-pin narrow SSOP package. The LTC2414 and LTC2418 are pin compatible and offer identical performance. The only difference between the two is in the number of input channels: the LTC2418 has 16 analog input channels while the LTC2414 has 8. The applications shown in this article can use either part, although the LTC2418 is used in this article to represent both parts. A 16-bit and pin compatible version of the LTC2418 is available in the LTC2439-1 for applications requiring less accuracy.

The input of the LTC2418 can be configured as 16 single-ended, 8 differential, or any combination of differential and single-ended channels to fit the end application (see Figure 1). Furthermore, the polarity of a differential channel can be reversed. Each configuration maintains the high performance of the core 24-bit ADC, including: 0.2ppm RMS and 3ppm total unadjusted error; full-scale differential input range of $-0.5 \cdot V_{REF}$ to $0.5 \cdot V_{REF}$; and an input common-mode voltage that can be anywhere within GND and V_{CC} for each channel with DC common mode input rejection better than 140dB.

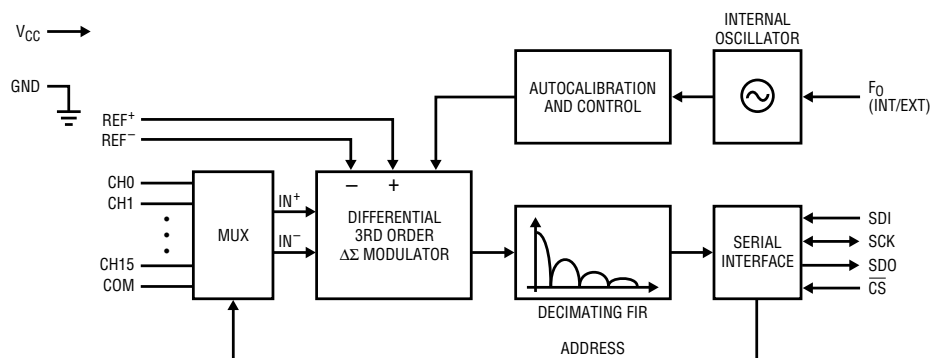


Figure 1a. LTC2418 combines a 17-input MUX with a core $\Delta\Sigma$ converter in one device

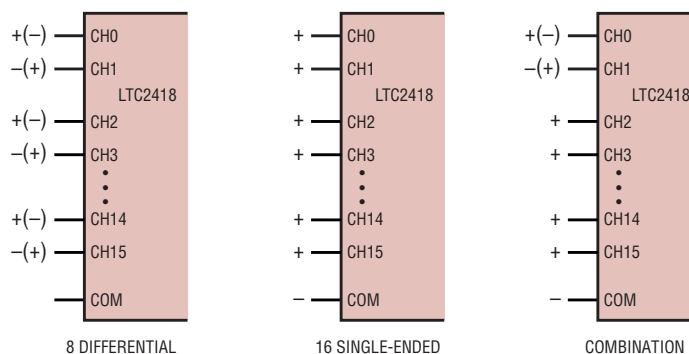


Figure 1b. LTC2418's flexible channel configuration allows any combination of 8 differential and 16 single-ended inputs.

The converter includes an on-chip oscillator that requires no external frequency setting components. A frequency select pin allows the LTC2418 to provide better than 110dB differential mode rejection at either 50Hz or 60Hz $\pm 2\%$. The LTC2418 communicates through a flexible 4-wire SPI digital interface with the channel address and a parity bit included in the data output, as shown in Figure 2. No extra register configuration is required except for the channel address.

One Part Takes All Measurements

The circuit in Figure 3 shows the versatility of the LTC2418. A combination of

single ended, differential, unipolar and bipolar input sources are simultaneously applied to the LTC2418. The low noise and high accuracy performance enable a wide dynamic input range while near zero drift (0.03ppm/°C full-scale drift, 20nV/°C offset drift) ensures consistent accuracy. The no latency feature guarantees that the first conversion result is accurate after a new channel is selected, significantly reducing the overhead typically associated with multiplexed $\Delta\Sigma$ ADCs. This feature provides a very simple switching scheme between different channels. Furthermore, the selected channel address and a parity bit are included in the data output to ensure

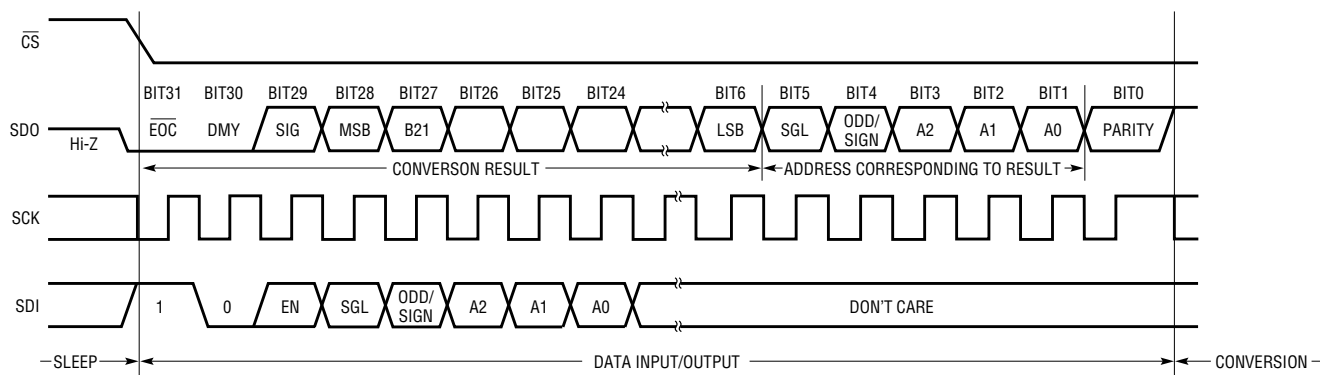


Figure 2. Simple digital input/output includes channel read-back and parity check

data integrity in noisy isolated environments.

Sensors with common mode output voltages at ground, V_{CC} , or anywhere in between may be digitized. Sensors with only a few mV full-scale outputs may be applied directly to the LTC2418. Large sensor offsets and tare voltages are transparently handled by the converter's wide input range, eliminating complex front end analog processing. Large level input signals ranging from GND to $0.5V_{REF}$ ($2.5V$) may also be applied to the device.

Here are the details of each input circuit shown in Figure 3:

□ CH0 and CH1 are configured to measure a current sense resistor with a differential input of 0 to 10mV and common-mode voltage near V_{CC} . The ability to handle a common-mode voltage up to V_{CC} directly and the high accuracy of the LTC2418 allow it to monitor

currents over a wide, 0A to 1A, while incurring a minimum drop in the monitored power supply. The LTC2418 achieves 10,000 counts resolution without a gain stage or common-mode shift.

- CH2 and CH3 differentially measure a 350 Ω bridge with common-mode voltage near $V_{CC}/2$. Typical strain gauge based bridges deliver 2mV/Volt of excitation, so the bipolar input is from -10mV to +10mV. The resolution is 1 part in 10,000 without averaging or external gain stages.
- CH4 and CH5 measure a thermistor in a half bridge application. In the example the output ranges from 0.77V to 2.47V over 0°C to 40°C. The LTC2418 can digitize the signal directly due to its excellent common-mode rejection and linearity.

□ CH6 accepts a large-swing, single-ended signal with a range from ground to 2.5V ($0.5 \cdot V_{REF}$). A reading equivalent to that of a 6-digit DVM is possible due to the accuracy and low noise ($1\mu V_{RMS}$) of the LTC2418.

□ CH7 measures a single-ended output of a thermocouple with near ground common-mode. The input can go slightly below ground without affecting the conversion accuracy. Cold junction compensation can be performed to get the accurate absolute temperature using a cold junction sensor similar to the thermistor circuit applied to CH4 and CH5. The temperature measurement may then be used to compensate the temperature effects of the bridge transducers like the one connected to CH2 and CH3.

The above channels measure a wide variety of sensors while using just half of the LTC2418's channels. Similar circuits can be easily added to the remaining eight channels in order to take more measurements. The channel address identification and the parity bit included in the output bit stream provide a convenient way to verify which sensor is being monitored and check the digital transmission integrity.

Simple Analog and Digital Interface

The LTC2418 interface, both analog and digital, is very simple. The analog inputs go through a multiplexer and drive the 3rd order modulator directly so the input common mode voltage

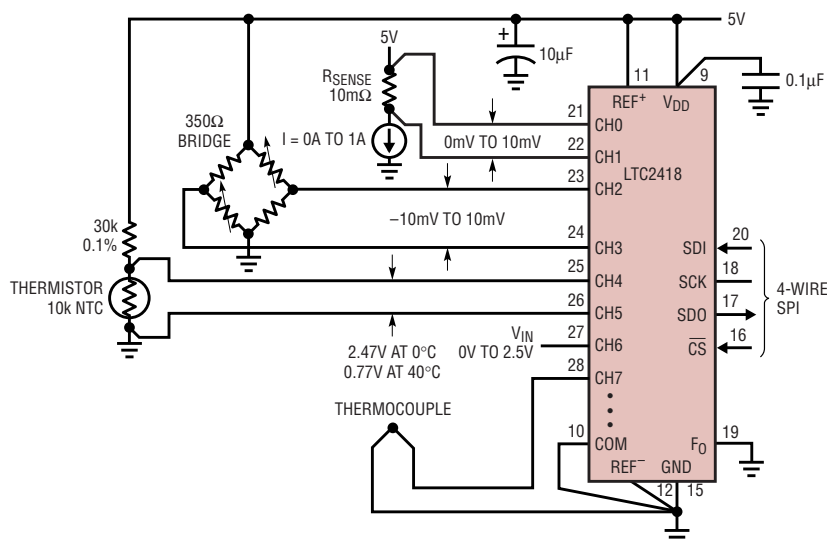


Figure 3. The versatility of LTC2418 allows a variety of sensors to be measured by a single device.

continued on page 28

300MHz–7GHz RF Detector Provides a Compact, Low Power Solution for RF Power Monitoring and Control Applications

by Ted Henderson and Vladimir Dvorkin

Introduction

The LTC5508 is a very wide bandwidth RF power detector that can be used in RF applications that cover a wide range of frequencies and power levels. This device exhibits excellent sensitivity and temperature stability over an input frequency range of 300MHz to 7GHz and an input power range of -32dBm to 12dBm. The operating current is less than 600 μ A, and in shutdown mode, the quiescent current is less than 2 μ A. The power detector contains a balanced Schottky diode configuration that together with an internal capacitor forms a peak detector (see Figure 1). This is followed by a dynamic range expansion circuit (gain compression block) and a buffer amplifier. The only required external components serve for coupling to the

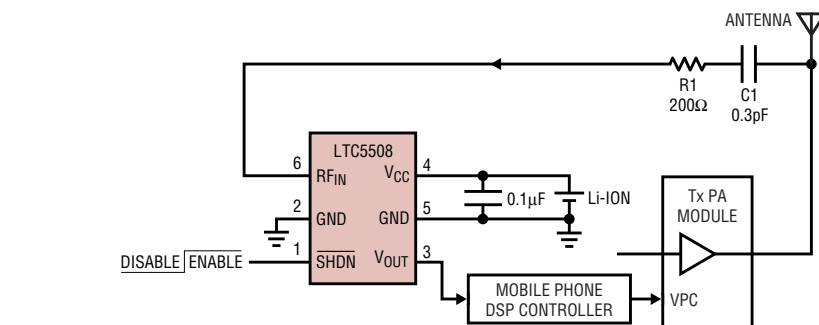


Figure 2. LTC5508 single band Tx power control application diagram with a capacitive tap.

RF input pin and for power supply decoupling as indicated in Figure 2. The LTC5508 is packaged in an SC70 package, and requires as few as one or two external components.

Figure 3 shows the LTC5508's output voltage vs. RF Input Power.

Figure 4 shows how the output voltage varies vs. temperature for several different RF input levels at 2GHz and 5GHz.

Applications of the LTC5508 include all flavors of IEEE 802.11 Wireless LAN, RF Infrastructure (IF Gain

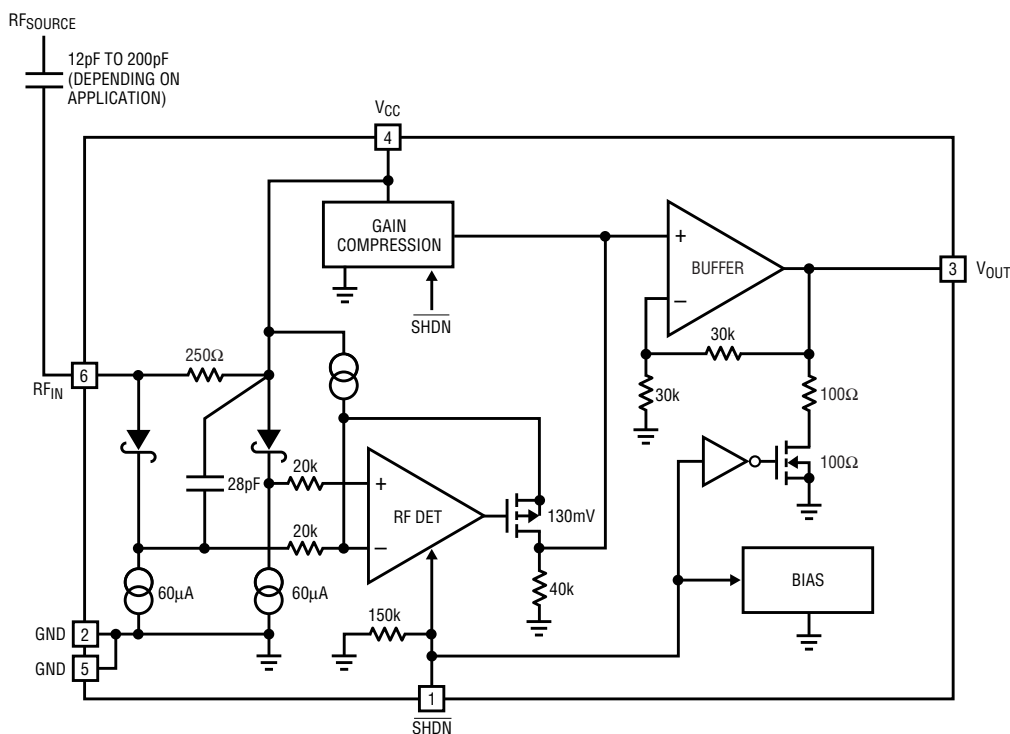


Figure 1. LTC5508 block diagram

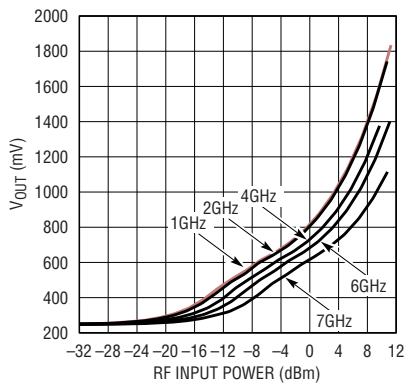


Figure 3. Typical LTC5508 output voltage vs RF input power level

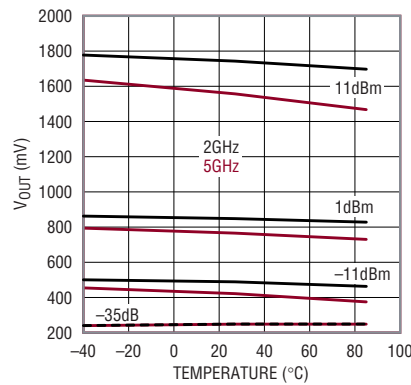


Figure 4. Typical LTC5508 output voltage change vs temperature for different input power levels at input RF frequencies of 2GHz and 5GHz

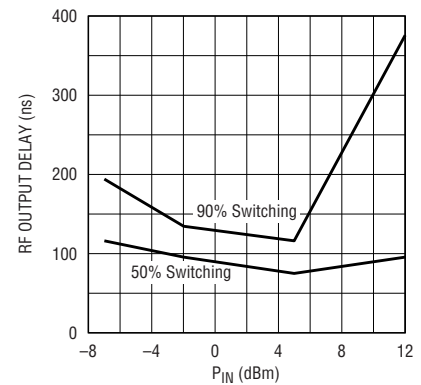


Figure 5. Typical LTC5508 output delay vs input power level

Control; RSSI for wireless, CATV and optical applications), RF Power Sensors (alarms, power meters, RF power control), and ASK Demodulators (home security, remote monitoring, low cost receivers). The LTC5508 is especially well suited to IEEE 802.11a applications, which require operation in the 5GHz–6GHz frequency range, and for combo applications such as 802.11a/b and 802.11a/g applications, which require operation at both 2.5GHz and at 5GHz–6GHz. It is also an optimal solution for cellphone and wireless modem applications, which benefit from its ultrasmall packaging.

A Typical Application

In a typical RF power control application, a small amount of RF output power is coupled from the antenna to the LTC5508 input. The LTC5508 output is a low frequency signal proportional to the instantaneous peak value of the RF input voltage. The output response time for different input power levels is shown in Figure 5. This low frequency signal is compared to an external reference level by an analog or digital block which then controls the transmit power amplifier.

Figures 2 and 6 show examples of single band and dual band, mobile phone transmitter power control using the LTC5508 IC with a simple R-C antenna tap. A 0.3pF capacitor (C1) followed by a 200Ω resistor (R1) forms a circuit with about –15dB coupling factor between the antenna and the LTC5508 in the PCS (1.8GHz–1.9GHz) band. The coupling

factor is approximately –20dB in the cellular (800MHz–900MHz) band. For improved coupling accuracy, the C1 capacitor should be a tight tolerance component ($\pm 0.05\text{pF}$), which is available from American Technical Ceramics. In an actual product implementation, the value of C1 and R1 may differ, depending on parts placement, printed circuit board (PCB) parasitics and antenna parameters.

The actual coupling factor can be optimized to satisfy the application requirements for power control level, power control range, and output power loss at the antenna. For example, the coupling factor between the LTC5508 and the antenna can be reduced by increasing the value of R1 from 200Ω to 220Ω or 240Ω using resistors with a 1% tolerance. For actual production, 1% tolerance resistors are preferable, but 5% tolerance is acceptable for most applications. The optimum value of

C1 is 0.3pF. If a 0.3 pF capacitor introduces too much loss into the main signal line, a lower value capacitor of 0.2pF can be used. With the component values indicated in Figures 2 and 6, the LTC5508 can be used to detect the RF output power with less than 0.1dB output signal loss at the antenna.

Capacitor C1 should be placed as close as possible to the antenna (without forming a “T” connection on the main microstrip line), and immediately followed by the R1 resistor and the LTC5508. C1, R1 and the LTC5508 should all be placed on the same side of the PCB as the PA output microstrip line to the antenna. If a PCB via is unavoidable in order to bring the coupled signal from one side of the PCB to the other, place the via at the connection of R1 to the LTC5508 RF input.

To minimize loss of RF power out of the antenna, and to maximize the

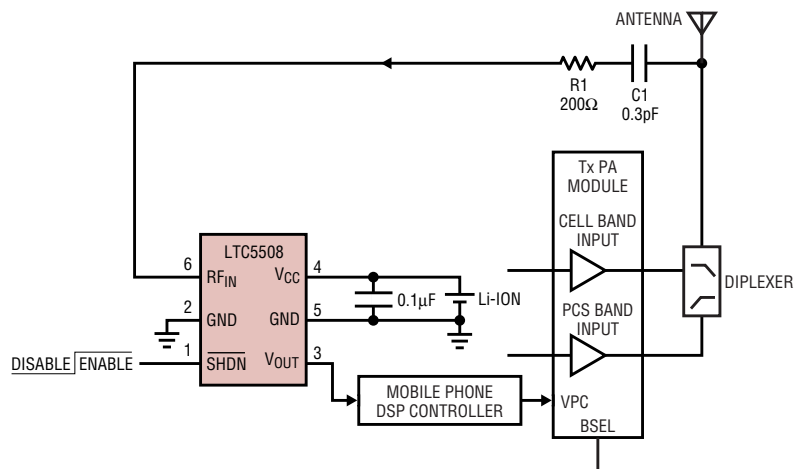


Figure 6. LTC5508 dual band Tx power control application with capacitive tap.

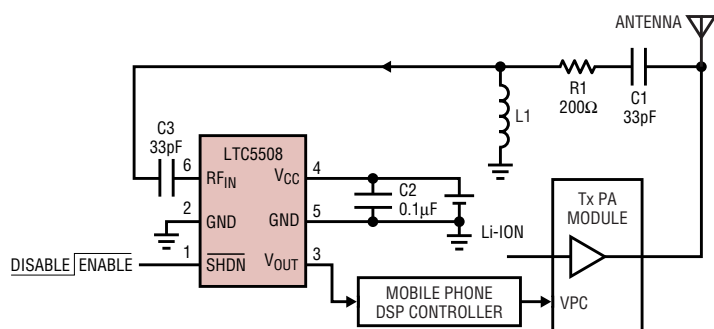



Figure 7. LTC5508 single band Tx power control application with a capacitive tap and optional shunt inductor.

sensitivity of the LTC5508, a shunt inductor (L1) to ground can be placed at the LTC5508's RF input (see Figure 7). The shunt inductor value should be chosen to tune out the

parasitic shunt capacitance of the IC package and the PCB parasitics at the frequency of interest. This will also require a DC blocking capacitor (C3 = 33pF), to decouple the L1 DC

path to ground from the LTC5508's internal DC bias. For PCS band applications, a value for L1 of 3.3nH to 5.6nH is recommended.

Conclusion

The LTC5508 adds to Linear Technology's RF power detector and RF power control family. The LTC5508 combines an RF peak detector and buffer amplifier in a small (2mm × 2mm) 6-pin SC70 package. The LTC5508 has a very wide RF bandwidth and input power range, low temperature drift, minimum external component requirements and a very small footprint, making this device an ideal choice for a wide range of RF detector applications. 

LTC2418, continued from page 25

can be anywhere between GND and V_{CC} , unlike $\Delta\Sigma$ parts with front-end buffers or gains that need the input to be above GND and below V_{CC} .

The LTC2418 performs offset and full-scale calibrations in every conversion cycle. The calibrations are transparent to the user—neither a calibration register nor a tedious calibration process is required to achieve stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift. This, combined with the No Latency feature, means that the conversion result is accurate immediately after a new channel is selected, without any latency or calibration delay, as shown in Figure 4.

Noise Rejection

Using its internal oscillator, the LTC2418 can be configured for better than 110dB differential mode rejection at 50Hz or 60Hz $\pm 2\%$ line frequency and harmonics by simply tying Pin F_0 to V_{CC} or GND. The unique digital filter design also provides a simultaneous 50Hz and 60Hz rejection option if driven by an external clock of 140kHz. The rejection over 48Hz to 62.4Hz is better than 87dB, as shown in Figure 5. The same performance is obtained for the internal clock mode

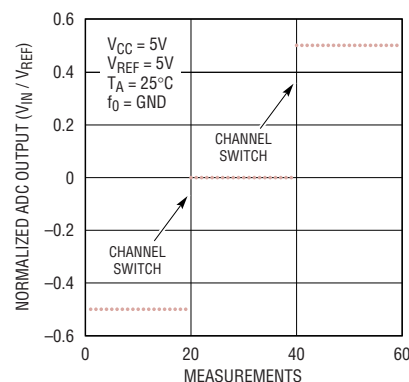


Figure 4. The No Latency architecture eliminates settling errors even for large input steps on a multiplexed channel change.

with the frequency scaled to have the notch frequency at 60Hz ($F_0 = \text{GND}$) or 50Hz ($F_0 = V_{CC}$).

In industrial applications, it is not uncommon to measure a small signal superimposed over relatively large perturbations. Traditional high order $\Delta\Sigma$ modulators suffer from potential instabilities at large input signal levels. The proprietary architecture used for Linear Technology's $\Delta\Sigma$ family guarantees predictable and stable behavior even when the input AC perturbation is 150% of the full scale, as shown by measurements in Figure 5. It is clear that the LTC2418 rejection performance is maintained

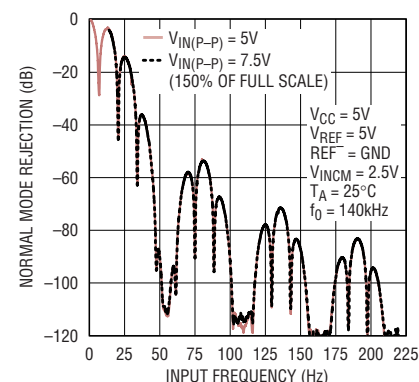



Figure 5. Simultaneous 50Hz/60Hz rejection of large input AC perturbation with $f_0 = 140\text{kHz}$. Scale frequency axis for rejection performance using internal oscillator or other external clock frequency.

without compromise in this extreme situation.

Conclusion

The LTC2418 is the multi-channel addition to Linear Technology's 24-bit differential $\Delta\Sigma$ family. A reduced channel, and pin compatible version is also available in the LTC2414. The LTC2414 can be configured as 4 differential inputs or 8 single-ended inputs. The LTC2414 and LTC2418 are available in 28-pin GN packages. With high absolute accuracy, ease-of-use and near zero drift, they provide very efficient solutions for multiple sensor acquisition applications. 

Combo Hot Swap/Load Share Controller Allows the Use of Standard Power Modules in Redundant Power Systems

by Vladimir Ostrerov and David Soo

Introduction

High power, high-reliability electronics systems depend on power supply load sharing to handle the heavy current loads and to increase system robustness. Usually the load is shared between modular DC/DC converters operated in parallel, a topology that offers several advantages depending on how it is implemented:

- ❑ **Redundancy.** Typically, load sharing power supplies can provide more power than the system can use. This way if any of the power supplies fail, the remaining power supplies can still support the load. Redundancy requires that a failed power supply is automatically isolated from the system, and that it can be replaced without interrupting the system power.
- ❑ **Reliability.** The reliability of the system depends in large part on the current sharing capability of the power supply modules. Ideally, the current is distributed evenly amongst the power supplies, so that on average each module dissipates equal heat. This in turn increases system lifetime.

- ❑ **Efficiency.** For very high power systems, significant efficiency gains can be achieved by operating converters at their most efficient operating point, which is somewhere in the middle of a converter's operational load range. In a parallel multi-converter architecture, efficiency is clearly at maximum when each converter operates at this optimum point. The only way to achieve this over a wide load range is to enable or disable converter modules as load re-

"The LTC4350 simplifies the design of load sharing systems by combining both a load share controller and a Hot Swap controller in one package."

quirements change, in order to keep the enabled modules operating at loads near their maximum efficiency. The LTC4350 makes this possible via its Hot Swap™ feature, which allows modules to be disabled or enabled on the fly without interrupting the power bus.

The LTC4350 simplifies the design of load sharing systems by combining both a load share controller and a Hot Swap controller in one package. The load share controller equalizes the current handling of each paralleled power supply, and the Hot Swap controller allows power supply modules to be safely removed from, or inserted into, a hot system.

Overview of the LTC4350's Features

The LTC4350's load share and Hot Swap controllers are connected by internal logic which coordinates load-sharing and hot swapping activities. The LTC4350's load share controller is a closed loop control system with a full set of features including precise voltage control and accurate current sharing. The closed loop control system has defined bandwidth and transient characteristics.

The LTC4350 protects the system it is powering from overvoltage and undervoltage conditions with separate overvoltage (OV) and undervoltage (UV) comparators, each with its own reference source. A timer sets the delay between events, when the UV pin goes high, and when load sharing turns on.

The LTC4350 enables active current sharing between the power supplies using an inner current loop and an automatic master outer voltage loop controller assignment. The power system based on the LTC4350 controllers with n power channels is shown in Figure 1. Each channel consists of the power module (DC/DC Converter); one LTC4350; a bidirectional power switch which connects the power module output to the load (a series connection of the two MOSFETs Q1 and Q2); a current sense resistor R_{SENSE} ; a few passive components to set loop compensation; and miscellaneous feedback circuitry. Each power module is controlled by one LTC4350. The LTC4350 SB (share bus) pins are connected together to form the load share bus. The voltage drop on the sense resistor R_{SENSE} is used as a feedback signal in the current control loop. The output voltage of each module is

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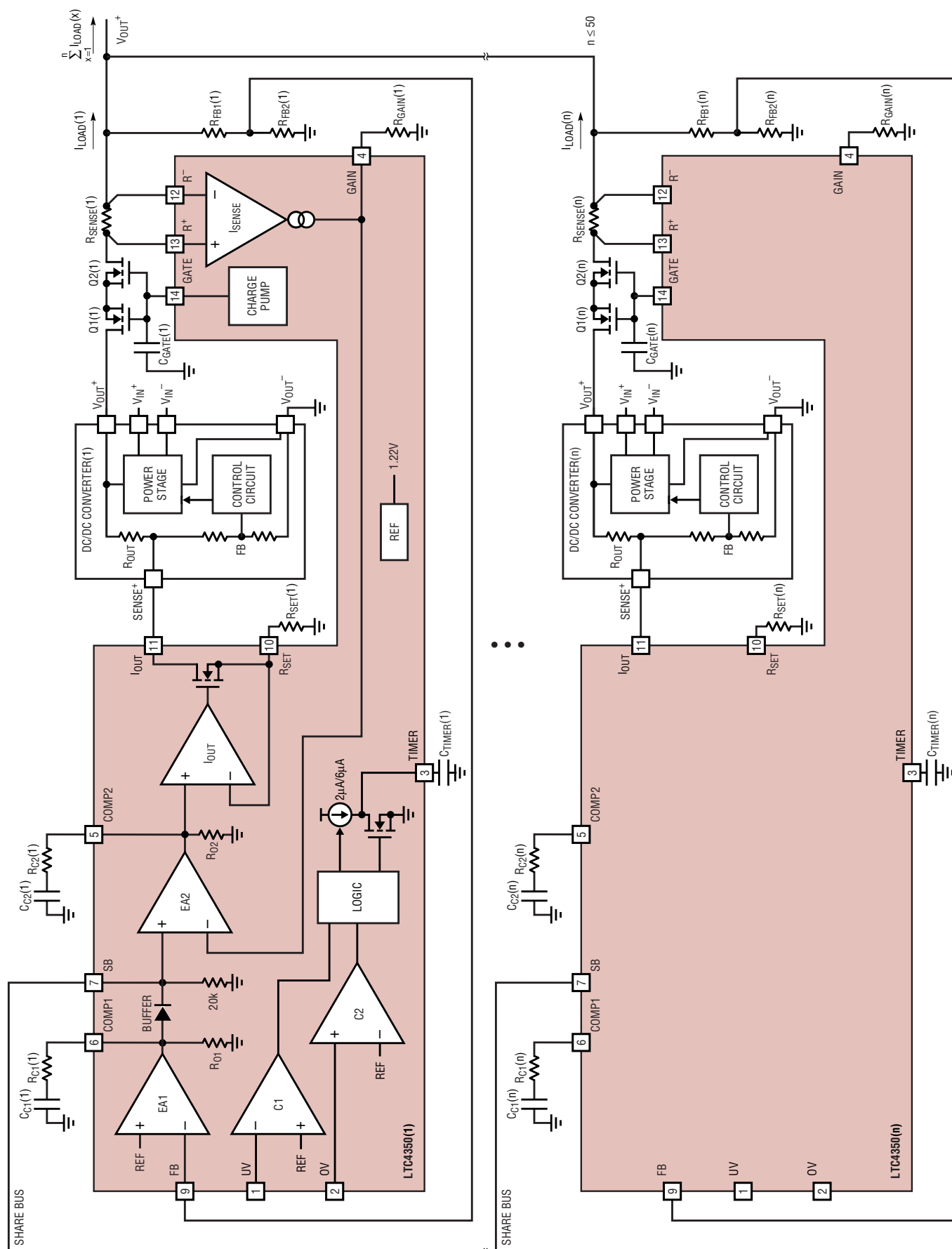


Figure 1. LTC4350-based power system

modified by the LTC4350 so that each module contributes an equal amount of current to the load.

The LTC4350 uses the power module remote sense input to adjust the power module output voltage. Each power channel is a 2-loop control system, the inner loop is a current control loop and the outer loop is a voltage control loop. The share bus voltage serves as the common command signal from the outer voltage control loop to all the current control loops, for each power module.

The current control loop includes:

- ❑ the current loop error amplifier (EA2) which includes compensation network $R_{C2}C_{C2}$;
- ❑ the voltage-to-current converter to drive the module's sense resistor (R_{OUT});
- ❑ the DC/DC converter module (as the plant of the loop);
- ❑ a load current sense amplifier consisting of current sense resistor R_{SENSE} and current signal amplifier I_{SENSE} (which uses a resistor connected to ground from the R_{GAIN} pin to set the current to voltage transfer ratio).

The voltage control loop includes:

- ❑ the voltage error amplifier (EA1) which includes compensation network $R_{C1}C_{C1}$;
- ❑ the internal 1.220V reference;
- ❑ the previously mentioned closed current loop;
- ❑ feedback divider ($R_{FB1}R_{FB2}$).

Table 1. Typical error amplifier parameters

Parameter	EA1 Voltage Error Amp	EA2 Current Error Amp
R_O	$24.7 \times 10^6 \Omega$	$8.5 \times 10^6 \Omega$
g_m	$0.769 k\Omega^{-1}$	$0.25 k\Omega^{-1}$

Only one voltage control loop is active, the other controller voltage error amplifier outputs are isolated by series diodes between the amplifier outputs and the share bus. This automatic selection of a master voltage control loop is the result of component tolerances. The voltage error amplifier providing the highest output level reverse biases the series diodes of all the other error amplifiers. If the channel functioning as the master controller fails or is removed from the system, the controller with the next highest output level becomes the master.

The LTC4350's hot swapping feature eliminates power supply transient stress in hot-insertion and hot-removal and isolates faulty modules by disabling the external power switch. The failed supply can be removed and replaced with a new one without interruption to the power system. The hot swap circuitry consists of the gate driver (pin 14) and the reverse current comparator.

Figure 1 shows a system with n power supplies and n LTC4350s, where $n \leq 50$. Each power channel is connected to the system power bus identically by paralleling the share bus (SB), positive (OUT+) and negative (OUT- or GND) outputs.

The LTC4350 is packaged in a 16-pin IC narrow SSOP package and operates over the range of 1.5V to 12V, which can be extended down to 1V with auxiliary circuitry. It should be noted that the share bus maximum voltage and gate voltage are a function of the LTC4350 supply voltage (V_{CC}).

Hot Swap FET Gate Drive Characteristics

The Hot Swap FET switch gate turn on voltage slew rate is a function of total gate capacitance including any additionally added capacitance and the 10 μ A charge pump output current as given by:

$$\frac{dV_{GATE}}{dt} = \frac{10}{C_{GATE}} \text{ V/s}$$

where C_{GATE} is in μ F

The 10mA high current sink capability of the gate pin shuts the FET switch off almost 1000 times faster than FET turn on.

Tailoring the Control System to Various Power System Designs

The wide range of available power modules, each with a different dynamic characteristics, requires tailoring the current and voltage control loops for each power system design.

The voltage loop and current loop error amplifiers EA1 and EA2 are transconductance amplifiers with output impedances of R_{O1} and R_{O2} and transconductances of g_{m1} and g_{m2} . The use of transconductance error amplifiers provides a simple means of compensation using simple RC shunt networks to ground.

Adding a shunt capacitor to ground converts the transconductance amplifier into a dynamic block with the transfer function of:

$$W(s) = \frac{G_{EA}}{T_p s + 1}$$

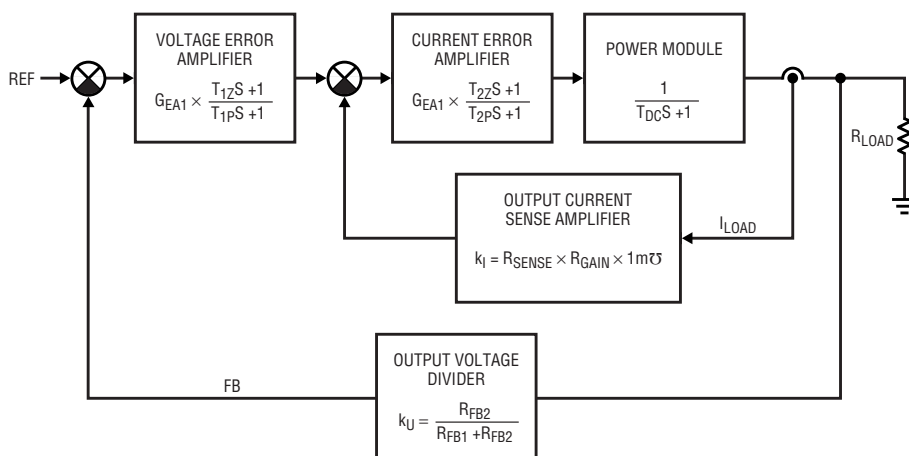


Figure 2. Power channel control system block diagram

where $G_{EA} = g_m R_O$ and $T_p = C_C R_O$

which includes the effect of the finite output resistance R_O .

The insertion of a resistor in series with the shunt capacitor adds a zero to the transfer function:

$$W(s) = G_{EA} \cdot \frac{T_Z s + 1}{T_p s + 1}$$

where:

$2\pi f_p = \omega_p = 1/T_p = 1/C_C(R_O + R_C)$ is the pole frequency,

$G_{EA} = g_m R_O$ is the error amplifier gain,

R_C and C_C are compensation components, and T_Z = Main time constant of the power converter.

The error amplifier parameters are not specified in the data sheet, but typical values are shown in Table 1.

A power channel control system block diagram for dynamic analysis is shown in Figure 2.

Operating Modes and Design Considerations

Load Share Controller Operation

LTC4350 performs load sharing as follows. All power supplies are preliminarily adjusted to 250mV–300mV below the desired output voltage. Each LTC4350 can increase the output voltage of its respective power module by creating an additional voltage drop across R_{OUT} —that is, the I_{OUT} amplifier sinks current through R_{OUT} to increase the module's output voltage. The LTC4350, using feedback from the common load share bus and the inner current loop, adjusts each supply to the desired output voltage and balances the load across all the supplies.

The LTC4350 can control output voltages down to 1.5V without the use of auxiliary circuitry. (To use the LTC4350 with output voltages below 1.5V, see Figure 6.) The LTC4350 has an internal 1.22V reference. The voltage feedback divider resistors for the outer voltage control loop are calculated from:

$$V_{OUT} = V_{REF}(1 + R_{FB1}/R_{FB2})$$

where $V_{REF} = 1.22V$

Hot Swap Controller Operation

The LTC4350-controlled external power switch allows power supplies to be hot swapped in and out of the powered system, minimizing disturbances on the system power bus. The external capacitance at the GATE pin is charged and discharged by constant current sources and controls the rate of turn on and turn off of the external FET switch. The undervoltage and overvoltage comparators in the LTC4350 monitor the power module and only enable the hot swap function when the power module output voltage is within tolerance. When the power supply is disconnected, the undervoltage comparator indicates a fault condition, the power switch gate is quickly discharged and the load is isolated from the power supply.

Special attention should be paid to choosing the gate voltage slew rate. The gate voltage slew rate should be chosen such that the load share control loop can prevent excessive reverse current flow into the power supply output capacitors when the external FET switch closes and load share is activated. The LTC4350 monitors reverse (negative) current flow. The reverse current limit (RCL) set point is calculated from:

$$I_{RCL} = 30mV/R_{SENSE}$$

One way to minimize the amount of reverse current is to minimize the bulk capacitance on the power module side of the MOSFET—taking the minimum capacitive loading requirements for the power supply module into account. If the DC/DC converter is capable of converting energy in both directions (source or sink current) the high reverse current in the transient caused by powering up additional modules can reach the reverse current protection level I_{RCL} . The only solutions are to reduce the external MOSFET gate slew rate and/or set the I_{RCL} threshold higher by lowering R_{SENSE} . Both solutions add their own problems, though. Reducing the MOSFET slew rate slows the disconnect rate of a failing or faulty power module (the two rates are directly proportional, both based on the GATE pin capacitance). Reducing R_{SENSE} lowers overall gain.

A balance must be struck with these competing requirements.

Protection Features

The LTC4350 can identify faults in the power supply and isolate it from the load when an external MOSFET power switch is used. In the case of a power supply output short to ground, the reverse current detector senses that the voltage across the current sense resistor has changed direction and has exceeded 30mV for more than 5 μ s. The power switch gate is immediately pulled low disconnecting the short from the load. The external MOSFET gate is allowed to ramp-up and turn-on the power switch as soon as the reverse voltage across the sense resistor is less than 30mV and the module output voltage is within the undervoltage–overvoltage comparator window. The condition where a power supply output shorts to high voltage is detected as an overvoltage fault. In this case, the gate of the power switch is pulled low, disconnecting the overvoltage from the load.

The STATUS pin state reports any of three types of faults. The first is undervoltage lockout when the UV pin falls below 1.220V while the output voltage is active. The second failure is an overvoltage condition when the OV pin is above 1.220V. The third fault is an overload or open supply output condition when the COMP2 pin is above 1.5V or below 0.5V and the voltage on the GAIN pin is greater than 100mV.

Control System Compensation

The design approach for the control system loop is to maximize the power system bandwidth. Besides the obvious benefits of the fast system and transient response, a high control loop bandwidth minimizes disturbances when connecting the power supply output to the operating bus.

The optimum solution for a power channel with a DC/DC converter and an LTC4350 load share controller is to design the load share inner current control loop channel bandwidth equal to, or close to, the DC/DC converter bandwidth, and the voltage loop

bandwidth 5% to 10% higher than the current loop bandwidth.

It is important that the step response of the closed current loop should be similar to the response of a first order system or second order system with a damping ratio of $\zeta \geq 0.75$. If this condition is not met, the step response will not be monotonic and will result in chattering oscillation as the voltage control loop keeps changing masters and the module output currents oscillate about their equilibrium values.

The control loop design starts with characterizing the DC/DC converter response. If the converter behaves like a first order system, the converter loop time constant, T_{DC} , can be calculated from the converter's 3dB frequency response, ω_{CROSS} , by $\omega_{CROSS} = 1/T_{DC}$.

To realize the maximum current loop bandwidth, which is equal to the DC/DC crossover frequency ω_{CROSS} , a current loop compensation network of the form:

$$W_{CURRENT}(s) = G_{EA} \cdot \frac{T_{2z}s + 1}{T_{2p}s + 1}$$

is required where T_{2p} and T_{2z} are the pole and zero time constants of the current loop error amplifier EA2. The maximum stable bandwidth is obtained when $T_{2z} = T_{DC}$. With any larger T_{2z} , the current loop bandwidth, $\omega_{CURRENT}$, will be less than ω_{CROSS} . The current error amplifier EA2 pole T_{2p} is used to set the overall open loop gain and must take into consideration the other gain terms in the current loop transfer function such as the load current sense amp I_{SENSE} and the voltage-to-current converter I_{OUT} . The requirements for setting the gains of these other blocks are discussed later. Figure 3 shows the response of a current control loop meeting the above criteria for 1st order plant compensation.

If the converter behaves like a second order system, the crossover frequency of the inner current control loop is reduced so that the composite loop behaves like a first order loop or an overdamped second order loop with $\zeta \geq 0.75$. This is achieved by matching the control loop zero T_{2z} to the cross

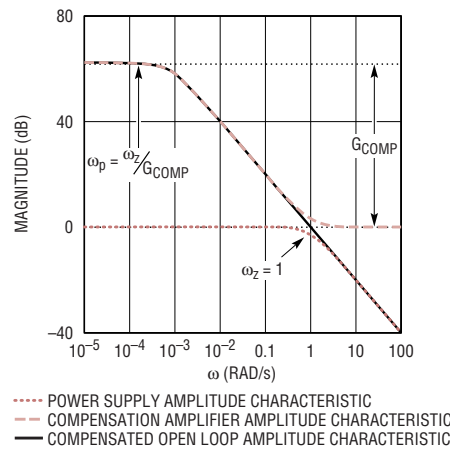


Figure 3. 1st order plant compensation

over frequency of the power module. $T_{2z} = 1/\omega_{CROSS}$ and then suppressing the gain of the control loop by 10dB to 15dB by adjusting T_{2p} appropriately. Figure 4 shows the approach to 2nd order power module compensation.

The other elements in the LTC4350 current and voltage loops must be chosen so as to guarantee normal loop operation up to the actual current limit, I_L , of the power module regardless of how much I_L exceeds the modules maximum output current specification. The maximum feedback current signal (voltage on the GAIN pin) must be lower than the maximum share bus voltage ($V_{SHARE BUS (MAX)}$) at an output current of I_L , where $V_{SHARE BUS (MAX)}$ is the lesser of $[(V_{CC} - 1.5V)]$ and $(5.6V)$.

This requirement has implications on the selection of R_{SENSE} and R_{GAIN} : $I_L R_{SENSE} R_{GAIN} / 1k\Omega \leq V_{SHARE BUS (MAX)}$

R_{SENSE} is chosen to provide the necessary 30mV reverse current detection at an acceptable fault current limit while minimizing power loss and forward voltage drop. The value of R_{GAIN} is then derived using the previous equations above maximizing the output voltage within the constraints of $V_{SHARE BUS (MAX)}$.

The current control loop error amplifier output voltage level of EA2 is converted to a current (by the I_{OUT} block), which is used to modulate the power module output voltage. The maximum output current capability of I_{OUT} is 20mA. The LTC4350 current measurement system gain is set

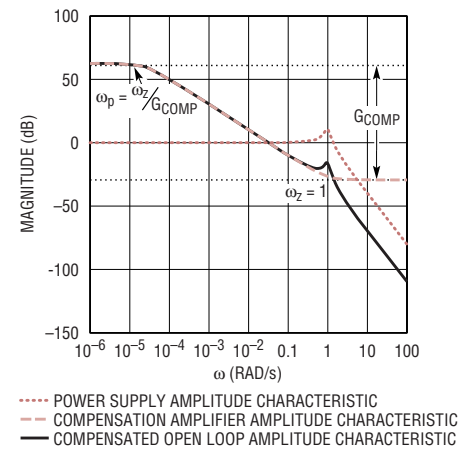


Figure 4. 2nd order plant compensation

by resistor R_{SET} connected between ground and the R_{SET} pin. The current range should be selected such that the LTC4350 can realize a 1V control range on the power module. This current is drawn from the +SENSE terminal of the power module. If the internal -resistance R_{OUT} between + V_{OUT} and +SENSE is less than 50 Ω , an external driver is needed to boost the 20mA maximum current to achieve the required 1V control range. The design example in figure 5 shows a circuit to boost the I_{OUT} current.

The open loop transfer function for the inner current control loop is:

$$LT = \frac{-I_{LOAD} R_{SENSE} R_{GAIN} G_{EA2} (T_{2z}s + 1) R_{OUT}}{1k\Omega (T_{2p}s + 1) R_{SET}}$$

T_{2p} is calculated by setting $|LT| = 1$ at ω_{CROSS} for a first order loop and for a 2nd order underdamped loop, T_{2p} is increased by a factor of 3 to 5 so that the loop crossover occurs below the peak in the module frequency response.

The overall voltage loop crossover frequency at $\omega_{VOLTAGE}$ should be set 5% to 10% above the current loop crossover frequency ω_{CROSS} . This prevents interaction between the inner current and outer voltage loops such that the output voltage responds quickly to transients and then the current control loop adjusts each power supply so that the loads are balanced.

Design Examples

A dual supply load share design example is shown in Figure 5. This design uses DATEL power modules with an

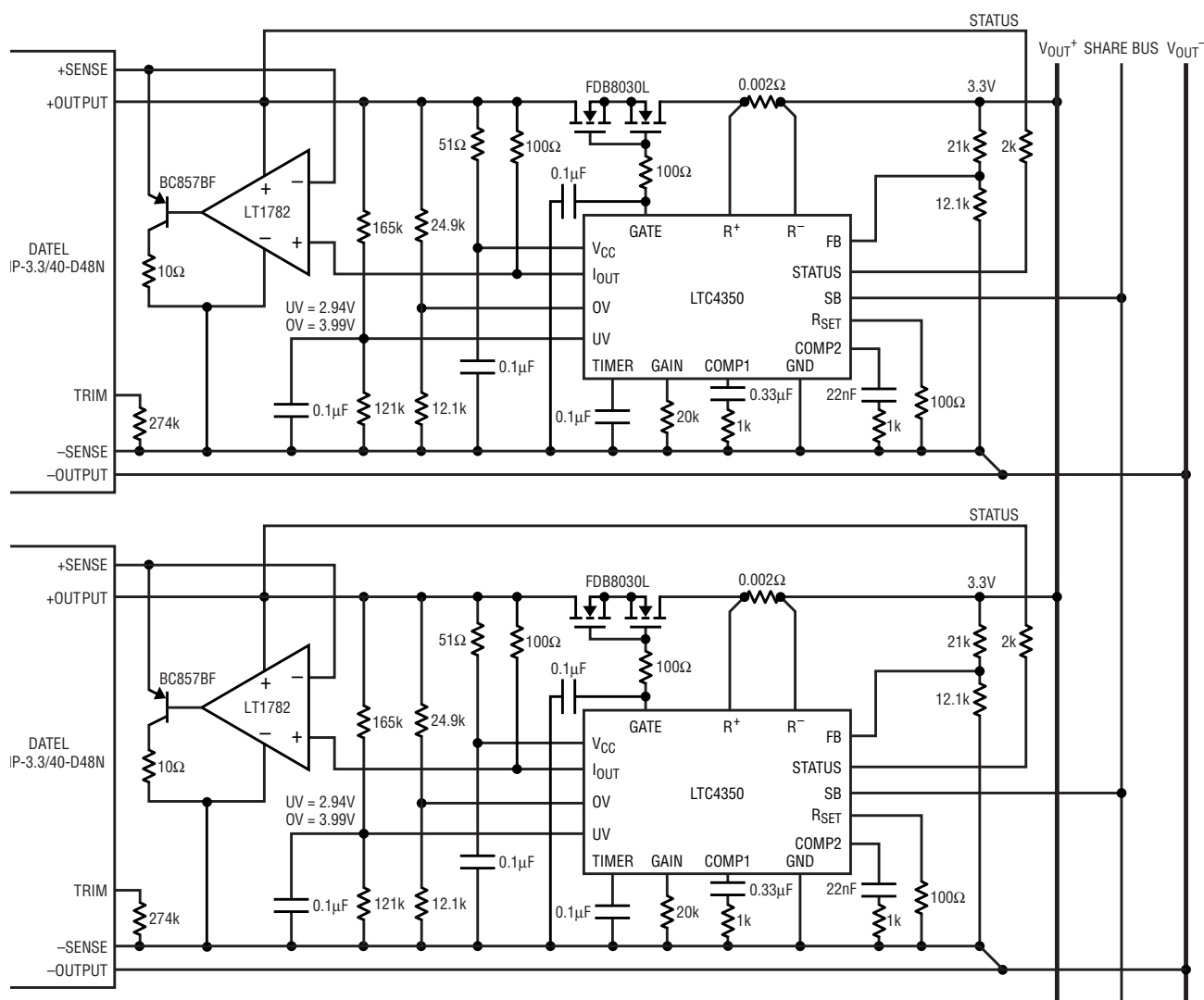



Figure 5. 3.3V Load share controller for DATEL® power modules

$R_{OUT} < 50\Omega$. To provide the required voltage control range, the I_{OUT} current is boosted with an external current amplifier.

To load share power supplies with output voltages below 1.5V, the feedback voltage must be amplified to match the 1.22V internal reference

on the feedback pin as shown in Figure 6.

Conclusion

The LTC4350 combines Hot Swap and load share functions into one IC, making it possible to provide effective power management solutions using standard off the shelf DC/DC converter modules. The LTC4350 also simplifies the design of custom supplies. The Hot Swap and load share functions work in concert to facilitate the addition of power system features that improve overall reliability and reduce down time, including fault isolation and identification, Hot Swap replacement of failed modules, redundancy, and improved thermal management. 

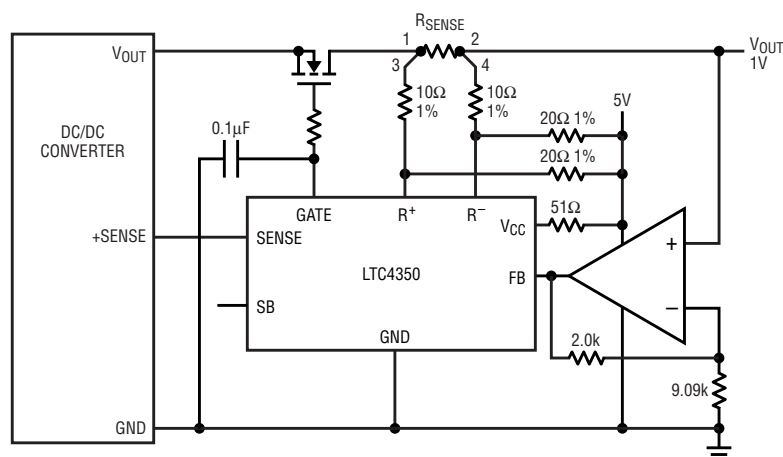


Figure 6. Example of 1V load share implementation (one channel)

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Double Maximum Load Current with Two Parallel Converters

by Keith Szolusha

Automotive, industrial, and FireWire® peripherals all call for high efficiency, space-saving power supplies with high current capabilities at very high voltages. The problem is that high voltage, monolithic (where the power switch is included) high current buck converters aren't always beefy enough to handle the required load currents. One solution is to parallel two converters to double the maximum load current. A few modifications to the standard buck

FireWire is a registered trademark of Apple Computer Corp.

converter configuration are required to maintain load-sharing and stability between the two converters and reduce input and output ripple.

Figure 1 shows a 8V–40V input, 5V output at 4A maximum load current DC/DC converter using two LT3430 60V monolithic 3A (peak switch current) buck regulators in parallel. The ICs are synchronized at up to 250kHz with a 180° phase shift between the two using the LTC6902 Multiphase Oscillator with Spread Spectrum Frequency Modulation.

Synchronization is important since the fixed 200kHz internal switching frequency varies slightly from part to part. If the two parallel converters are allowed to run at different frequencies, there is the possibility that, over time, the output ripple will carry some undesirable low frequency ripple components equal to the difference in frequency of the two ICs.

Running the two ICs 180° out of phase reduces input and output ripple. Usually, one IC is increasing current while the other IC is decreasing cur-

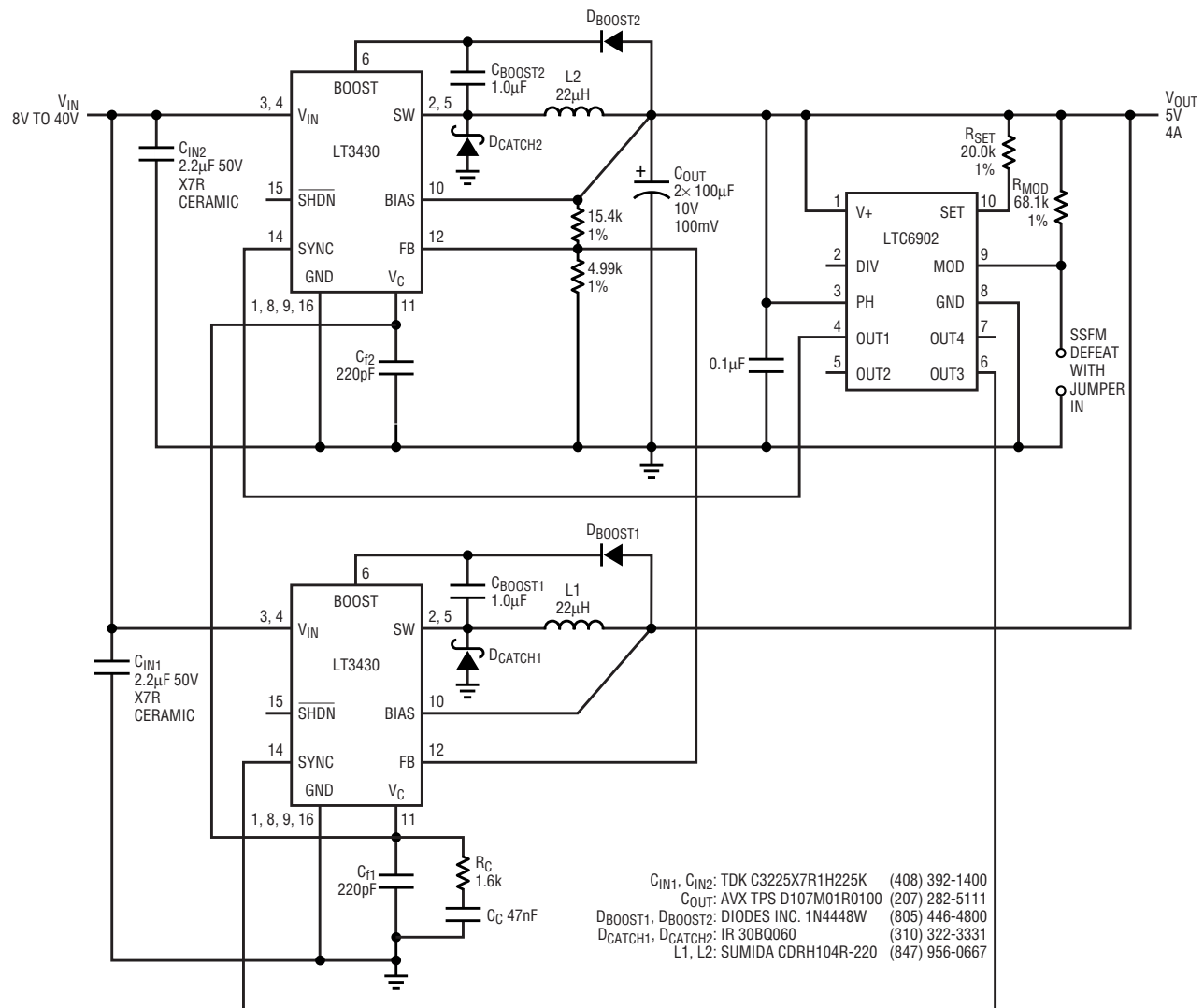


Figure 1. An 8V–40V input, 5V, 4A output DC/DC converter using two LT3430EFE buck regulators in parallel, synchronized at 250kHz using the LTC6902 multiphase oscillator featuring spread spectrum frequency modulation (SSFM).

rent, allowing the ripple current of one to counteract the ripple of the other, and thus minimize stress on the input and output capacitor energy banks. If, on the other hand, the two ICs are operated in phase, both ICs would demand current out of the capacitors, and send current into the capacitors at the same time on each cycle, effectively doubling the ripple of the circuit over using a single IC. The spread spectrum frequency modulation (SSFM) mode of the synchronization signal from the LTC6902 is set between 235kHz and 250kHz. This reduces the peak EMI that would be observed had the switching frequency been fixed at 250kHz. If a comparison of peak EMI is desired between SSFM mode and a fixed 250kHz frequency, grounding the modulation pin of the LTC6902 defeats SSFM mode.

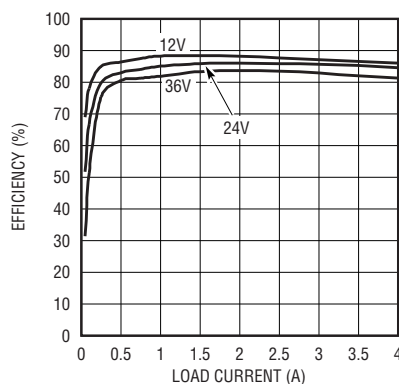



Figure 2. Efficiency of the parallel LT3430 circuit shown in Figure 1

Given the proper layout, at around 40%–60% duty cycle, the 2-converter circuit requires half of the capacitance that is required for a single high-current IC circuit with 4A load current. In applications that require a wide range of duty cycles, the double-IC

ripple is a little more than half of the single-IC ripple.

Over a wide range of loads, the optimal setup for thermal and efficiency considerations is when both ICs evenly share the load. By tying the outputs of the error amplifiers (V_C pins) together, the differences in the two error amplifier and feedback network gains are removed and the parts can work together within the tolerances of the inductors and modulator gains. Current sharing is approximately even in this design over the entire load current range.


Two separate 2.5A, 22 μ H power inductors are better than one much-larger 5A, 10 μ H inductor because their collective volume is smaller than the volume of the single inductor by a factor of $\sqrt{2}$, minimizing overall component height. 

Use a Current Feedback Amplifier's Low Current-Noise Input for Fast Photodiode Amplifier

by Glen Brisebois

Current feedback amplifiers offer high bandwidth with minimal power supply current draw. However, they are rarely used as transimpedance amplifiers in photodiode applica-

tions because of the high current noise associated with their inverting inputs. Figure 1 shows how to take advantage of the 400MHz (unity gain) bandwidth LT1396 Current Feedback

Op Amp without the disadvantage of the inverting input current noise. The photodiode is connected to the non-inverting input of amplifier A in a gain of 2. Amplifier A's output drives the inverting input of amplifier B through R1, selected for optimal time domain response. Feedback resistor R2 sets the transimpedance gain at 3.01k Ω while C1 compensates the photodiode capacitance. Risetime was measured at 6ns, 10% to 90%, and bandwidth was modeled in Pspice at 75MHz, assuming a 3pF photodiode. Output noise spectral density was measured at 18nV/ $\sqrt{\text{Hz}}$, consistent with the 6pA/ $\sqrt{\text{Hz}}$ non-inverting input current noise and the 3k Ω resistance. The MSOP package version of the dual LT1396 keeps board space usage to a minimum. 

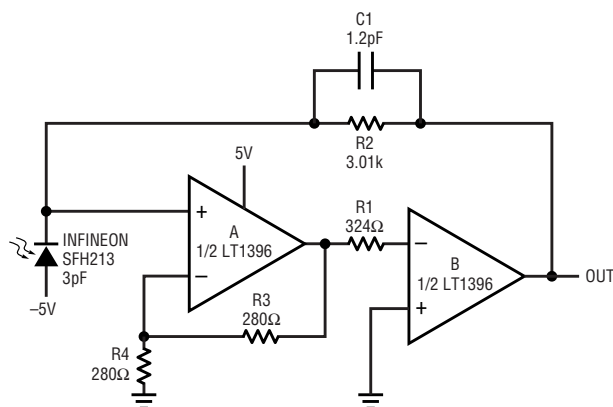


Figure 1. This circuit uses an LT1396 current-feedback op amp to save power in a photodiode application while avoiding inverting-input current noise.

For more information on parts featured in this issue, see <http://www.linear.com/go/ltmag>

New Device Cameos

Quadrature Demodulator Directly Converts 800MHz–1.5GHz Signals

The LT5516 is an 800MHz to 1.5GHz direct conversion quadrature demodulator optimized for high linearity receiver applications. It is suitable for communications receivers where an RF or IF signal is directly converted into I and Q baseband signals with bandwidth up to 260MHz. The LT5516 incorporates balanced I and Q mixers, LO buffer amplifiers and a precision, high frequency quadrature generator.

In an RF receiver, the high linearity of the LT5516 provides excellent spur-free dynamic range, even with fixed gain front end amplification. This direct conversion receiver can eliminate the need for intermediate frequency (IF) signal processing, as well as the corresponding requirements for image filtering and IF filtering. Channel filtering can be performed directly at the outputs of the I and Q channels. These outputs can interface directly to channel select filters (LPFs) or to a baseband amplifier.

The LT5516 is available in a 16-lead QFN 4mm x 4mm package with exposed pad.

Negative Hot Swap Controller Protects Boards from Slow Transient and Short-Circuit Faults

The LTC4214 negative Hot Swap™ controller provides three levels of in-rush and short-circuit protection for low voltage supplies in servers and mainframes.

Load current faults are controlled in three stages. Slight overloads of 1x to 2x trip the circuit breaker feature only if they persist beyond a user-programmable time delay. Overloads exceeding 2x rated current are actively limited, which maintains a safe power level in the MOSFET. Catastrophic short circuits that exceed the designed operating current by 4x or more activate a high-speed comparator to quickly

bring the current under control of the 2x active limiting loop. Separate soft-start circuitry limits inrush currents when a board is inserted or removed from the power bus.

Undervoltage and overvoltage monitors allow the user to define the operating voltage range. Owing to its versatile “floating supply” design the LTC4214 operates directly from –6 to –16V supplies, yet is easily adapted to control any negative voltage ranging all the way from zero up to the –36 to –75V telecom supply range.

Two configurations are available: the LTC4214-1 latches off after an overcurrent fault, and the LTC4214-2 includes an automatic retry feature. The LTC4214 is offered in the 10-pin MSOP package in both commercial and industrial temperature ranges.

Precision Op Amp in a 9mm² DFN Package

Linear Technology announces its first microvolt input precision op amp that is available in a 3mm x 3mm DFN leadless package. The LT6011 dual op amp combines low noise and precision input performance with low power consumption and rail-to-rail output swing.

Maximum input offset voltage is only 125µV (and an even lower 75µV in the standard SO-8 package). What's more, temperature, noise, input common mode voltage, or output swing have little effect on input precision. The typical offset voltage drift versus temperature is only 0.2µV/°C, and total noise in the 0.1Hz to 10Hz band is 0.4µV_{P-P}. The 135dB CMRR changes the offset by less than 0.2µV/V, while the 120dB Open-Loop Gain adds a maximum of 1µV/V to the input offset.

Supergain input transistors and base current cancellation limit the input bias current of this amplifier to 150pA.

The LT6011 can operate from any supply voltage between 2.7V and 36V, adding to its versatility. The amplifier outputs swing to within 40mV of either

supply rail, which is critical in low voltage applications.

Supply current is only 135µA per amplifier—important for battery powered and heat sensitive applications.

The LT6011 is specified to operate from –40°C to 85°C, and is available in an 8-lead SOIC as well as a tiny 3mm x 3mm leadless DFN package.

165MHz Op Amps Offer Rail-to-Rail Input and Output, and Ultralow, 0.95nV/√Hz Noise

The LT®6200/LT6201 are single and dual ultralow noise, rail-to-rail input and output unity gain stable op amps that feature 0.95nV/√Hz noise voltage. These amplifiers combine very low noise with a 165MHz gain bandwidth, 50V/µs slew rate and are optimized for low voltage signal conditioning systems. A shutdown pin reduces supply current during standby conditions and thermal shutdown protects the part from overload conditions.

The LT6200-5/LT6200-10 are single amplifiers optimized for higher gain applications resulting in higher gain bandwidth and slew rate. The LT6200 family maintains its performance for supplies from 2.5V to 12.6V and are specified at 3V, 5V and ±5V.

For compact layouts the LT6200/LT6200-5/LT6200-10 are available in the 6-lead ThinSOT™ and the 8-pin SO package. The dual LT6201 is available in an 8-pin SO package with standard pinouts as well as a tiny, dual fine pitch leadless package (DFN). These amplifiers can be used as plug-in replacements for many high speed op amps to improve input/output range and noise performance.

Dual DC/DC Controller Brings 2-Phase Efficiency to High Output Voltage Applications

The LTC3727-1 is a high performance dual step-down switching regulator controller that drives all N-channel synchronous power MOSFET stages. The constant frequency, current mode architecture allows phase-lockable operating frequencies up to 550kHz. Power loss and noise due to the ESR of the input capacitors are minimized

by operating the two controller output stages out of phase.

The LTC3727-1 is capable of output voltages up to 14V and currents as high as 20A, making it suitable to many automotive applications where 8.5V or 12V outputs are common. It is functionally the same as the LTC3727 but without the short-circuit latch-off feature of that device.

LTC3727-1 is available in a small 28-Lead SSOP package and the even smaller (5mm × 5mm) QFN package, which also offers extremely low thermal resistance.

Dual Smart Battery Charger Extends Battery Run Times; Cuts Charge Times in Half

The LTC1760 Smart Battery System Manager is a highly integrated level 3 battery charger and selector intended for products using dual smart batteries. Three SMBus interfaces allow the LTC1760 to servo to the internal voltage and currents measured by the batteries while allowing an SMBus Host to monitor either battery's status. Charging accuracy is determined by the battery's internal voltage and current measurement, typically better than ±0.2%.

A proprietary PowerPath™ architecture supports simultaneous charging or discharging of both batteries. Typical battery run times are extended by up to 10%, while charging times are reduced by up to 50%. The LTC1760 automatically switches between power sources in less than 10µs to prevent power interruption upon battery or wall adapter removal.

Thermistors on both batteries are automatically monitored for temperature and disconnection information (SafetySignal). 

LTC3010, continued from page 20

how long they last, and how often they occur. Looking closer at the application above would show that the transient spikes of 72V on the input can last as long as 5ms and occur every 100ms. The load current rises from 5mA to 50mA for a 50ms period as the unit is polled and transmits its data. This polling only occurs once every 250ms.

Most designers think in time frames of a few microseconds or faster, especially as clock speeds increase. Even in the application discussed here, timing is in the range of milliseconds. Thermal timing, on the other hand, tends to be much slower. Average thermal time constants for a surface mount part soldered onto a PC board are usually several seconds. The thermal time constant should be adjusted to reflect the device package and the thermal mass that is attached to it on the PC board, but these factors certainly do not alter thermal time constants by orders of magnitude. The upshot of this is that for an application as shown above, power dissipation can be averaged over a longer time frame, such as 500ms. There is no worry of the device exceeding the maximum junction temperature and going into thermal shutdown during short transient events, simply because nothing has time to heat up in these events.

Over a 500ms period of time, the unit will be polled twice, with 20% (100ms) of the time spent providing

50mA of load current instead of 5mA. The input is at 48V for 18% (90ms) of the time, and the other 2% (10ms) can be at 72V during a transient spike. The remaining 80% (400ms) of the time is spent at 5mA of load current, split so that 77% (385ms) is spent at 48V input, the other 3% (15ms) at 72V in. The breakdown for power dissipation is as follows:

- 18% of the time at 48V, 50mA (unit polled, no transient on input)
- 2% spent at 72V, 50mA (unit polled, transient spike on input)
- 77% spent at 48V, 5mA (unit quiescent, no transient)
- 3% spent at 72V, 5mA (unit quiescent, transient input)


From here it is possible to calculate the average power dissipation over a 500ms time frame:

$$\begin{aligned} P &= 18\% \cdot (48 - 5) \cdot 0.05 \\ &\quad + 2\% \cdot (72 - 5) \cdot 0.05 \\ &\quad + 77\% \cdot (48 - 5) \cdot 0.005 \\ &\quad + 3\% \cdot (72 - 5) \cdot 0.005 \\ &= 0.39 + 0.07 + 0.17 + 0.01 \\ &= 0.64W \end{aligned}$$

For a board with worst-case thermal layout (~40°C/W), this still translates to only a 26°C rise in junction temperature above ambient. This allows for operating the LT3010 at almost 100°C ambient, a much better proposition than trying to maintain a room temperature maximum ambient.

Figure 4 shows the maximum output current that can be achieved with the LT3010, assuming a junction-to-ambient thermal resistance of either 35°C/W or 40°C/W and a maximum ambient temperature of 50°C. For a junction-to-ambient thermal resistance of 35°C/W, the maximum output current at a 70V differential (input-to-output) voltage is 30mA continuous. This can be treated the same as a 50mA load operating at a 60% duty cycle. For different values of expected thermal resistance or ambient temperature, these curves can be adjusted accordingly.

Conclusion

The LT3010 offers exceptional performance in a small package. By holding off high input voltages, localized low power applications can be easily created without external pre-regulation schemes or complex switching supplies. Low quiescent current, and a shutdown option, minimize power draw. A stable output is available with a wide range of output capacitors, including small ceramics. Internal protection circuitry in the LT3010 eliminates the need for external protection diodes, further saving space and lowering cost. The thermally enhanced 8-lead MSOP package offers the one last thing needed for this sort of design—low thermal resistance. 

DESIGN TOOLS

New! 2003 Databooks

Linear Technology is pleased to announce the availability of seven new databooks organized by product family. This set (described below) supersedes all previous LTC databooks. Each databook contains all related product data sheets, selection guides, QML/space information, package information, appendices, and a complete reference to all of the other family databooks.

For more information, or to obtain any of the new databooks, contact your local sales office (see the back of this magazine), or visit www.linear.com.

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Linear Applications Handbook, Volume III — This 976-page handbook includes Application Notes 55 through 69 and Design Notes 70 through 144. Subjects include switching regulators, measurement and control circuits, filters, video designs, interface, data converters, power products, battery chargers and CCFL inverters. An extensive subject index references circuits in LTC data sheets, design notes, application notes and *Linear Technology* magazines.

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Linear Direct Online Store — The Linear Online Store at www.linear.com now offers a simple way to order LTC products factory direct. The new store accepts major credit cards and allows customers to create personalized accounts where they can check order history, shipment information and reorder products. Also, the maximum quantity per order has increased to 500.

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NEW! Power Management & Wireless Solutions for Handheld Products — The solutions in this product selection guide solve real-life problems for cell phones, digital cameras, PDAs and other portable devices. Circuits are shown for Li-Ion battery chargers, battery managers, USB support, system power regulation, display drivers, white LED drivers, photoflash chargers, DC/DC converters, SIM and smart card interfaces, photoflash chargers, and RF PA power supply and control. All solutions are designed to maximize battery run time, save space and reduce EMI where necessary—important considerations when designing circuits for handheld devices.

Software

SwitcherCAD™ III/LTC SPICE — LTC SwitcherCAD III is a fully functional SPICE simulator with enhancements and models to ease the simulation of switching regulators. This SPICE is a high performance circuit simulator and integrated waveform viewer, and also includes schematic capture. Our enhancements to SPICE result in much faster simulation of switching regulators than is possible with normal SPICE simulators. SwitcherCAD III includes SPICE, macromodels for 80% of LTC's switching regulators and over 200 op amp models. It also includes models of resistors, transistors and MOSFETs. With this SPICE simulator, most switching regulator waveforms can be viewed in a few minutes on a high performance PC. Circuits using op amps and transistors can also be easily simulated. Download at www.linear.com

FilterCAD™ 3.0 — FilterCAD 3.0 is a computer aided design program for creating filters with Linear Technology's filter ICs. FilterCAD is designed to help users without special expertise in filter design to design good filters with a minimum of effort. It can also help experienced filter designers achieve better results by playing "what if" with the configuration and values of various components and observing the results. With FCAD, you can design lowpass, highpass, bandpass or notch filters with a variety of responses, including Butterworth, Bessel, Chebychev, elliptic and minimum Q elliptic, plus custom responses. Download at www.linear.com

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