

Complete Dual-Channel Receiver Combines 14-Bit, 125Msps ADCs, Fixed-Gain Amplifiers and Antialias Filters in a Single 11.25mm × 15mm μ Module Package

by Todd Nelson

Introduction

Extensive hands-on applications experience is a prerequisite for any designer hoping to take full advantage of an ADC's capabilities when sampling high dynamic range signals in multichannel IF-sampling or in I/Q baseband communications channels. An intimate knowledge of the amplifier output stage and ADC front end is required to match the impedances, while careful attention to layout is required to minimize coupling of the digital outputs into the sensitive analog input.

In fact, good layout is paramount to maintaining ADC performance, yet ever more demanding market requirements call for smaller designs and higher channel density, which exacerbate layout issues. These design requirements can challenge even the most seasoned engineer if

his expertise lies in the RF or digital worlds.

The LTM9002 dual-channel, IF/baseband receiver harnesses years of applications design experience and squeezes it into an easy-to-use 11.25mm × 15mm μ Module package. Inside the package is a high performance dual 14-bit ADC sampling up to 125Msps, antialiasing filters, two fixed gain differential ADC drivers and a dual auxiliary DAC. By combining these components, the LTM9002 eliminates the burden of input impedance matching, filter design, gain/phase matching, isolation between channels and high frequency layout, dramatically improving time to market. Even in this small package, the LTM9002 guarantees high performance that will enhance many communications and instrumentation applications.

Multichannel ADC Applications

Multichannel applications have several unique requirements, such as channel matching in terms of gain, phase, DC offset, and channel-to-channel isolation. Gain and phase errors directly affect the demodulation of the I and Q channels. And since direct conversion receivers are typically DC-coupled, DC offset limits the dynamic range of the receiver. Multiple-input, multiple-output (MIMO) systems depend on multiple receiver channels all receiving the same signal while detecting the slight variations caused by multipath delays so gain and phase errors affect these systems as well. Like I/Q receivers, diversity receivers require excellent isolation between channels because crosstalk appears as noise corruption and can be more difficult to suppress

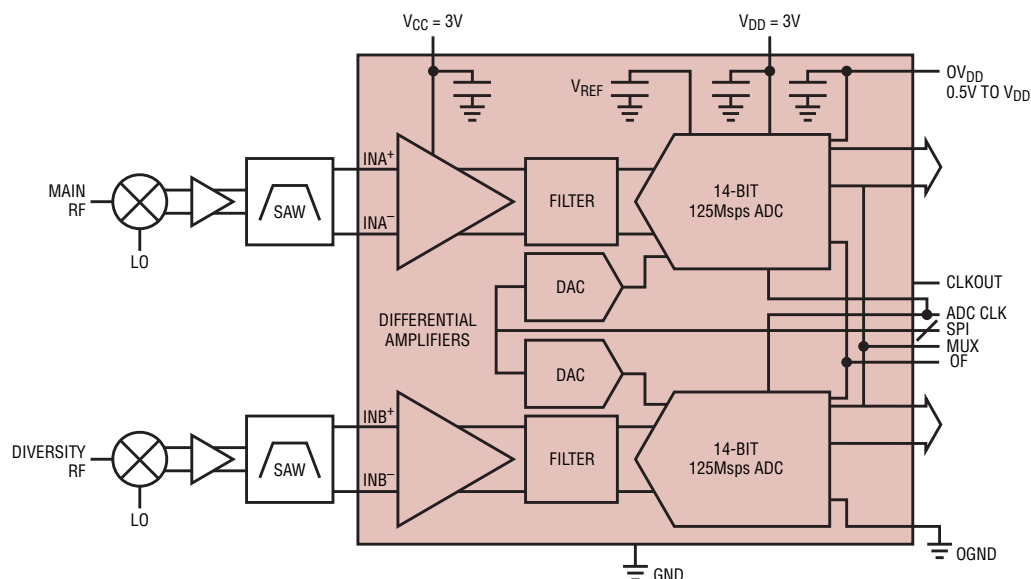


Figure 1. LTM9002 used for a Main/Diversity receiver.

with digital filtering. Clearly, channel matching and channel isolation of the ADC and driver circuits directly impact system-level performance. For many multichannel applications, these errors cannot be corrected in the digital domain.

Performance

The LTM9002 achieves 66dB Signal to Noise Ratio (SNR) and 74dB Spurious Free Dynamic Range (SFDR) at 140MHz input frequency. Figure 2 shows the FFT under these conditions. SNR is a function of the ADC and amplifier performance as well as the amplifier gain and filter bandwidth. The inherent amplifier noise is proportional to the voltage gain; therefore, the 26dB amplification increases the amplifier noise by 20 times whereas 8dB amplification would only increase the noise by 2.5 times. Likewise, the amplifier noise (in nV/\sqrt{Hz}) increases with the square of the filter bandwidth. It is important to remember these relationships when assessing the entire signal chain.

For multichannel applications, channel-to-channel matching and isolation are important considerations. The LTM9002 achieves 90dB isolation at 140MHz input frequency despite the small form factor. The overall gain is typically 26dB on the default span setting and varies just 0.1dB between the two channels. The 12-bit auxiliary DAC can be configured to adjust the span by 61 μ V per step using the circuit in Figure 3.

Another important performance metric is printed circuit board (PCB) area efficiency. Here, the LTM9002 excels. The LTM9002 requires no external components—no supply bypass capacitors, no passive filtering, no impedance matching or translating components. In many IF-sampling applications, gain can be obtained through transformers, but they are often large and difficult for automated assembly equipment to mount. In DC-coupled applications, amplifiers are required as ADC drivers, along with their associated antialias filter network. It is not uncommon for the entire IF/baseband receiver system to

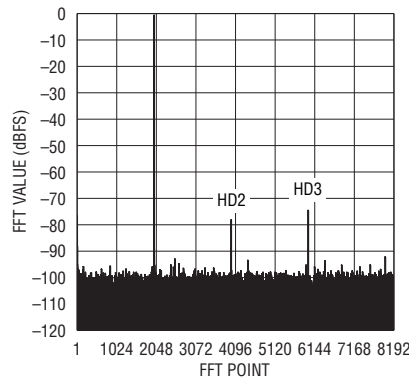


Figure 2. FFT showing LTM9002 AC performance with 140MHz input frequency.

consume two square inches of board area (approximately 25mm \times 50mm). None of this external circuitry is required with the LTM9002 so it requires only about one-quarter of a square inch (11.25mm \times 15mm), better by a factor of eight.

Attributes and Configurations

The μ Module construction allows the LTM9002 to mix standard ADC and amplifier components regardless of their process technology and match them with passive components for a particular application. The μ Module receiver consists of wire-bonded die, packaged components and passives mounted on a high performance, 4-layer, Bismaleimide-Triazine (BT) substrate. BT is similar to other laminate substrates such as FR4 but has superior stiffness and a lower coefficient of thermal expansion.

The LTM9002-AA utilizes a dual, 14-bit, 125Msps ADC, two 26dB fixed-gain amplifiers and also includes a 12-bit dual DAC configured for full-scale span adjustment as shown in Figure 1. Internal antialias filters limit the input frequency to less than 170MHz. The amplifiers present a 50 Ω differential input impedance and an input range of ± 50 mV, or -16 dBm. This default span is set by connecting the SENSE pin to V_{DD} , and can be adjusted in three ways. For a -3 dBm lower span, the SENSE pin can be connected to 1.5V. By connecting SENSE to V_{DD} or 1.5V, the internal reference is used. An external reference can be used by applying 0.5V–1.0V to the SENSE pin. The auxiliary DAC offers a final option for selecting the range. Alternately, fine adjustments to the span, such as balancing the gain of the two channels, can be made with external references or the auxiliary DAC.

Multiple power saving modes include independently disabling either amplifier or the ADC. The ADC has two shutdown states: NAP and SLEEP modes. In NAP mode, the internal reference remains biased so that conversions can resume within 100 clock cycles upon start-up. In SLEEP mode the reference is shut down and start-up takes 1 μ s or more. A clock duty cycle stabilizer feature is available and an output clock signal is provided for accurately latching the output data. The two channels can be

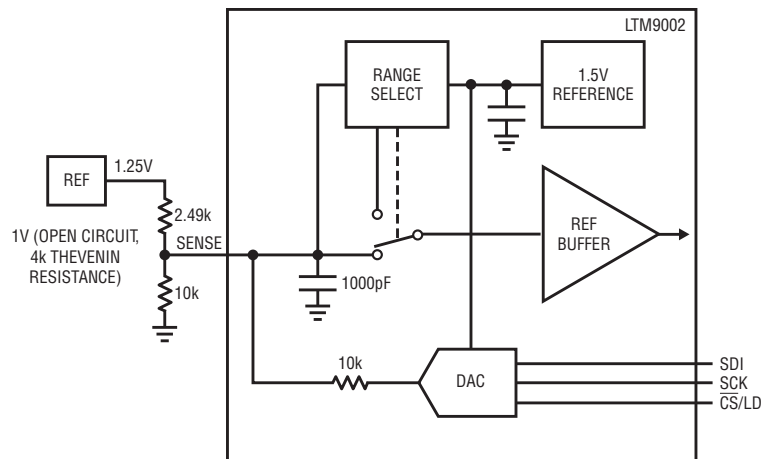


Figure 3. Using an external reference and the internal auxiliary DAC for span adjustment.

output on separate parallel busses or multiplexed onto a single parallel bus to save processor pins.

Interfacing to the Analog Inputs

The analog inputs of the LTM9002 present a differential 50Ω resistive input impedance, which in most cases exactly matches the signal path. The input common mode level should be approximately $V_{CC}/2$. Traditionally, the input of an ADC requires considerable care in terms of drive current, settling time and response to the nonlinear characteristics of sample-and-hold switching. For lowest distortion performance, the common mode level at the ADC inputs must be optimized for the particular ADC front-end; for best signal-to-noise (SNR) performance, the signal swing must utilize the maximize ADC input range. All this is taken care of within the LTM9002.

Interfacing to the Digital Outputs

The LTM9002 uses standard CMOS output buffers that switch from OV_{DD}


to OGND. OV_{DD} can range from 0.5V to 3.6V, accommodating many different logic families and OGND can be as high as 1V. Because the LTM9002 supplies are internally bypassed, no local supply bypass capacitors are required. The power supply for the digital output buffers should be tied to the same supply that powers the logic being driven. For example, if the converter drives a DSP powered by a 1.8V supply, then OV_{DD} should be tied to that same 1.8V supply. Lower OV_{DD} voltages also help reduce interference from the digital outputs to the analog or clock circuitry. OV_{DD} and OGND are isolated from the ADC power and ground. An internal resistor in series with the output makes the output appear as 50Ω to external circuitry and may eliminate the need for external damping resistors.

Power Supplies and Bypassing

The LTM9002 requires a 3.0V supply. To optimize performance for each block within the LTM9002, multiple supply pins are used. Internally, each supply is bypassed to ground very close to the die to minimize coupled noise.

A common problem with traditional ADC board layouts is long traces from the bypass capacitors to the ADC degrade system performance. The bare die construction with internal bypass capacitors in the LTM9002 provides the closest possible decoupling and eliminates the need for external bypass capacitors.

Conclusion

Multichannel ADC applications need good channel-to-channel matching and isolation without consuming valuable board space. Driving high performance ADCs is challenging enough without the matching, isolation and board space constraints. The LTM9002 integrated dual IF/baseband receiver subsystem manages to address all of these requirements while eliminating the design task of mating an ADC and its driver. By integrating the passive filtering and supply bypassing, the overall size is dramatically smaller than otherwise possible with discrete implementations. The LTM9002's μ Module packaging is itself developed to maximize the performance of the integrated components. 

LTC4350, continued from page 9

Specifics of Power System Design With a Bidirectional Energy Flow Power Supply

Certain switcher topologies, such as a synchronously rectified buck converter, permit large, uncontrolled reverse current if the output voltage is forced to a potential that is higher than the regulation point. In addition, an unwelcome transient can occur when one LTC4350 power channel is added to an operating system. Due to the difference between the initial power supply output voltage and the operating output voltage (usually 200mV–300mV), significant negative current can be induced in the newly added power supply. This current can disable the LTC4350 if the voltage drop at R_{SENSE} exceeds 50mV. After the negative current drops, the LTC4350 goes into its initial start-up cycle and the process may repeat indefinitely. This current can also damage the

power supply, as it does not have the ability to transform energy to the primary side.

An equivalent output power stage circuit that exemplifies this case is shown in Figure 10.

To reduce or eliminate negative current, it is necessary to reduce the difference between voltages when the MOSFET switch is first turned on. The newly activated power supply output voltage starts to increase when the LTC4350 load share capability is brought into operation. The LTC4350 is designed to launch the load share mechanism when the gate pin voltage exceeds V_{CC} by 4V but the MOSFET's gate threshold is in the range of 1V to 5.5V. To synchronize both events, activating load share capability and turning on the power switch, the MOSFET threshold voltage must be higher than or equal to 4V. This is easily satisfied by using a sub-logic

level MOSFET and placing a low knee current Zener diode (Central Semiconductor's CMPZ4676-CMPZ4682) in the MOSFET gate circuit.

An alternative solution involves disabling synchronized rectification until the LTC4350 STATUS pin signal is low and load share capability is active, but this method is restricted by the power supply controller's ability to power up non-synchronously in a condition of unidirectional energy flow.

Conclusion

The calculations and methods described here show how the LTC4350 can be used to build a stable and accurate load share power system with any kind of power supply, including a mix of power modules. The LTC4350 also has the unique feature of operating with bidirectional power flow converters. 