

4-Channel I²C Multiplexer Provides Address Expansion, Bus Buffering and Fault Management

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Introduction

As data processing, mass storage and communications systems have grown, the size and complexity of the subsystems employed to transfer information such as temperature, fan speed, system voltages and Vital Product Data (VPD, board identification, for example) have grown in proportion. This information is most often transferred through two-wire serial buses, such as I²C or SMBus.

Several practical problems can arise in the design of these systems, especially as they become large. First, many devices, such as Small Form Factor Pluggable optical modules (SFPs) have hard-wired I²C addresses, preventing the use of multiple such devices due to address conflict. Second, as the variety of devices increases and more I/O cards are hot-swapped into and out of a system, the likelihood of an I²C device becoming confused and holding the bus low increases. Third, bus timing specifications become difficult to meet with increasing equivalent bus capacitance. In addition to these large system issues, cycling power whenever a new I/O card is installed is not an option in uninterruptible systems of any size.

The LTC4306 4-channel 2-wire bus multiplexer/switch with bus buffers addresses all of these issues (see Table 1 for a short list of features). A master on the upstream 2-wire bus (SDAIN, SCLIN) can connect to any combination of downstream buses through the LTC4306's bus buffers and multiplexers/switches. As a result, the same device address can be used on multiple downstream buses. The buffers provide capacitive isolation between the upstream and downstream buses, allowing for partitioning of the system loading. Rise time accelerators further aid in overcoming capacitance limitations. Stuck Low Timeout circuitry

Table 1. Some features of the LTC4306	
Feature	Benefits
4 Selectable Downstream Buses	<input type="checkbox"/> Maximum flexibility of bus configurations <input type="checkbox"/> Nested addressing when used a MUX
Disconnect from Stuck Bus	<input type="checkbox"/> Frees masters to resume upstream communications
2-Wire Bus Buffers	<input type="checkbox"/> Breaks up capacitance
Buffer Supply Independence	<input type="checkbox"/> Level-shifting: 2-Wire buses can be pulled up to supply voltages ranging from 2.2V to 5.5V, independent of the LTC4306 V _{CC} voltage
Slew Limited Rise Time Accelerators	<input type="checkbox"/> Aid in reducing rise time <input type="checkbox"/> Allow larger bus pull-up resistors for better noise margin <input type="checkbox"/> Drive long cables with no reflection issues
2-Wire Bus Hot Swap	<input type="checkbox"/> Prevents 2-wire bus corruption during live insertion and removal from backplane
Fault Reporting	<input type="checkbox"/> Helps master find and resolve system faults efficiently
Mass Write Address	<input type="checkbox"/> Issue one command to all LTC4306s at the same time

disconnects the upstream bus from the downstream buses when the bus is low for a programmed length of time, freeing the upstream bus to resume communications. Finally, any of the LTC4306's 2-wire bus pins can be hot-swapped into and out of a live system without corrupting it. The LTC4306 works with supply voltages ranging from 2.7V to 5.5V.

General Operation

A block diagram for the LTC4306 is shown in Figure 1, and a description of its register contents is given in Table 2. The UVLO comparator prevents the LTC4306 from receiving commands until the V_{CC} voltage rises above 2.5V (typical). This ensures that the LTC4306 does not try to function until it has sufficient bias voltage. When ENABLE is brought below 1V, the LTC4306 is reset to its default

high-impedance state and ignores any attempts at communication on its 2-wire buses. When ENABLE is brought back above 1.1V, masters may resume communication with the LTC4306.

Disconnecting from a Stuck Bus

The LTC4306 disconnects the upstream bus from the downstream buses when the 2-wire bus is stuck low for a programmed period of time. Masters are then free to resume communications on the upstream bus, assuming the source of the problem resides on a downstream bus. The Stuck Low Timeout circuitry monitors the two common internal nodes of the downstream SDA and SCL switches and runs a timer whenever either of the internal node voltages is below 0.52V. The timer is reset whenever both internal voltages are above 0.6V.

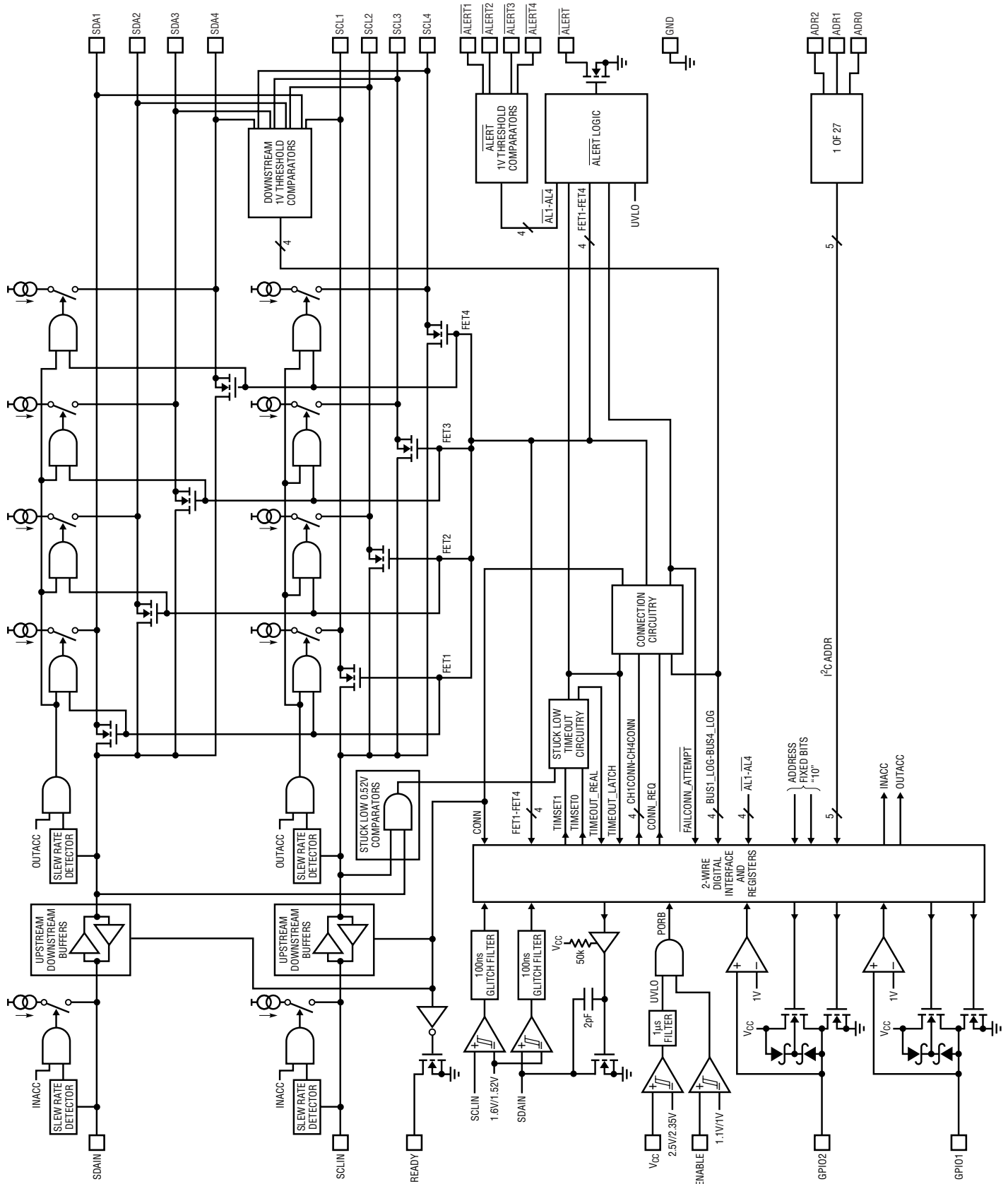


Figure 1. A block diagram of the LTC4306

Table 2. LTC4306 Register Contents

Register	Contents
0	Gives logic state of ALERT1#–ALERT4# pins, and present and latched states of Stuck Low Timer. Indicates whether upstream bus is connected to any downstream buses and whether any failed attempts at connection occurred.
1	Activates/deactivates upstream and downstream rise time accelerators. Writes and reads logic states of GPIO pins.
2	Configures behavior mode of GPIOs. Enables/disables Mass Write feature. Programs Stuck Low Time. Sets requirements on downstream bus logic states for connection to upstream bus.
3	Connects upstream bus to any combination of 4 downstream buses. Masters can read logic state of the downstream buses before connecting to them.

Using register 2, masters can set times of 7.5ms, 15ms, or 30ms, or they can choose to disable the timeout feature.

2-Wire Bus Buffers and Multiplexer Switches Provide Capacitance Buffering and Level Shifting

Masters write to register 3 to connect to any combination of downstream channels. The 2-Wire Bus Buffers provide capacitive isolation between the upstream SDAIN, SCLIN bus and the downstream buses. Thanks to this feature, masters can include LTC4306s at various points in their system to break one large bus into several smaller buses. When any downstream bus is connected, the LTC4306 allows the READY pin to be pulled to a logic high by an external resistor.

By default, the LTC4306 only connects to downstream buses that are high. Attempts to connect to a low downstream bus fail and cause the LTC4306 to pull the ALERT# pin low to indicate a fault. Masters can override this feature by writing to register 2 and instructing the LTC4306 to execute connection commands regardless of the downstream logic state.

The upstream and downstream bus pull-up supply voltages can range from 2.2V to 5.5V, independent of the LTC4306 V_{CC} voltage—the LTC4306 therefore provides level-shifting between buses having different pull-

up voltages. To guarantee proper operation when connecting multiple downstream channels at once, make sure that the LTC4306 V_{CC} voltage is less than or equal to all downstream pull-up voltages to maintain channel-to-channel isolation during logic highs.

Rise Time Accelerators Reduce Rise Times

By writing to Register 2, masters may activate the rise time accelerators on the upstream bus, downstream bus, neither or both. When activated, the accelerators turn on in a controlled manner and source current into the buses to make them rise at a typical rate of 100V/ μ s during positive bus transitions. These strong pull-up currents allow users to build large, heavily capacitive systems while still meeting rise time specifications, but are also slew limited for driving long

cables. In addition, given the strong drive provided by the accelerators, system designers can choose large resistor pull-ups to minimize bus logic low voltages, thereby maximizing logic low noise margin.

Fault Information Aids Diagnosis

After a fault occurs and the LTC4306 pulls the ALERT# pin low, the LTC4306 works with the master to resolve the fault simply and quickly. The LTC4306 stores specific fault information in read-only register 0. Faults stored include a stuck low bus, faults on the downstream buses, and a failed attempt to connect to a downstream channel.

If the source of the problem is on a connected downstream bus, the master can communicate directly with the offending device. In this case, the LTC4306 acts transparently, with the master and offending device communicating directly via the LTC4306's bus buffers.

In all other cases, the LTC4306 communicates with the master on the upstream 2-wire bus to resolve the fault. After the master broadcasts the Alert Response Address (ARA), the LTC4306 responds with its address on SDAIN and releases ALERT#. The LTC4306 also releases ALERT# if it is addressed by the master. The master determines the source of the fault by reading register 0. After the master solves the problem, it writes a dummy byte to register 0 (which is a read-only register) to reset the fault detection circuitry.

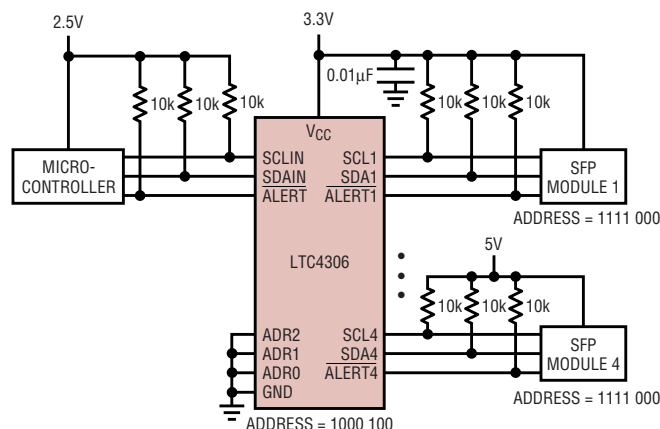


Figure 2. A circuit illustrating the nested addressing and level shifting features of the LTC4306

Nested Addressing and Level-Shifting

The circuit shown in Figure 2 illustrates the nested addressing, level-shifting and capacitance buffering features of the LTC4306. For simplicity, only channels 1 and 4 are shown. Note that the backplane, card 1 and card 4 are pulled up to three different supply voltages. Also, the SFP modules have the same address, but no conflict occurs as long as channels 1 and 4 are never active at the same time.

2-Wire Bus Hot Swapping with the LTC4306 Located on the Backplane

Figure 3 shows a circuit with the LTC4306 located on the backplane and an I/O card plugging into downstream channel 4. Again, channels 2 and 3 are omitted for simplicity. Before plugging and unplugging the card, make sure that channel 4 is not connected to the upstream bus, so that any transaction occurring on the upstream bus is not disturbed. The pull-up resistors on

SDA4 and SCL4 are shown on the backplane, but they may be located on the I/O card, as long as masters on the backplane do not connect to channel 4 when no card is present. The pull-up resistor on ALERT4# must be located on the backplane, to prevent false fault reporting when the I/O card is not present.

2-Wire Bus Hot Swapping with the LTC4306 Located on an I/O Card

In Figure 4 the LTC4306 resides on the edge of an I/O card having four separate downstream buses. Connect a 200k Ω resistor from ENABLE to ground and make ENABLE the shortest pin on the connector. This ensures

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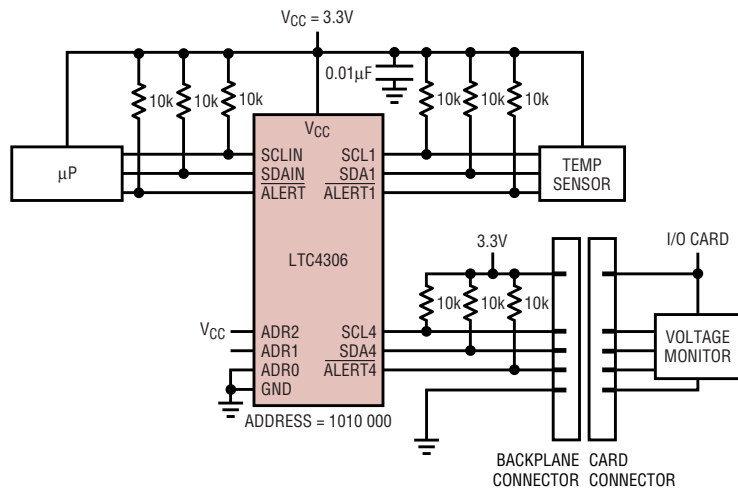


Figure 3. A 2-Wire Bus hot-swapping application circuit with the LTC4306 resident on the backplane

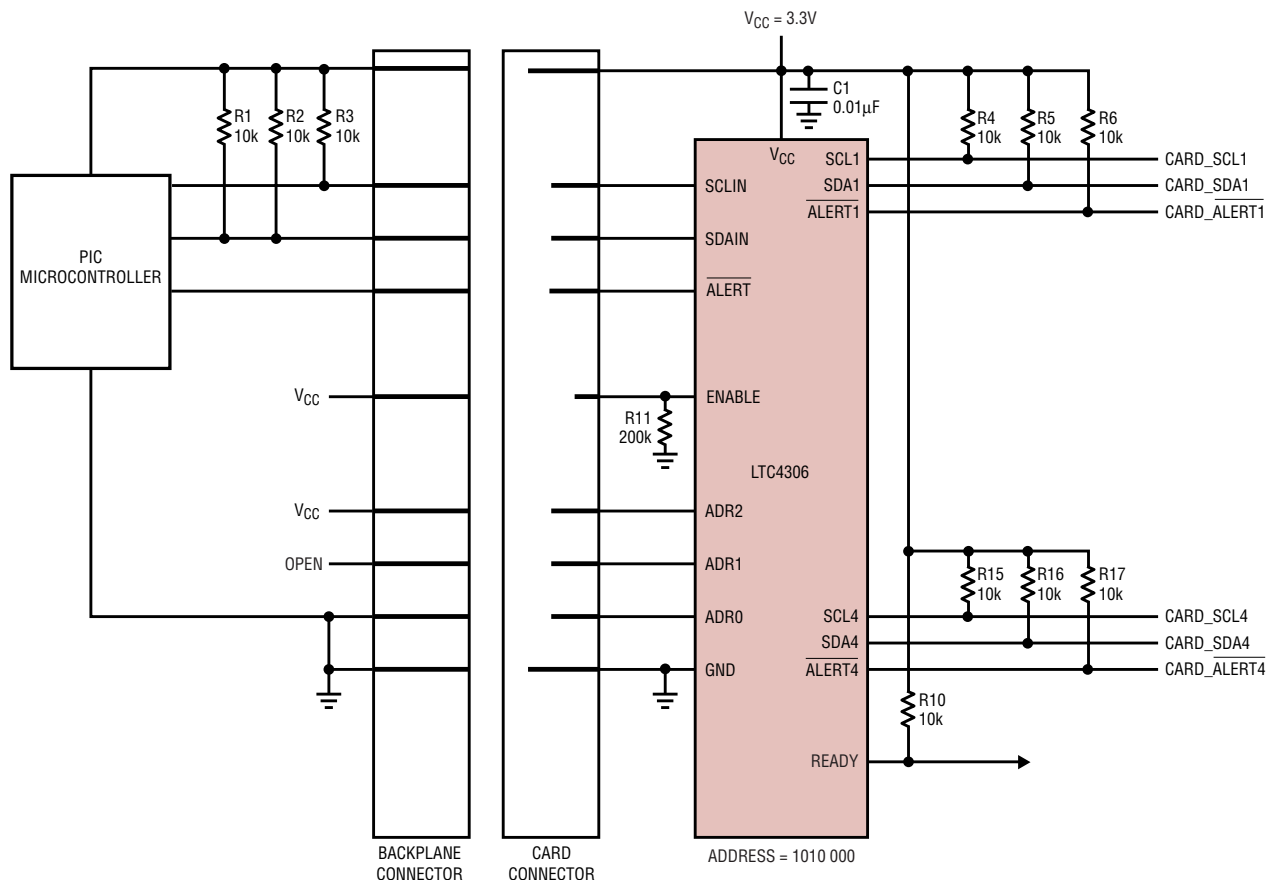


Figure 4. A 2-Wire Bus hot-swapping application circuit with the LTC4306 resident on the I/O card

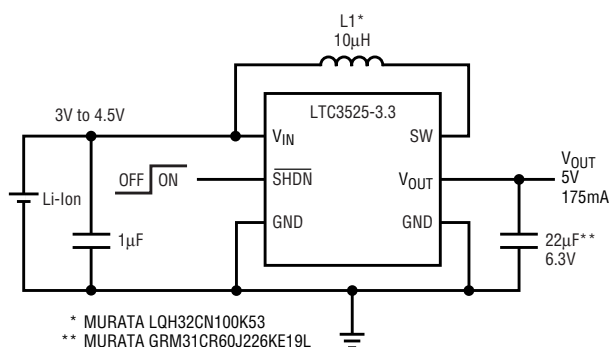


Figure 5. Li-ion to 5V converter delivers 175mA of load current with <0.5% ripple

Figure 3. Note that the charge pump design requires an input voltage of at least 1.7V to generate a regulated 3.3V output. Comparable inductor-based solutions require larger packages and more external components, making them unsuitable to applications where board space is at a premium, or too expensive for cost sensitive applications.

Single Cell to 3.3V Converter with 1mm Profile

A single alkaline or nickel cell to 3.3V converter, using the LTC3525-3.3, is shown in Figure 4. This application uses an inductor and output capacitor chosen to achieve a 1mm profile. It delivers 60mA of load current from a single cell, and 140mA from two cells, while fitting into a 5mm × 7mm footprint. The ability of the converter to operate with input voltages below 1V allows it to use all the available energy in the battery, and also prevents the converter from shutting off in the event that a load transient causes a momentary drop in input voltage.

Li-ion/3-Cell to 5V Converter Delivers Over 175mA with Low Output Ripple

The LTC3525 has been designed for very low output ripple with minimal output capacitance. In most applications, a 10µF ceramic capacitor will yield less than 1% peak-to-peak output ripple. By using a 22µF capacitor, the output ripple can be reduced to less than 0.5% of V_{OUT} , making it suitable for many noise sensitive applications that previously required a larger, more expensive fixed frequency converter.

The circuit in Figure 5, which occupies a space of just 6mm × 6mm, supplies 5V at 175mA or more from a Li-ion battery (or three alkaline or nickel cells). With a 22µF output capacitor, the output ripple is only 22mV_{P-P} at light load, and less than 50mV_{P-P} at full load, as shown in Figure 6. The efficiency peaks at 93% and remains above 85% over three decades of load current, as shown in Figure 7. This solution could also be used to provide 5V at 200mA in a 3.3V powered system. The entire solution fits in a 1.8mm profile.

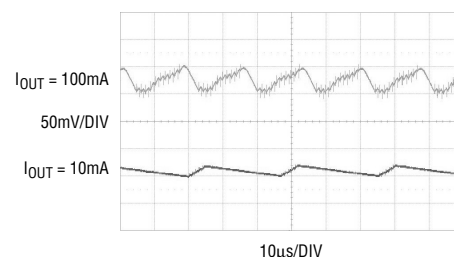


Figure 6. Output voltage ripple of the 5V converter at min and max load

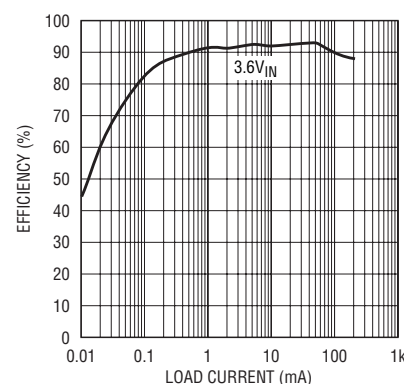


Figure 7. Efficiency versus load for the Li-ion to 5V converter

Conclusion

Many of today's battery powered portable devices, such as MP3 players, medical instruments and digital cameras can benefit from the small size, simplicity and extended battery life offered by the LTC3525. Its tiny, low profile SC70 package and minimal external part count make it a viable, high performance alternative to less efficient charge pump designs. Its 400mA switch current and low output ripple allow it to replace more expensive fixed frequency converters in cost-sensitive applications.

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that ENABLE remains at a constant logic low while all other pins are connecting, so that the LTC4306 remains in its default high impedance state and ignores connection transients on SDAIN and SCLIN during connection. In addition, make the ALERT# connector pin shorter than the V_{CC} pin, so that V_{CC} establishes solid contact with the I/O card pull-up supply pin and powers the pull-up resistors on ALERT1#–ALERT4# before ALERT#

makes contact. When disconnecting, ENABLE breaks contact first, resetting the LTC4306 to its default state, so that it causes minimal disturbance on the SDAIN and SCLIN bus as the card disconnects.

Conclusion

The LTC4306 eases the practical design issues associated with large 2-wire bus systems. It serves as a multiplexer to provide nested addressing. It disconnects buses when they are

stuck low. It breaks a large capacitive bus into smaller pieces and allows I/O cards to be hot-swapped into and out of live systems. It logs faults, reports to the master, and works with the master to resolve faults efficiently.

