

Negative High Voltage Hot Swap Controllers Incorporate an Accurate Supply Monitor and Power Module Sequencing

by Kevin Wong

Introduction

When a circuit board is inserted into a live backplane slot, discharged supply bypass capacitors on the board can draw large transient currents from the system supplies. In high-voltage systems like the -48V backplanes prevalent in high reliability telecom systems, such transients can reach hundreds of amps and damage connector pins, PCB traces and board components. In addition, current spikes can cause voltage glitches on the power bus, causing other boards in the system to reset. This is particularly unacceptable in telecom systems where the ability to safely Hot Swap modules is a primary system requirement.

The LTC4253A and LTC4253A-ADJ facilitate safe board insertion and removal from a live backplane by applying power in a controlled manner. Running off a simple, fast responding

shunt regulated supply that allows very high voltage operation, they are uniquely suited for applications on the -48V bus.

User programmable, high accuracy undervoltage and overvoltage detectors act as supply monitors and ensure the supply is stable and within tolerance before applying power to the load. An inrush current control loop then takes over, resulting in a controlled startup current profile. When the external pass transistor is fully enhanced, Power Good status outputs then allow time adjustable or load feedback enabled sequencing of up to four load modules. Short circuits or excessive supply current events trigger protective circuits which quickly isolate the fault to prevent glitching of the backplane supply. With all these features, these devices offer a comprehensive solution for -48V Hot Swap applications.

Typical Application

Figure 1 shows a typical -48V Hot Swap application using the LTC4253A. The LTC4253A floats on the negative rail and uses an internal shunt regulator that together with R_{IN} and C_{IN} , regulates V_{IN} to about 13V above the negative rail. The MOSFET N-channel transistor Q1 is placed in the power path to control turn on and turn off with input from resistor R_S which senses the load current. R_C and C_C provides compensation for the current limit loop. R1 and R2 form a resistive divider that allows MOSFET turn on only when the -48V supply is between the user programmed undervoltage and overvoltage thresholds. The resistive divider R1/R2 connects to the -48V RTN rail via a short pin so that during plug in, the MOSFET is held off by the undervoltage condition until the longer power pins are properly seated. The five opto-couplers form an

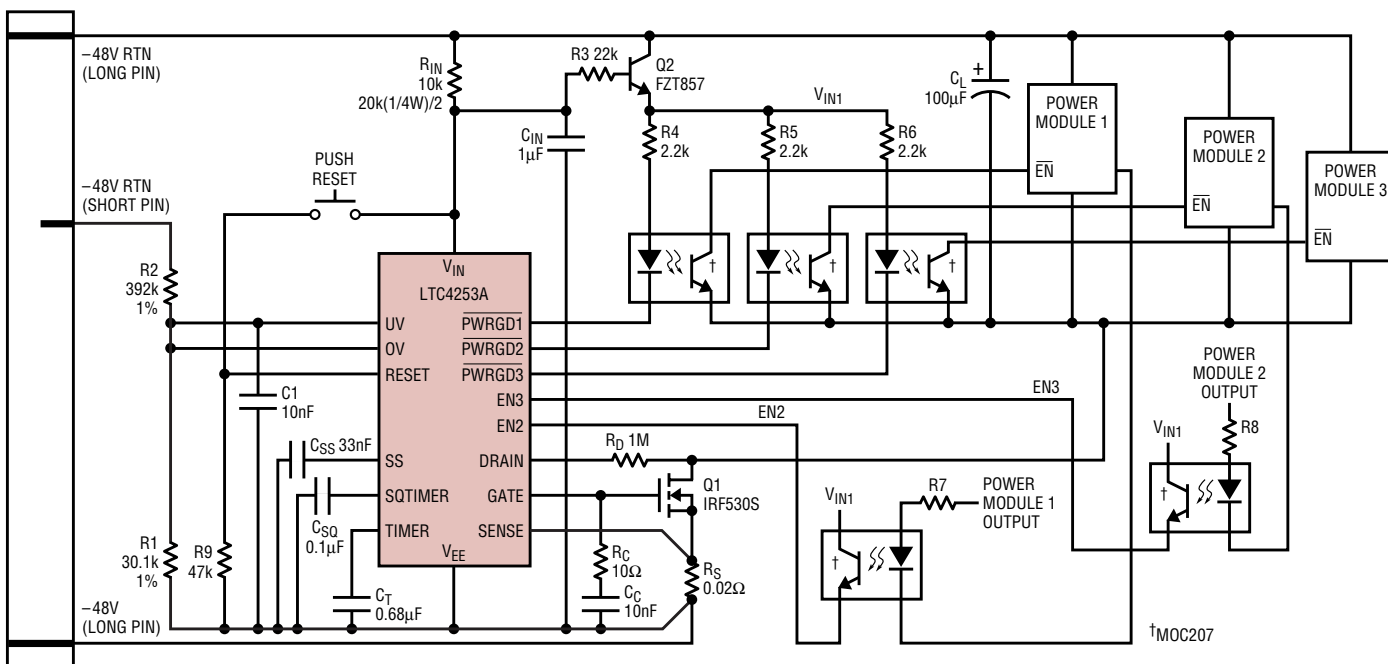


Figure 1. -48V/2.5A Hot Swap controller with opto-isolated Power Good sequencing

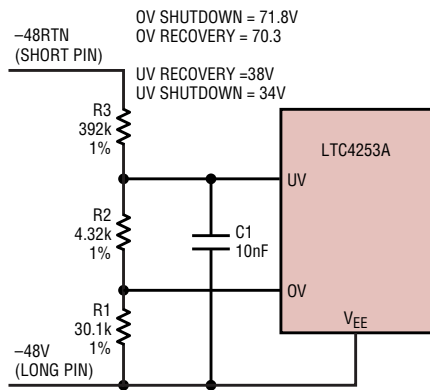


Figure 2. Undervoltage and overvoltage resistive divider connection to the LTC4253A

electrically isolated interface between LTC4253A and the load modules for power sequencing.

Undervoltage and Overvoltage Detection

The LTC4253A and LTC4253A-ADJ have 1% accurate undervoltage and overvoltage threshold detectors that can be set to any desired power supply range. This level of accuracy and flexibility allow these parts to be easily designed to conform to any operating

ranges specified by the various prevailing -48V standards.

In the LTC4253A, an UV hysteric comparator detects undervoltage conditions at the UV pin, with the following thresholds (with respect to V_{EE}):

- UV low-to-high (V_{UV}) = 3.08V
- UV low-to-high hysteresis (V_{UVHST}) = 0.324V

An OV hysteric comparator detects overvoltage conditions at the OV pin, with the following thresholds (with respect to V_{EE}):

- OV low-to-high (V_{OV}) = 5.09V
- OV low-to-high hysteresis (V_{OVHST}) = 0.102V

The undervoltage recovery and overvoltage shutdown thresholds are designed to match the standard telecom operating range of 43V to 71V with the UV and OV pins shorted as in Figure 1. The undervoltage shutdown and overvoltage recovery thresholds are then 38.5V and 69.6V respectively. The UV and OV pins can also be separated for implementing different operating ranges as shown in Figure 2.

The LTC4253A-ADJ offers additional flexibility in allowing the user to implement any required undervoltage recovery, undervoltage shutdown, overvoltage recovery and overvoltage shutdown thresholds. It achieves this by having two extra pins UVL and OVL connected to the internal comparators as shown in Figure 3. The undervoltage comparator has multiplexed inputs from UVL and UV, which is tapped off a resistive string across the power supply as in Figure 4. When comparator output UVD is high, UV is multiplexed to the comparator input UVIN. When UVD is low, UVL is multiplexed to UVIN. The overvoltage comparator similarly implements the overvoltage function. The various thresholds to note are (with respect to V_{EE}):

- UV low-to-high (V_{UVHI}) = 3.08V
- UVL high-to-low (V_{UVLO}) = 3.08V
- OV low-to-high (V_{OVHI}) = 5.09V
- OVL high-to-low (V_{OVLO}) = 5.08V

By tapping UVL, UV, OVL and OV off a resistive string across the power supply, undervoltage recov-

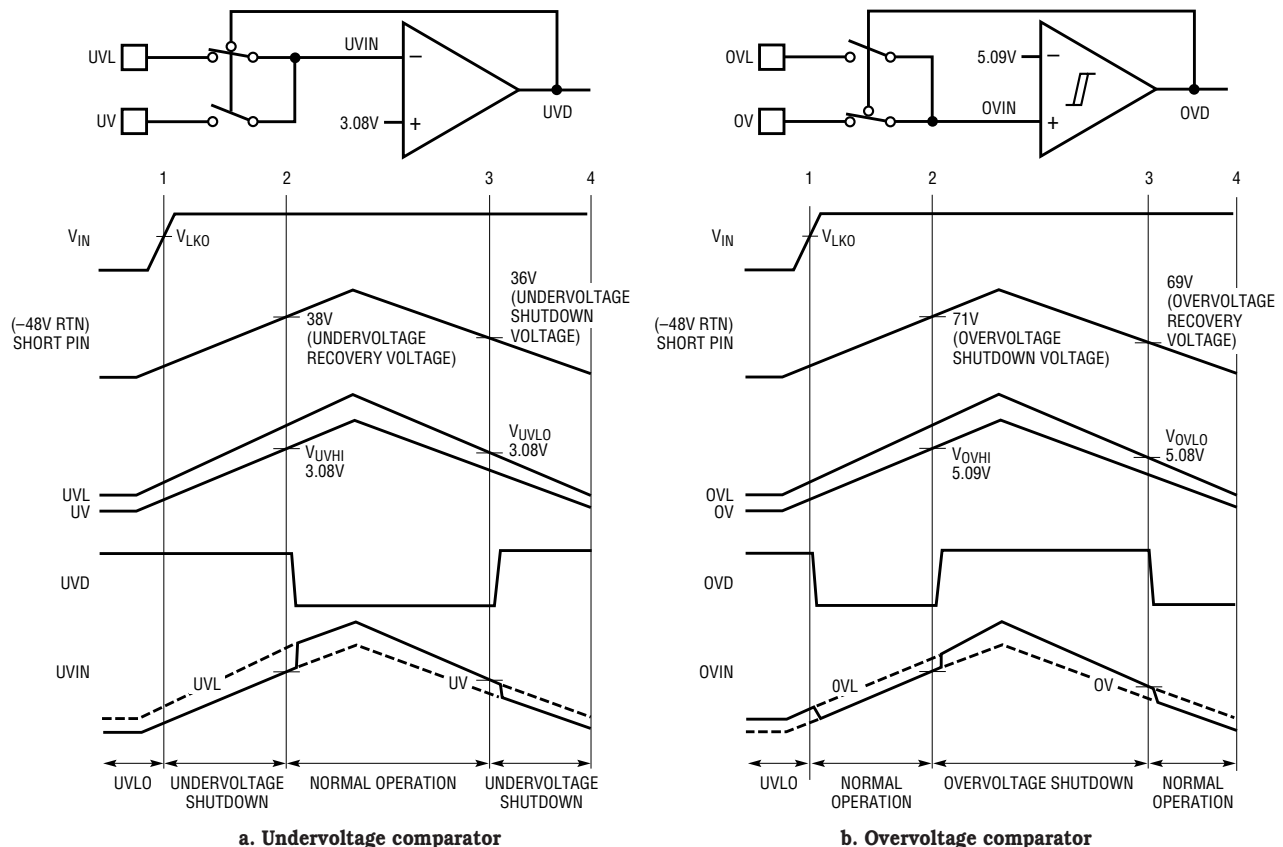


Figure 3. The LTC4253A-ADJ UV/OV detector block

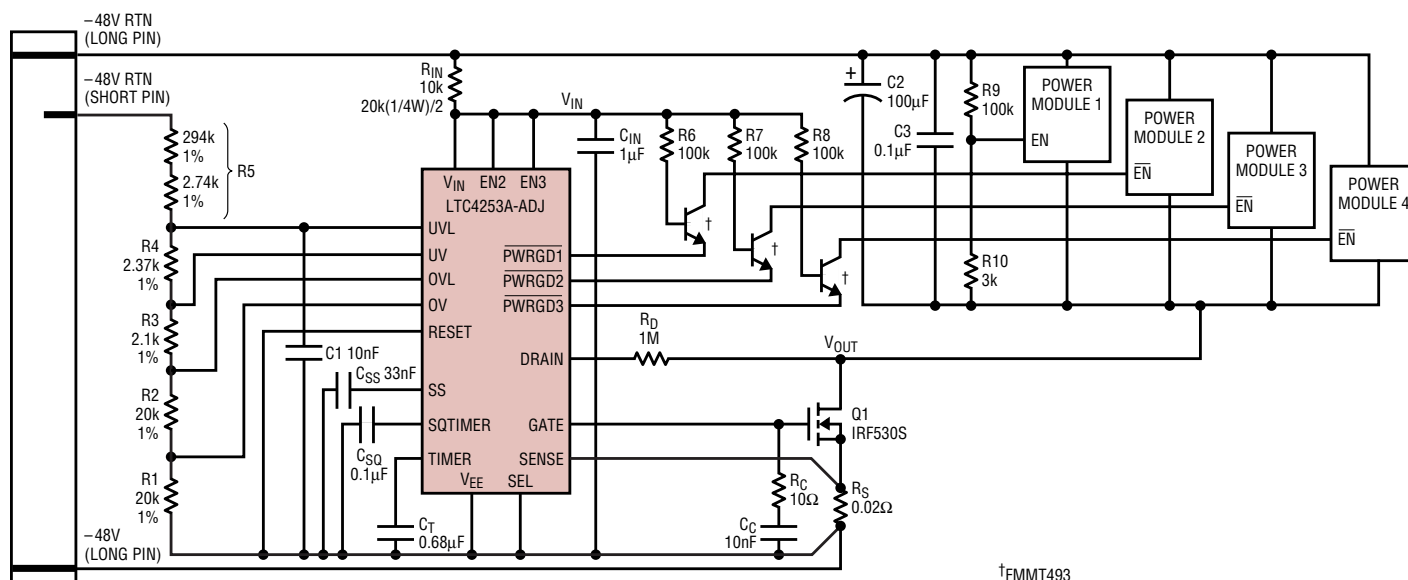


Figure 4. A -48V/2.5A Hot Swap controller with transistor enabled Power Good sequencing

ery = 43V, undervoltage shutdown = 39V, overvoltage recovery = 78V and overvoltage shutdown = 82V are implemented in Figure 4. Any required supply operating range can thus be implemented with great accuracy.

di/dt Soft Start

The LTC4253A offers a current soft start pin (SS) that acts as the reference for the analog current limit amplifier ($V_{ACL} = V_{SS}/20$). By attaching a capacitor at the SS pin, the analog current limit threshold ramps up in an exponential profile with an RC time constant equal to $50k\Omega \cdot C_{SS}$. The analog current limit amplifier forces the inrush current to follow this profile when the GATE pin rises above the

external MOSFET threshold and turns on the MOSFET. In this way, inrush current ramps up with a controlled slew rate (di/dt) that is approximately fixed and adjustable by C_{SS} (Figure 5a). Controlling the load current slew rate reduces system EMI and disturbances to the supply rail during startup.

The LTC4253A-ADJ offers an additional mode when the SEL pin is held low (it has an internal pullup to V_{IN} of $20\mu A$). In this mode, the SS pin is servoed from the time the GATE pin is released until it clears the external MOSFET threshold and turns the MOSFET on. The result is that the LTC4253A-ADJ enters analog current limit with V_{ACL} ramping up from close to zero. The resultant inrush current

profile presents a smooth ramp up from zero and the load current slew rate is able to maintain an approximately fixed di/dt gradient right from turn on (Figure 5b). This di/dt gradient is similarly adjustable by C_{SS} .

Power Good Sequencing

The LTC4253A has three sequenced \overline{PWRGD} outputs and two enable (EN) inputs. This allows three load modules to be enabled sequentially, minimizing any sudden load power demand on the backplane supply.

The three load modules can be timer sequenced as in Figure 4 where the EN pins are enabled by tying them to V_{IN} . The three \overline{PWRGD} signals assert sequentially with a fixed time delay adjustable by capacitor C_{SQ} (approximate $TD = 600ms \cdot (C_{SQ}/1\mu F)$). The load modules can also be load feedback sequenced as in Figure 1 where the load modules control the EN pin inputs. In this way when Load Module 1 is enabled by $\overline{PWRGD1}$ and fully started up, it can signal back via the EN2 input to enable Load Module 2, which is enabled after one $SQTIMER$ delay ramp. Load Module 2 can similarly enable Load Module 3 when it is ready. This mode of sequencing is shown in Figure 6.

The interface between the Hot Swap controller and the load modules is implemented with opto-couplers as in Figure 1 to take care of the differing

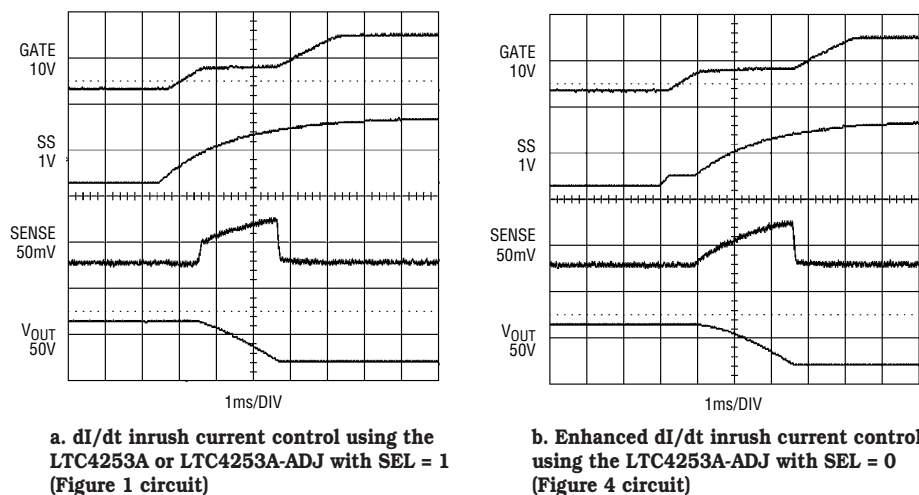


Figure 5. di/dt soft-start waveforms

signal common. If the load modules' $\overline{\text{EN}}$ inputs have sufficient protection against negative bias current, a simpler NPN interface can be implemented as in Figure 4.

Figure 7 highlights an additional feature of the LTC4253A-ADJ. The $\overline{\text{PWRGD1}}$ signal only activates after one SQTIMER ramp delay from the time GATE goes high and DRAIN goes low. This feature can be exploited to provide an additional EN1 signal so up to four load modules can be sequenced as in Figure 4.

Short Circuit Operation

Current faults are controlled in three stages using three thresholds: 50mV for a timed circuit breaker function, 60mV for an analog current limit loop and 200mV for a fast comparator that limits peak current in the event of a catastrophic short-circuit. This three-stage fault current minimizes backplane supply disturbances due to current faults.

A voltage across the SENSE resistor (R_S) of greater than 50mV triggers TIMER to source 200 μA into a timing capacitor C_T . C_T eventually charges to a 4V threshold and the part latches off. If the fault goes away before C_T reaches 4V, C_T slowly discharges (5 μA). A low impedance short can glitch the voltage across R_S above 200mV. This triggers a fast comparator that asserts a hard pulldown on the MOSFET gate to quickly bring the voltage across R_S

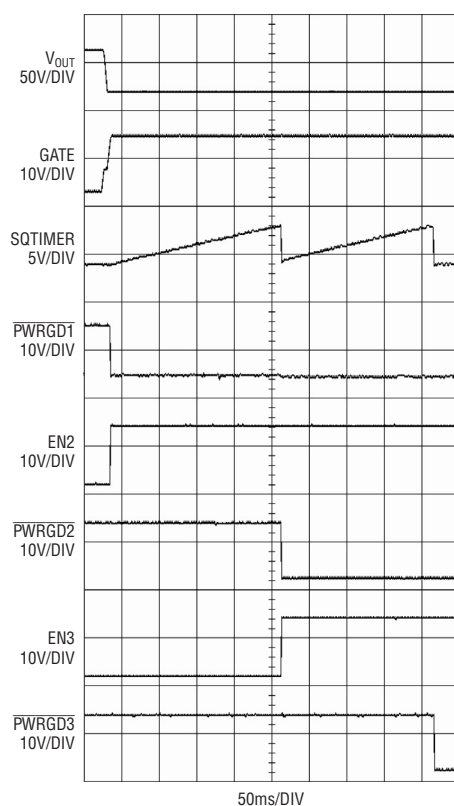


Figure 6. The LTC4253A controlling the turn on of three load modules using Load Feedback Sequencing

back below 200mV. This effectively limits the initial transient fault current. An analog current limit loop then controls the voltage across R_S to 60mV until TIMER reaches 4V (see Figure 8).

R_D in Figure 1 allows the MOSFET drain to pump current into the DRAIN pin internally clamped at around

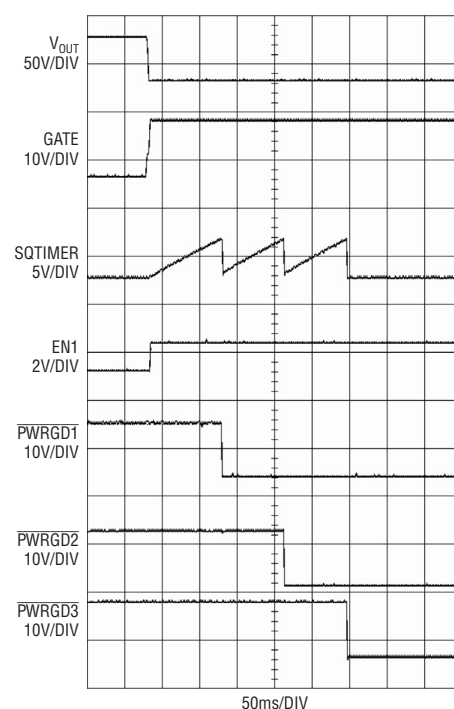



Figure 7. The LTC4253A-ADJ controlling the turn on of four load modules using Timing Sequencing

6V. This current is multiplied up by eight times and added to the 200 μA circuit breaker TIMER pullup current. This adds a component to the circuit breaker timeout period that is linearly proportional to the V_{DS} of the MOSFET, thus allowing the MOSFET to be designed to function closer to its SOA limits under different conditions.

Conclusion

The LTC4253A and LTC4253A-ADJ inherit the proven capabilities of Linear Technology's -48V Hot Swap family and add enhanced features. Chief among these is a highly flexible and 1% accurate undervoltage and overvoltage detection capability. Additional features include enhanced slew rate controlled inrush current profile and the ability to sequence up to four load modules. The LTC4253A is available in a 16-pin SSOP package and is completely pin compatible to the LTC4253. The LTC4253A-ADJ is available in a 20-pin SSOP package as well as a 20-pin 4mm \times 4mm QFN package. 

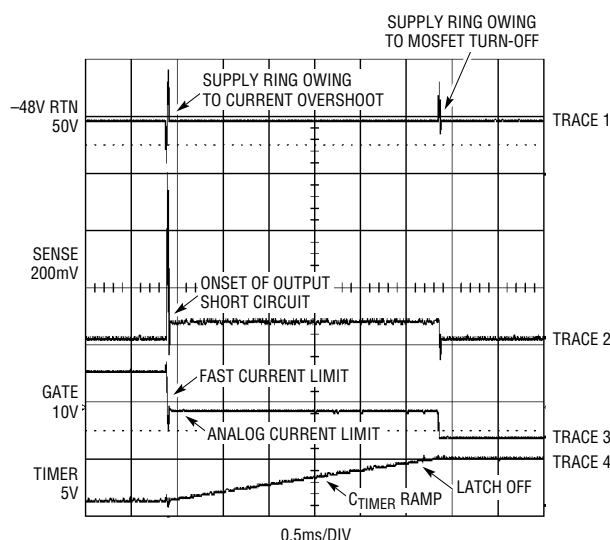


Figure 8. Output short-circuit waveforms

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