Prioritize Power Sources in Any Order, Regardless of Relative Voltage: No µP Required

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Does your application have multiple input power sources? Are one or more secondary source voltages equal to or higher than the main source? How do you ensure the main source powers the output when a higher voltage, secondary source is present? How do you prevent sources from cross conducting, or backfeeding during input source switchover? Do you need to prevent current sharing between similar voltage sources? Are you worried about users plugging in sources backwards or plugging in overvoltage sources to the system? The LTC4417 prioritized PowerPath™ controller, with its wide 2.5V to 36V operating voltage range, solves all these issues by controlling the connection of the input sources based on user-defined priority and validity while protecting the system from overvoltage and reverse voltage insertions up to ±42V.

PRIORITIZING THREE INPUT SOURCES

Figure 1 shows a triple-input prioritizer. Here, the 12V wall adapter is given top priority, the 14.8V Li-ion battery stack is prioritized second, and 12V sealed lead acid (SLA) battery has the lowest priority. Priority is simply set by connecting the sources to the LTC4417 in pin order: V1 is the highest priority; V3 the lowest priority.

The LTC4417 connects a higher priority input source to the output as long as the input source voltage remains valid—i.e., within its resistive-divider-defined overvoltage (OV) and undervoltage (UV) window. As long as the higher priority source remains valid, lower priority inputs remain disconnected, regardless of their relative voltages.

Accurate (±1.5%) comparators continuously monitor each input's OV and UV pins to ensure an input source is stable for at least 256ms before validating and allowing a connection to the output. Input sources are quickly disconnected if an OV or

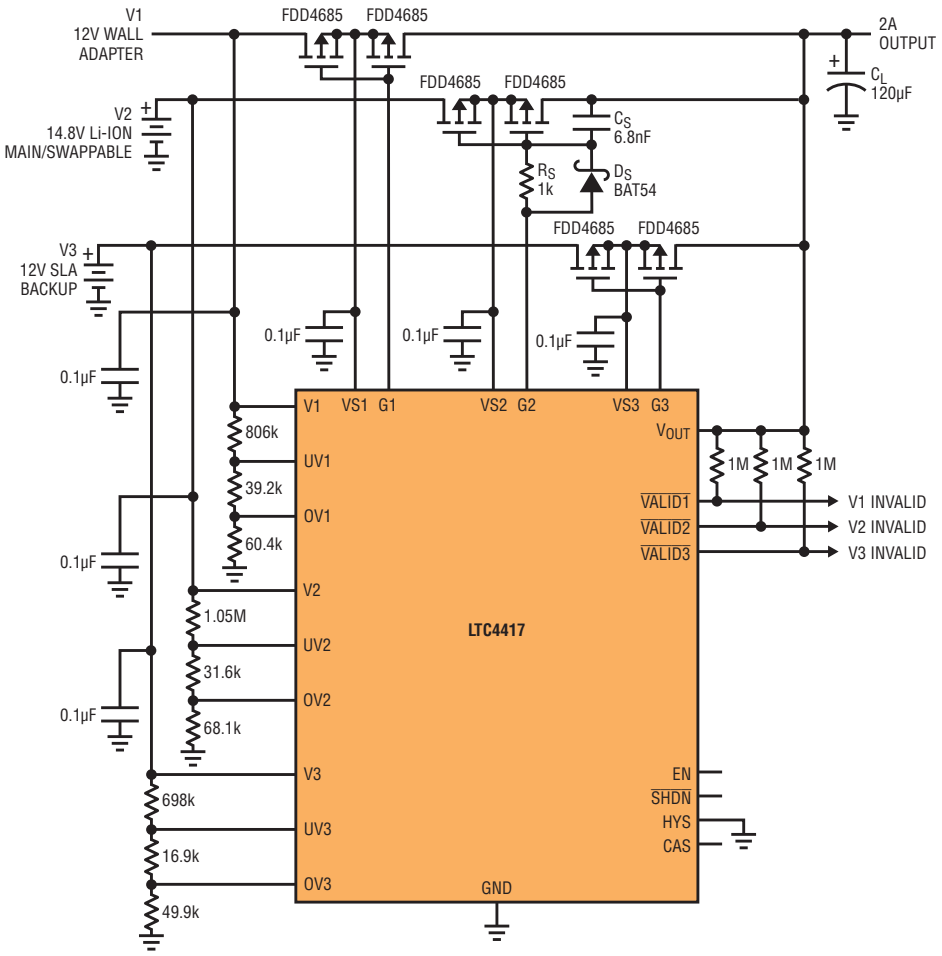

Figure 1. Triple input LTC4417 prioritized input source selection application

The high voltage (2.5V to 36V), triple input LTC4417 prioritized PowerPath controller is easy to use, robust and complete. Automatically prioritized supply current sourcing extends the life of lower priority input sources while controlled switching protects input sources from cross and reverse conduction during switchover.

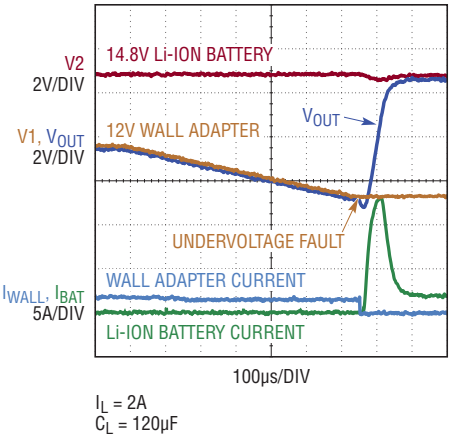

Figure 2. Switchover from a lower voltage input to a higher voltage input

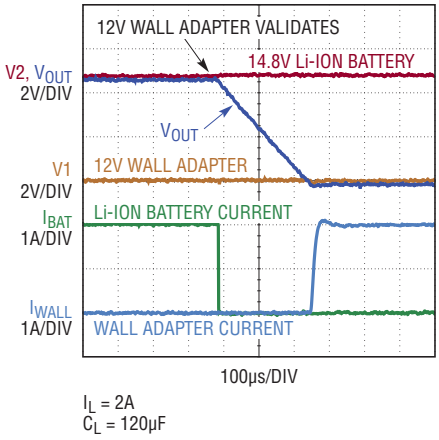

Figure 3. Switchover from a higher voltage to a lower voltage input

UV condition is sensed. An internal 8µs OV, UV filter time helps prevent false tripping.

Switching over to another valid input source can only occur when an OV or UV fault is detected or a higher priority source becomes valid. Referring again to Figure 1, this allows the lower voltage, higher priority 12V wall adapter to remain connected to the output provided it is valid. If another source is powering the output, the 12V wall adapter is reconnected to the output as soon as the wall adapter becomes valid.

The LTC4417 drives external back-to-back P-channel MOSFETs as switches to connect and disconnect input supplies to and from the output. Strong gate drivers ensure the back-to-back P-channel MOSFETs are firmly held off during input source insertion and provide enough strength to drive large, low $R_{DS(ON)}$, P-channel MOSFETs for reduced steady state power dissipation and increased output operating voltage range. An integrated 6.2V gate to source clamp prevents gate-to-source oxide overvoltage stress while allowing sufficient overdrive to enhance common logic level rated P-channel MOSFETs.

An important feature of the LTC4417 is the break-before-make circuit that protects input sources from cross-conduction during switchover. Gate-to-source (V_{GS}) comparators sense that the external MOSFETs of the disconnecting input source are off before another input source is allowed to connect to the common output. To prevent reverse conduction from the output to an input source during connection, reverse voltage (REV) comparators delay the connection if a higher output voltage is detected. Connection is delayed until the output voltage drops below the connecting input source voltage.

Figure 2 captures the event when the LTC4417 disconnects the 12V wall adapter from the output due to a UV fault. Once the V_{GS} comparator confirms that the disconnecting 12V wall adapter's back-to-back P-channel MOSFETs are off, the next highest priority valid input source, the 14.8V Li-ion battery, is immediately connected to the output. The two input source current waveforms show that no cross or reverse conduction occurs between the input sources during switchover, thanks to the V_{GS} comparator.

A resistor and capacitor, R_S and C_S in Figure 1, serve to limit the 14.8V Li-ion battery inrush current to a peak of 14A when it connects to the output. High inrush currents can cause input source UV faults, exceed the external MOSFET's maximum pulsed drain current (I_{DM}), or potentially damage connectors. The addition of R_S and C_S increases the switchover time, resulting in an output voltage droop of 400mV. Note that larger R_S and C_S values result in lower inrush currents at the expense of additional output voltage droop. Keep this trade-off in mind when selecting R_S and C_S. The Schottky diode, D_S, preserves the strong turn-off.

Figure 3 shows the LTC4417 disconnecting the lower priority valid 14.8V Li-ion battery stack to allow the newly validated higher priority 12V wall adapter to connect to the output. The REV comparator senses the initial 14.8V output voltage and prevents the 12V wall adapter from immediately connecting to the output. The REV comparator delays the connection until the output discharges below the 12V wall adapter voltage to ensure no reverse current occurs, as shown by the two input source current waveforms.

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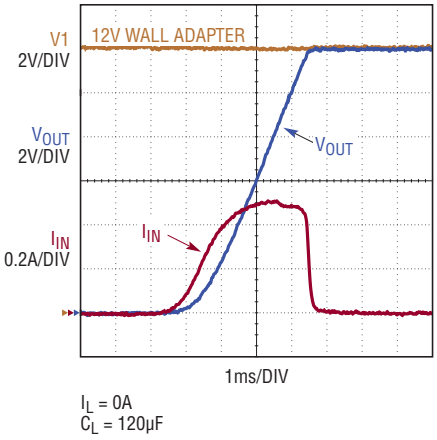


Figure 4. Output soft-start

Inrush current is also limited from the 12V wall adapter because it is quickly switched in when the output voltage is 11.88V. As its current waveform shows, the wall adapter provides the 2A load current plus the small additional current necessary to charge V_{OUT}.

PRIORITIZED, LOW I_{CC} MINIMIZES POWER DRAW

The LTC4417 draws only 28µA of total operating current, and it draws as much of this as possible from the highest priority valid supply. During normal operation, more than half the supply current is drawn from the output when V_{OUT} is above 2.5V. When V_{OUT} is less than 2.5V, operating current is drawn from the highest priority valid input supply, with any remaining supply current sourced from the highest voltage input source. The LTC4417 consumes almost no current from lower priority input sources when their voltages are lower than the output voltage.

When $\overline{SHDN}$ is forced low, the part is placed into a suspended mode where the OV and UV comparators are powered down to conserve power and all input sources are invalidated. In this state, the supply current is drawn from the highest voltage source.

OUTPUT SOFT-START

High inrush currents can occur when a higher voltage input source quickly connects to a lower voltage output bulk capacitor. When the output voltage is less than 0.7V, the LTC4417 soft starts V_{OUT} to minimize inrush current.

Figure 4 shows the input current and output voltage waveforms when the LTC4417 soft-starts from the 12V wall adapter to an initially discharged 120µF output bulk capacitor. As the figure shows, the peak input current is limited to 500mA.

After the output has been connected to its first supply, systems with similar voltages have minimal inrush current when changing channels due to the similar input and output voltages during input source switchover. This allows systems with similar input source voltages to omit the R_S, C_S, and D_S inrush current limiting circuitry shown in Figure 1.

Figure 5. 24V Application with reverse voltage protection

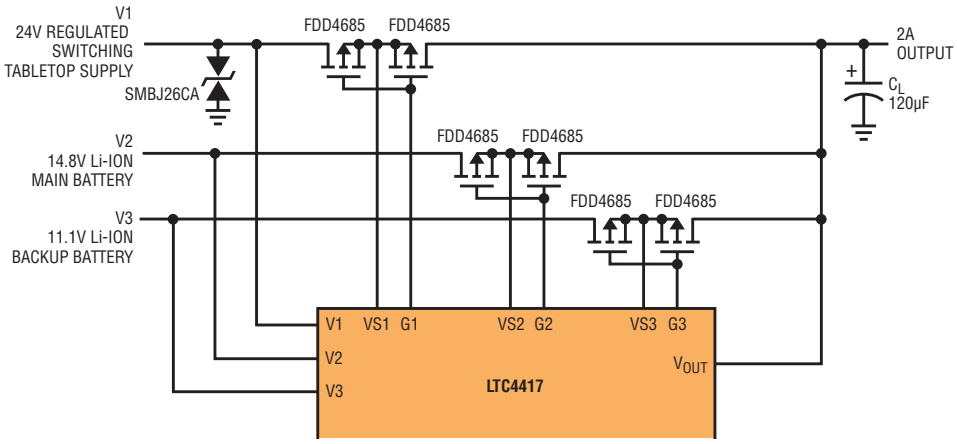
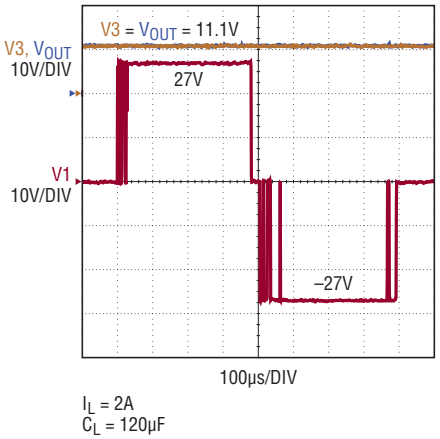


Figure 6. Over and reverse voltage blocking



With input source pins, V1 to V3, designed to handle ±42V, the LTC4417 only requires that the external P-channel MOSFETs be chosen with a BV_{DSS} rating greater than any anticipated voltage excursions from input to output for seamless over, under and reverse voltage input source insertion protection.

OVERVOLTAGE, UNDERVOLTAGE AND REVERSE VOLTAGE INSERTION PROTECTION

Applications where sources are physically plugged in and unplugged face the possibility of improper or faulty source insertions. Faulty wall adapter insertions can expose the system to potentially damaging overvoltage events while reverse voltage insertion can occur from improperly inserted batteries. These miscues can be compounded by the prevalence of standardized connectors with differing voltage specifications. With input source pins, V1 to V3, designed to handle ±42V, the LTC4417 only requires that the external P-channel MOSFETs be chosen with a BV_{DSS} rating greater than any anticipated voltage excursions from input to output for seamless over, under and reverse voltage input source insertion protection.

Figure 5 shows a complete input fault insertion protected system. The LTC4417 protects itself against input voltage ranging from –42V to 42V. The –40V BV_{DSS} FDD4685 P-channel MOSFETs are chosen to withstand the worst-case voltage excursion. During insertion, a 256ms deglitch timer ensures the strong gate drivers initially hold the external MOSFETs off. Transient voltage suppressor (TVS) diodes, highly recommended with input voltages above 20V, ensure transient voltage excursions do not exceed the LTC4417's absolute maximum voltage of ±42V. Figure 6 shows the LTC4417 blocking a forced V1 overvoltage step of 27V and subsequent –27V reverse voltage step from the 11.1V Li-ion battery stack and output. Inrush current limiting circuitry is not shown in Figure 5 for simplicity.

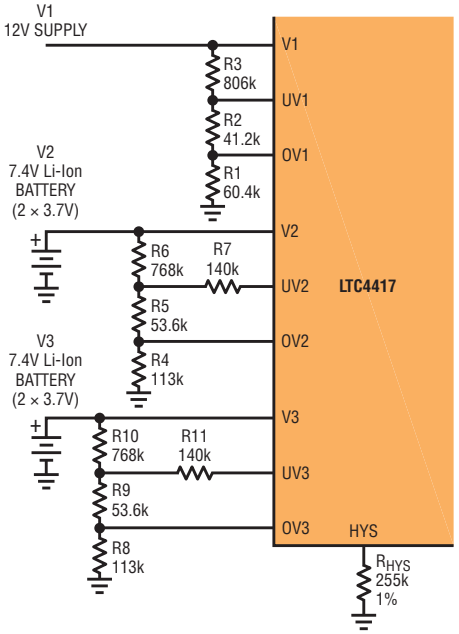


Figure 7. Configuring hysteresis voltages

HIGH IMPEDANCE INPUT SOURCE APPLICATIONS

Internal series resistance, present in all batteries and capacitors, produces a voltage drop that lowers the operating voltage when load currents are present. Removal of the load current allows the voltage source to recover this voltage drop. Some batteries and capacitors can recover hundreds of millivolts when load currents are disconnected due to a UV fault. If insufficient hysteresis is provided, the input source can reenter its valid window and reconnect.

For these situations, the LTC4417 allows the user to enable and set a hysteresis current through an external resistor, R_{HYS}. When hysteresis is switched in, one-eighth of the current flowing through R_{HYS} flows through the OV, UV resistive dividers to generate the hysteresis voltage. By adjusting the value of the resistive dividers and/or adding a resistor in series with the OV and UV pins, individual hysteresis voltages can be tailored to each input source's internal resistance characteristic, preventing false reconnection after recovery.

Figure 7 shows a 255kΩ resistor, R_{HYS}, setting 245nA of hysteresis current through the resistive dividers, R1 through R3, to generate approximately 200mV of OV and UV hysteresis at the 12V wall adapter. Resistive T-structures, R4 through R7 and R8 through R11, are used to set independent OV and

The LTC4417 can easily be cascaded to prioritize any number of input sources. Simply connect all of the cascaded LTC4417s' V_{OUT} pins to the system output and connect any higher priority LTC4417 CAS pin to the next lower priority LTC4417 EN pin.

UV hysteresis voltages of 201mV and 390mV, respectively, at the Li-ion batteries.

PRIORITIZE ANY NUMBER OF SOURCES

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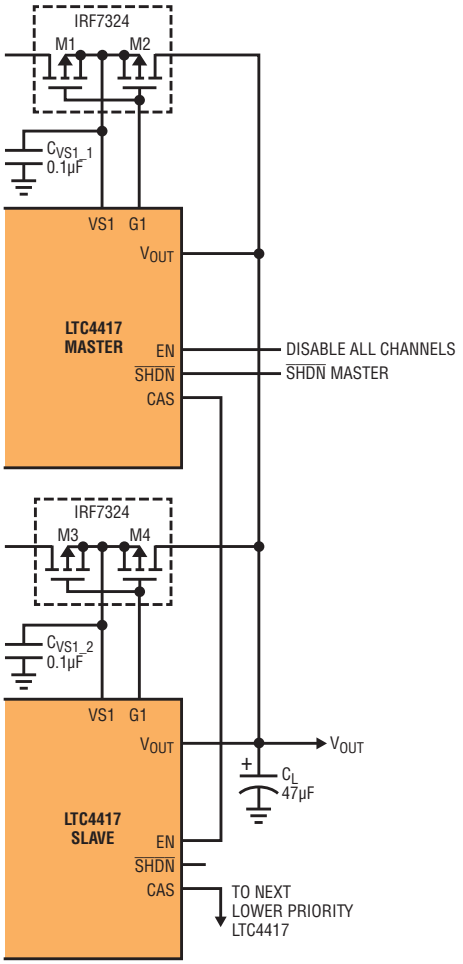
Figure 8. Cascading application



CONCLUSION

The high voltage (2.5V to 36V), triple input LTC4417 prioritized PowerPath controller is easy to use, robust, and automously allows applications to be powered from a variety of input sources, independent of voltage. Automatically prioritized supply current sourcing extends the life of lower priority input sources while controlled switching protects input sources from cross and reverse conduction during switchover.

Key features such as continuous input source monitoring through ±1.5% accurate overvoltage and undervoltage comparators, 256ms input deglitch time, and strong gate drivers with an integrated 6.2V clamp, enable overvoltage, undervoltage, and reverse voltage protection from faulty input source connections.

Resistive divider defined overvoltage and undervoltage trip points, adjustable current mode hysteresis, external inrush current limiting, and external back-to-back P-channel MOSFETs make the LTC4417 customizable to numerous applications. The LTC4417 is available in 24-lead GN and leadless 4mm × 4mm QFN packages. Both packages are available in C, I and –40°C to 125°C H grades.

Visit www.linear.com/LTC4417 for data sheets, demo boards and other applications information. ■