Compact Quad Step-Down Regulator with 100% Duty Cycle Operation Withstands 180V Surges

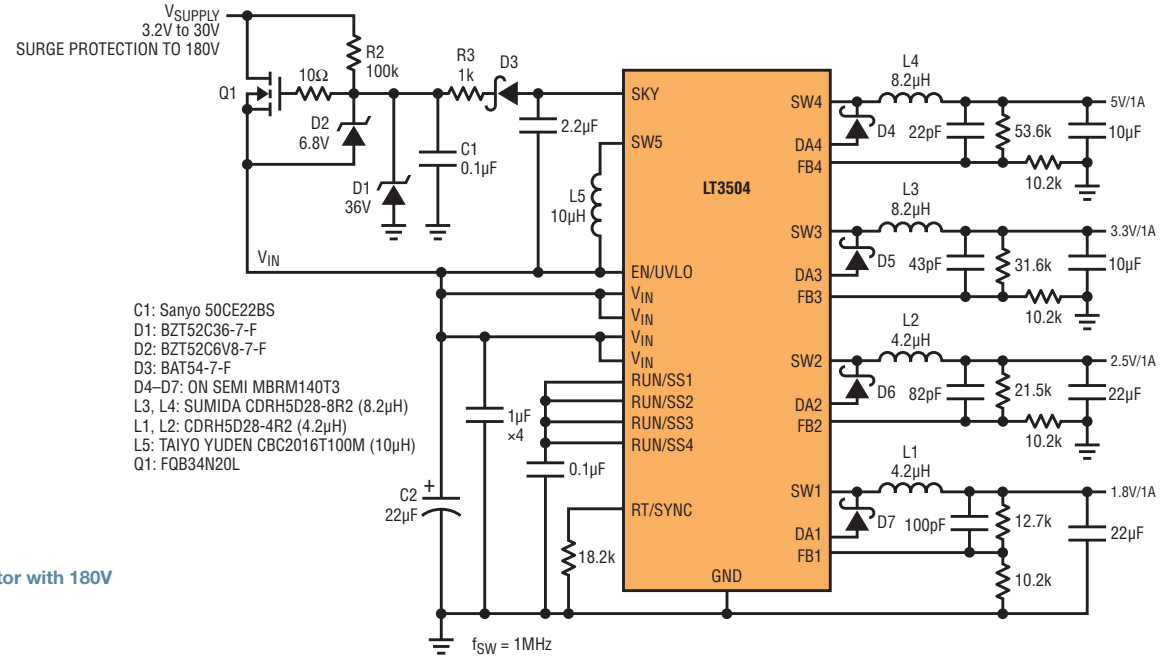
Jonathan Paolucci

Automotive, industrial and distributed applications routinely subject step-down DC/DC converters to a vast assortment of supply voltage transients. High voltage power spikes and input voltage dips can destroy sensitive circuits and jeopardize system reliability. To avoid damage, most applications rely on Tranzorbs or protection circuits that use MOSFETs as pass elements to suppress input voltage transients. If an N-channel MOSFET is used for this purpose, some means of providing gate drive above the input rail is necessary to bias the MOSFET on. Generating this bias is an undesirable complication that most engineers would prefer to avoid.

The LT3504 is a 4-channel monolithic step-down regulator designed for 100% duty cycle operation. Its unique architecture makes available a bias voltage, which is easily adapted to an N-channel protection scheme, allowing the LT3504 to operate continuously through overvoltage transients and dropouts down to 3.2V. Among its many features, the LT3504 includes output voltage tracking and sequencing, programmable frequency, programmable undervoltage lockout, and a power good pin to indicate when all outputs are in regulation.

QUAD 1A STEP-DOWN REGULATOR

Figure 1 shows the complete application circuit for a 4-output, 1A step-down regulator operating over a 3.2V to 30V range. Q1 provides surge protection to 180V. An on-chip boost regulator generates a voltage rail (V_{SKY}) that is 5V greater than the input voltage V_{IN}. Under normal operating conditions (V_{IN} < 33V), the V_{SKY} rail supplies gate drive to MOSFET Q1, providing the LT3504 with a low resistance path to V_{SUPPLY}. Additionally, the V_{SKY} pin supplies base drive for the switches in each buck converter channel, which allows for 100% duty cycle and



LTspice IV
circuits.linear.com/628

Figure 1. Complete quad buck regulator with 180V surge protection

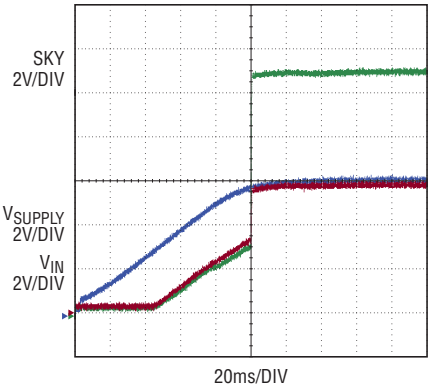


Figure 2. Figure 1's start-up behavior

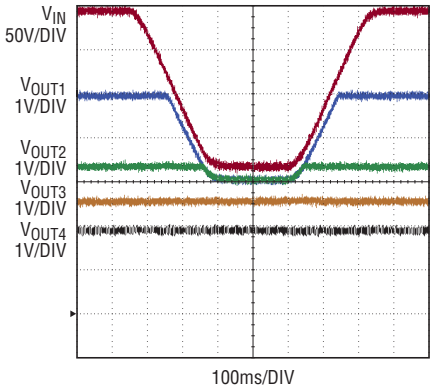


Figure 3. Figure 1's dropout performance

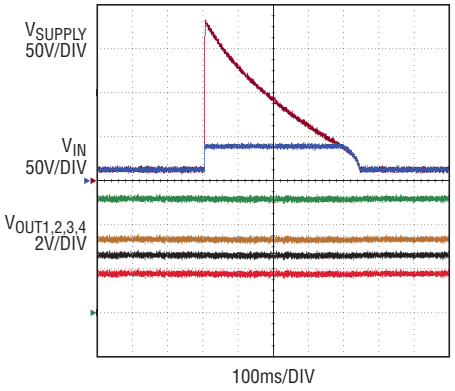


Figure 4. Overvoltage protection withstands 180V surge

eliminates the need for the boost capacitor typically found in buck converters.

Start-up behavior is shown in Figure 2. Resistor R2 pulls up on the gate of Q1, forcing source-connected V_{IN} to follow approximately 3V below V_{SUPPLY}. Once V_{IN} reaches the LT3504's 3.2V minimum start-up voltage, the on-chip boost converter immediately regulates the V_{SKY} rail 5V above V_{IN}. Diode D3 and resistor R3 bootstrap Q1's gate to the V_{SKY}, fully enhancing Q1. This connects V_{IN} directly to V_{SUPPLY} through Q1's low resistance drain-source path. It should be noted that, prior to the presence of V_{SKY}, the minimum input voltage is about 6.2V. However, with V_{SKY} in regulation and Q1 enhanced, the minimum run voltage drops to 3.2V, permitting the LT3504 to maintain regulation through deep input voltage dips. Figure 3 shows all channels operating down to the LT3504's 3.2V minimum input voltage.

OVERVOLTAGE INPUT TRANSIENT PROTECTION FOR MULTIPLE OUTPUTS

Figure 4 shows the LT3504 regulating all four channels at 1A load through a 180V surge event without interruption. As the supply voltage rises, Zener diode D1 clamps Q1's gate voltage to 36V. The source-follower configuration prevents V_{IN} from rising further than about 33V, well below the LT3504's 40V maximum input voltage rating. The LT3504 uses cycle-by-cycle peak current limiting, as well as catch diode current limit sensing, to protect the part and the external pass device from carrying excessive current during overload conditions.

Bear in mind that significant power dissipation occurs in Q1 during an overvoltage event. The MOSFET junction temperature must be kept below its absolute maximum rating. For the overvoltage transient shown in Figure 4, MOSFET Q1 conducts 0.5A (1A load on all buck channels) while withstanding the voltage difference between V_{SUPPLY} (180V) and V_{IN} (33V). This results in a peak power of 74W. Since the overvoltage pulse in Figure 4 is roughly triangular, average power dissipation during the transient event is approximately half the peak power. As such, the average power is given by:

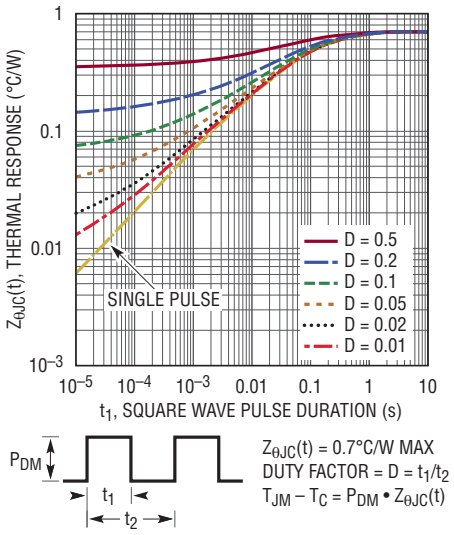
$$P_{AVG}(W) = \frac{1}{2} \bullet P_{PEAK}(W) = 37W$$

In order to approximate the MOSFET junction temperature rise from an overvoltage transient, one must determine the MOSFET transient thermal response as well as the MOSFET power dissipation. Fortunately, most MOSFET transient thermal response curves are provided by the manufacturer (as shown in Figure 5). For a 400ms pulse duration, the FQB34N20L MOSFET thermal response $Z_{\theta JC}(t)$ is 0.65°C/W. The MOSFET junction temperature rise is given by:

$$T_{RISE}(°C) = Z_{\theta JC}(t) \bullet P_{AVG}(W) = 24°C$$

Note that, by properly selecting MOSFET Q1, it is possible to withstand even higher input voltage surges. Consult manufacturer data sheets to ensure that the MOSFET operates within its Maximum Safe Operating Area.

Figure 5. FQB34N20L MOSFET transient thermal response



INDUCTIVE SPIKE PROTECTION

Input voltage transients, coupled with low ESR input capacitors, can produce large inductive spikes, which may damage buck converters. These high dV/dt events cause large inrush currents to flow in power connections and filter capacitors, particularly if parasitic inductance and resistance

(continued on page 29)

The inputs for three of the LDOs are hardwired to the output of the switching regulator, but the input to the remaining bank of two LDOs is undedicated, so it can be connected to the switching regulator or elsewhere. The outputs of the LDOs can be operated separately or paralleled for higher output currents.

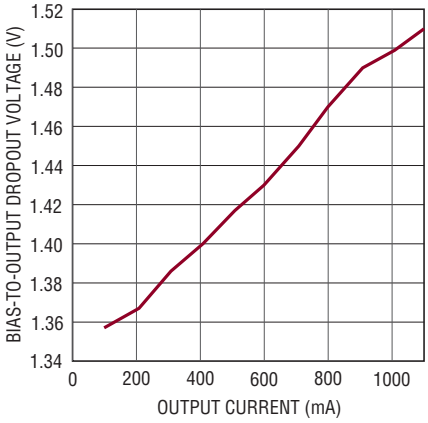


Figure 2. LDO V_{BIAS}-to-output dropout voltage vs output current

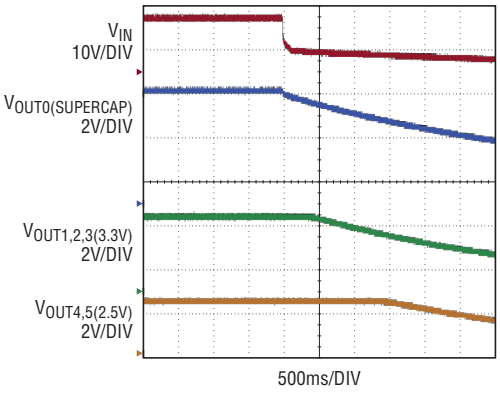


Figure 3. Supercapacitor power backup system holds up the 3.3V output for well over 100ms

output current of the LDOs is 1.5A, the holdup time for the 3.3V LDO output is:

$$3.3V\ HOLDUP\ TIME = \frac{C}{I}\Delta V$$
$$= \frac{1.5}{1.5}0.1$$
$$= 100ms$$

Both the LDO bias and LDO input power are connected to 5V from the supercapacitor. Although 5V is non-optimal with regard to power dissipation, it maximizes holdup time if the input supply fails. Power loss is minimized by operating the LDO with inputs that just meet, and do not exceed, the bias dropout requirements of the 3.3V LDO. But the supercapacitor voltage must exceed the input power dropout requirement to meet bias dropout and holdup requirements. To mitigate this increased power dissipation, the LTM8001 parallels LDOs to distribute heat and lower operating temperatures.

Holdup time is longer when the supercapacitor provides bias to the LDOs compared to using a conventional capacitor for that purpose. This avoids detrimental effects of charging a large capacitor directly with the input voltage. Figure 3 shows that the 3.3V output holdup time exceeds 100ms when the supercapacitor is charged to 5V and the LDO outputs are 3.3V at 1A and 2.5V at 0.5A.

CONCLUSION

The LTM8001 makes it easy to design a multiple output voltage regulator circuit featuring supercapacitor backup power. It is possible to achieve significant holdup time without adding large and undesirable capacitance directly to input power.

Visit www.linear.com/LTM8001 for data sheets, demo boards and other applications information. ■

(LT3504 continued from page 27)

is low. External gate network C1 and D2 limits these inrush currents by controlling Q1's gate voltage slew rate. Since V_{IN} follows Q1's gate voltage, the external gate network forces V_{IN} to ramp modestly compared to the abrupt input voltage transient present on V_{SUPPLY}, as shown in Figure 6.

CONCLUSION

The high voltage standoff capability of the series connected MOSFET blocks dangerous spikes from reaching the LT3504. During normal operation, the LT3504's built-in boost regulator permits 100% switch duty cycle operation and serves as an excellent MOSFET gate driver. The LT3504, along with a MOSFET and gate clamp, provides a transient-robust, compact multioutput solution.

Visit www.linear.com/LT3504 for data sheets, demo boards and other applications information. ■

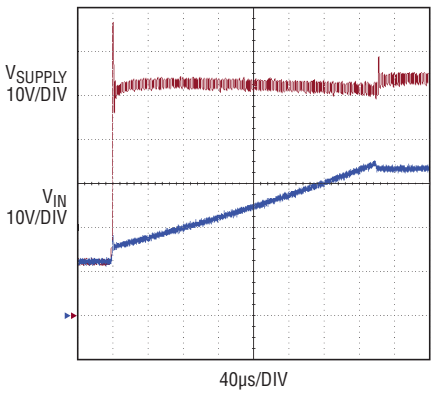


Figure 6. Fast V_{SUPPLY} dV/dt is blocked from V_{IN} by series MOSFET and gate network