

# Tiny Digital Predistortion Receiver Integrates RF, Filter and ADC

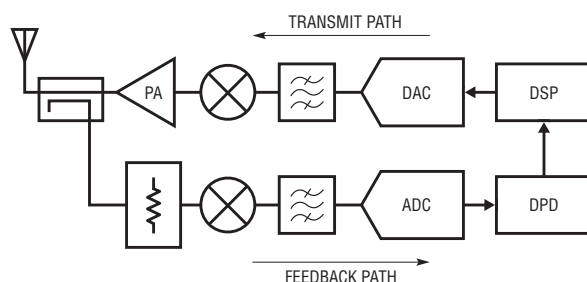
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The power amplifier (PA) consumes more electrical power than any other block in a cellular basestation and is therefore a significant factor in the operating expense for the service provider. Complex digital modulation requires extremely high linearity from the PA, so it must be driven well below saturation where it is most efficient. To improve PA efficiency, designers use digital techniques to reduce the crest factor and improve PA linearity, allowing it to run closer to saturation. Digital predistortion (DPD) has emerged as the preferred method of PA linearization. A great deal of focus is paid to the DPD algorithm but another critical element is the RF feedback receiver.

## DPD RECEIVER REQUIREMENTS

The DPD receiver converts the PA output from RF back to digital as part of a feedback loop (see Figure 1). Key design requirements are the input frequency range and power level, the intermediate frequency and the bandwidth to be digitized. Some of these are derived

Figure 1. Digital predistortion signal chain



directly from the PA specifications and some are optimized at design time.

The baseband transmit signal is upconverted to the carrier frequency and is defined in frequency by the air interface standard: WCDMA, TD-SCDMA, CDMA2000, LTE, etc. Since the purpose of the DPD loop is to measure the PA transfer function, it is not necessary to separate the carriers or demodulate the digital data. PA nonlinearity produces odd order intermodulation products which constitute spectral regrowth in the adjacent and alternate channels. Third-order products appear within a range of three times the bandwidth of the desired channel (see Figure 2). Likewise, fifth-order products appear within a range of five times the bandwidth and seventh-order products within seven times the bandwidth. Therefore, the DPD receiver must acquire a multiple of the transmit bandwidth equivalent to the order of the intermodulation products being linearized.

The trend in current development is to mix the desired channel to an intermediate frequency (IF) and capture the full bandwidth of all the intermodulation products. The exact IF is chosen to ease

filtering and avoid other frequencies that are already fixed based on specification requirements. The sample rate is similarly chosen as a multiple of the digital modulation chip rate, for example, 3.84MHz in WCDMA. Finally, the Nyquist theorem dictates that the sample rate must be at least twice the sampled bandwidth. Although many configurations are acceptable, one that meets these constraints is an IF of 184.32MHz, an ADC sample rate of 245.76MHz and a bandwidth of 122.88MHz.

In the case of a 20W PA, the average output power is 43dBm. The peak to average ratio (PAR) is about 15dBm. To set the average input power to the mixer of the receive chain at -15dBm, the combination of the coupler and attenuator insertion loss needs to be 58dB (refer to Figure 1). The in-band noise of the PA is specified by the WCDMA standard at a maximum of -13dBm/MHz (-73dBm/Hz). Therefore, the combination of the coupler and attenuation (-58dB) and the PA noise limit (-13dBm/MHz) yields a receiver sensitivity level that must be below -71dBm/MHz (-131dBm/Hz). For sufficient margin, a number at least 6dB to 10dB better than this is desirable. This sets the frequency

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plan, power level and sensitivity requirements for the DPD receiver.

### INTEGRATED DPD RECEIVER

Once the system requirements are defined, the task turns to the circuit implementation using a mixer, IF amplifier, ADC, passive filtering, matching networks and supply bypassing. While calculations and simulations are helpful, there is no substitute for evaluation of real hardware, which generally leads to multiple printed circuit board (PCB) iterations. However, a new class of integrated receivers based on Linear Technology's  $\mu$ Module<sup>®</sup> packaging technology greatly simplifies this task. The LTM<sup>®</sup>9003 digital predistortion  $\mu$ Module receiver is a fully integrated DPD receiver—essentially RF-to-bits in a single device.

The LTM9003 consists of a high linearity active mixer, an IF amplifier, an L-C bandpass filter and a high speed ADC (see Figure 3). The wire-bonded bare die assembly ensures that the overall form factor is highly compact, but also allows the reference and supply bypass capacitors to be placed closer to the die than possible with traditional packaging. This reduces the potential for noise to degrade the fidelity of the ADC. This idea extends to the high frequency layout techniques used throughout the receiver chain of the LTM9003.

The integration eliminates many challenges of driving high speed ADCs. Linear circuit analysis cannot account for the current pulses resulting from the sample-and-hold switching action of the ADC. Traditional circuit layout requires multiple iterations to define an input network that

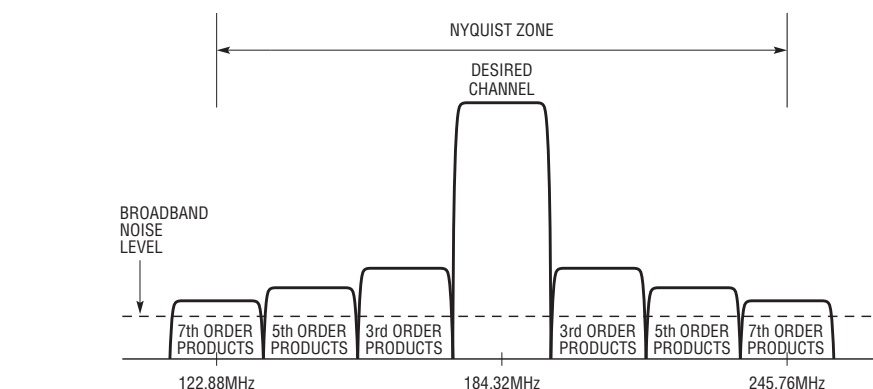


Figure 2. Intermodulation products

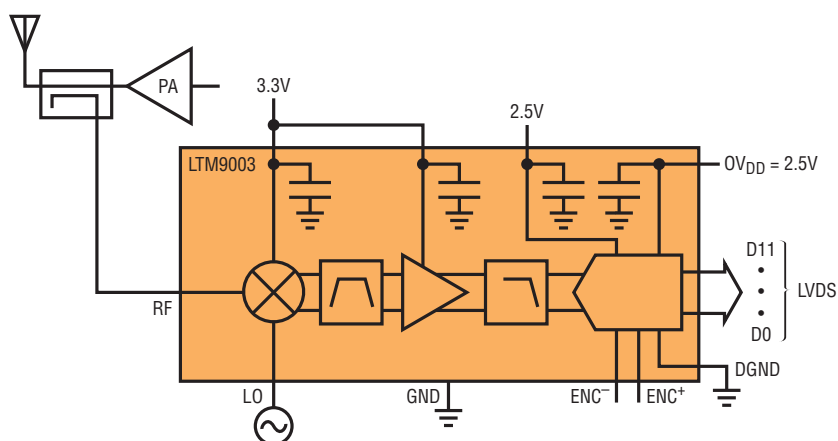
absorbs these pulses, is absorptive out of band, and yet works seamlessly with the preceding amplifier. The IF amplifier must also be capable of driving this network without adding distortion. Solving these challenges may be the greatest hidden attribute of the LTM9003  $\mu$ Module receiver.

The passive bandpass filter is a third order filter with an extremely flat pass-band. The center 25MHz of the band

exhibits less than 0.1dB ripple, and over the entire 125MHz the passband ripple is only 0.5dB. The third order configuration ensures that the shoulders of the frequency response are monotonic which is important for many DPD algorithms.

The overall performance of the LTM9003 greatly exceeds the system requirements described above. With a single tone at  $-2.5\text{dBm}$ , which is equivalent to  $-1\text{dBFS}$  at

Figure 3. LTM9003 integrated digital predistortion receiver



At the engineering level, the LTM9003 saves time. Filter design and component matching require PCB iteration to get it right. It is particularly challenging to design a filter that is undisturbed by the switching action of the ADC sample and hold circuitry. Even the placement of capacitors for supply decoupling affects overall performance and can cause board layout revisions.

the ADC, the signal to noise ratio (SNR) is typically  $-145\text{dBm/Hz}$ . This figure is well below the target value of  $-131\text{dBm/Hz}$  defined by the WCDMA standard. The worst-case harmonics are 60dBc. The  $\text{IP}_3$  figure of  $25.7\text{dBm}$  means that the LTM9003 could support an ACPR of 87dBC if the PA were linear enough. Relative to the system requirements and the capability of the best power amplifiers available, the LTM9003 greatly exceeds the requirements. The entire chain consumes about  $1.5\text{W}$  from a  $3.3\text{V}$  and a  $2.5\text{V}$  supply, yet requires a circuit board area of only  $11.25\text{mm} \times 15\text{mm}$ .

#### ALTERNATE CONFIGURATIONS

$\mu\text{Module}$  technology also offers an unexpected level of flexibility. By changing the values of the passive components or substituting ICs that are optimized as a group, the LTM9003 can be made available in application-specific versions, with no loss of performance or increased complexity.

For example, the LTM9003-AA utilizes a low power, silicon germanium active

mixer operating from a  $3.3\text{V}$  supply. The  $2 \times \text{RF} - 2 \times \text{LO}$  product gives a 60dBc second harmonic, which is the worst spur in the spectrum. This can be improved at the expense of power consumption by replacing the mixer with a similar  $5\text{V}$  part. The second harmonic is then improved by 4dB in the LTM9003-AB. Similarly, the sample rate can be reduced by substituting a  $210\text{Msps}$  ADC which consumes less power and the L-C filter values can be changed to realize a different filter bandwidth yet still achieve excellent passband flatness.

#### BIG BENEFITS IN SMALL PACKAGE

The benefits of using the LTM9003 for PA linearization occur at several levels. At a high level, DPD allows you to run the PA with less back-off. The result is that the PA is more efficient and therefore consumes less power for the same output power level.

At the board level, the  $\mu\text{Module}$  packaging integrates all of the key components into a small area including the passive filter and decoupling components. This

saves significant board space, simplifies layout and improves performance. The integration may enable a high performance remote radio head (RRH).

At the engineering level, the LTM9003 saves time. Filter design and component matching require PCB iteration to get it right. It is particularly challenging to design a filter that is undisturbed by the switching action of the ADC sample and hold circuitry. Even the placement of capacitors for supply decoupling affects overall performance and can cause board layout revisions. These tasks can consume months of engineering time to debug each revision and evaluate the changes. With the LTM9003, this work has already been done.

#### CONCLUSION

While the digital algorithms for DPD garner much attention, the analog receiver design is similarly demanding. The LTM9003  $\mu\text{Module}$  receiver simplifies this design by integrating the entire receiver in a single tiny package. ■

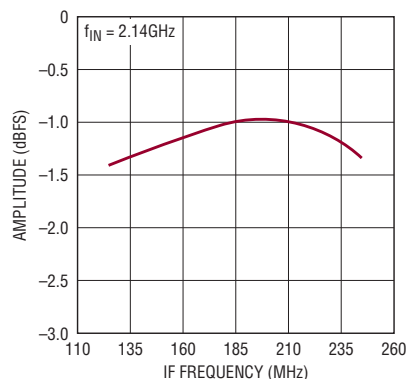


Figure 4. IF frequency response

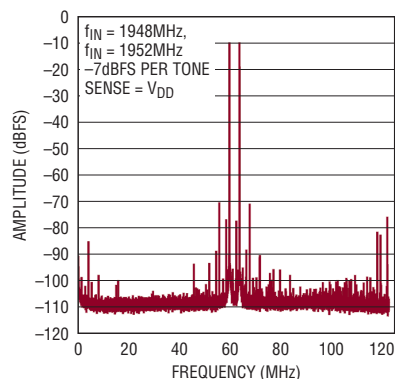


Figure 5. 64k point 2-tone FFT

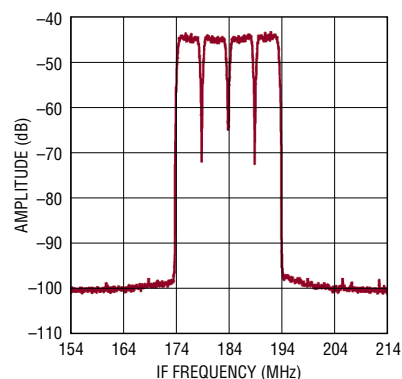


Figure 6. FFT of 4-channel WCDMA input at 2.14 GHz