

# Rail-to-Rail 14-Bit Dual DAC in a Space Saving 16-Pin SSOP Package

by Hassan Malik

Linear Technology introduces the LTC1654, a 14-bit rail-to-rail voltage output dual DAC in a space saving 16-pin SSOP package. This part offers a convenient solution for applications where density, resolution and power are critical parameters. The LTC1654 is guaranteed to be 14-bit monotonic over temperature with a typical differential nonlinearity of only 0.3LSB. The supply voltage range is 2.7V to 5.5V.

The LTC1654 is software programmable for two different speed/power modes of operation: a FAST mode with 3.5 $\mu$ s settling time and 750 $\mu$ A supply current and a SLOW mode with 8 $\mu$ s settling time and 450 $\mu$ A supply current. Either of the two DACs can be independently set to the FAST or the SLOW mode of operation. The

output amplifiers swing to within 450mV of either supply rail when sourcing or sinking 5mA and are capable of driving over 300pF of load capacitance. The output noise voltage density at 1kHz is 540nV/ $\sqrt{\text{Hz}}$  in SLOW mode and 320nV/ $\sqrt{\text{Hz}}$  in FAST mode.

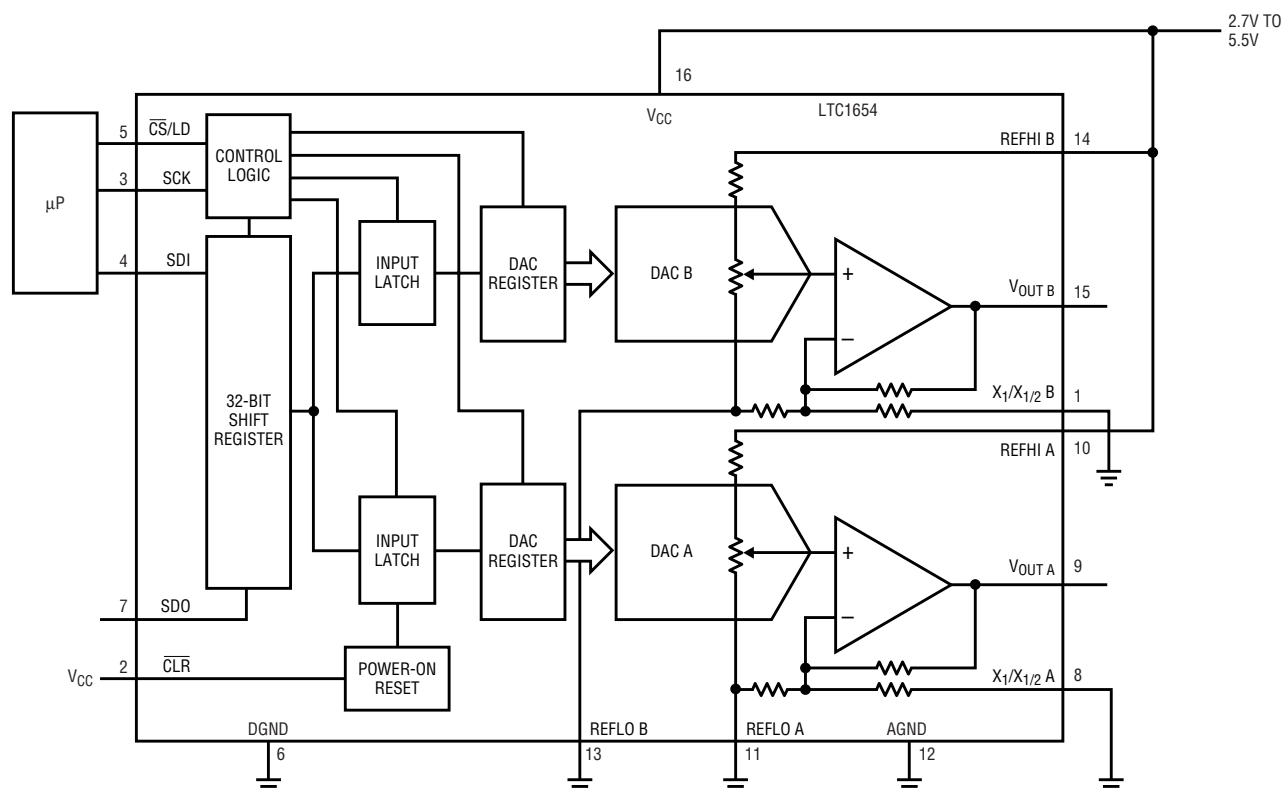
The LTC1654 has separate REFHI and REFLO pins for each DAC and two different gain modes. A gain of one is set by connecting the  $X_1/X_{1/2}$  pin to REFLO and a gain of one-half is set by connecting this pin to  $V_{\text{OUT}}$ . The two different gain modes allow the user to set different output spans. The REFHI inputs have an operating range from ground to  $V_{\text{CC}}$  and the REFLO inputs have an operating range from ground to  $V_{\text{CC}} - 1.5\text{V}$ . A block diagram of the part is shown in Figure 1.

The LTC1654 allows each of the DACs to be individually shut down, in which state they consume less than 4 $\mu$ A/DAC. The REFHI input goes into a high impedance state when the DAC is in shutdown. The respective speed states are retained in shutdown as long as the supply voltage is maintained above the minimum value of 2.7V. When the supply voltage is first applied, both DACs are active and in SLOW mode, with all zeros loaded in the input shift register and DAC latches.

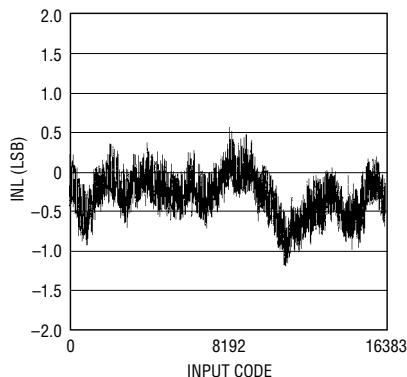
The LTC1654 has a double-buffered 3-wire serial interface consisting of clock, data and chip select pins. This interface is SPI/QSPI and

*continued on page 33*

MICROWIRE is a trademark of National Semiconductor Corp.



**Figure 1. LTC1654 block diagram**



**Figure 2. LTC1654 typical integral nonlinearity (INL)**

*LTC1654, continued from page 28*

MICROWIRE™ compatible. The maximum clock rate is 33MHz. Double buffering allows individual load and update capability for each DAC. There are three different methods for loading data into the serial interface: a 24-bit word without daisy chaining, a 32-bit word without daisy chaining and a 32-bit word with daisy chaining. The 24-bit word loading method requires eight bits for control and address followed by sixteen bits of data. The last two LSBs in the 16-bit

data segment are “don’t cares.” The 32-bit word loading method without daisy chaining requires eight “don’t cares” followed by eight bits for control and address and sixteen bits of data. The 32-bit word loading method with daisy chaining is the same as above except that the D<sub>OUT</sub> pin is used.

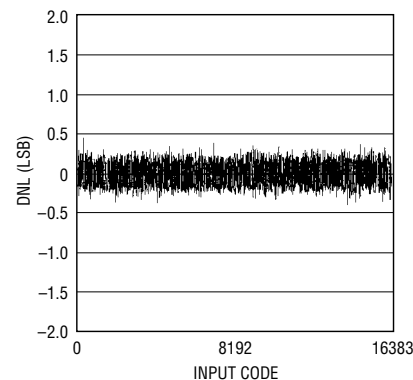
When the REFHI pins are connected to V<sub>CC</sub> and the LTC1654 is configured for a gain of one, the voltage outputs swing from ground to V<sub>CC</sub>. The typical differential and integral nonlinearities are shown in Figures 2 and 3, respectively. V<sub>OUT</sub> is as follows for the two different gain configurations:

Gain of one (X<sub>1</sub> / X<sub>1/2</sub> pin connected to REFLO):

$$V_{OUT} = (V_{REFHI} - V_{REFLO}) \cdot (SDI/16384) + V_{REFLO}$$

where SDI is the decimal representation of the digital data input.

Gain of one-half (X<sub>1</sub> / X<sub>1/2</sub> pin connected to V<sub>OUT</sub>):



**Figure 3. LTC1654 typical differential nonlinearity (DNL)**

$$V_{OUT} = (1/2)(V_{REFHI} - V_{REFLO}) \cdot (SDI/16384) + V_{REFLO}$$

In any rail-to-rail DAC, the output swing is limited to voltages within the supply range. If the DAC offset is negative, the output for the lowest codes limits at 0V. Similarly, limiting can occur near full-scale when the REFHI pin is tied to V<sub>CC</sub>. This can be avoided by ensuring that V<sub>REFHI</sub> is less than V<sub>CC</sub> by at least 15mV or by using the gain of one-half configuration. 