

CompactPCI Hot Swap Controllers with Bus Precharge, On-Chip Intercept of PCI Reset Signal and Much More

by Andrew Gardner

Introduction

When a circuit board is inserted into a "hot" (powered) backplane, its supply bypass capacitors can draw large currents from the backplane power bus as they charge. These currents can cause glitches on the backplane supply voltage, resetting other boards in the system, and can even damage edge connectors. The LTC1644 and LTC1646 Hot Swap™ controllers safely limit these charging currents during board insertion into a hot backplane. They also offer several features specifically tailored for CompactPCI™ (CPCI) Hot Swap applications:

- ❑ Precharge output for biasing I/O connector pins during board insertion and extraction to minimize bus glitches
- ❑ On-chip intercept of the global PCI reset signal
- ❑ Dual-level circuit breakers for the 5V and 3.3V supplies with slow and fast response times for overcurrent and short-circuit fault conditions, respectively
- ❑ The ability to power-up all supplies over a wide range of capacitive loads using foldback

current limit without causing spurious overcurrent faults

The LTC1644 provides a Hot Swap solution for CPCI applications requiring all four rails available from a CPCI connector: 5V, 3.3V, 12V and -12V. The LTC1644 is intended for use in CPCI applications where only the 5V and 3.3V rails are used. The LTC1644 is available in a 20-pin SSOP package, whereas the LTC1646 is available in a space-saving 16-pin SSOP package.

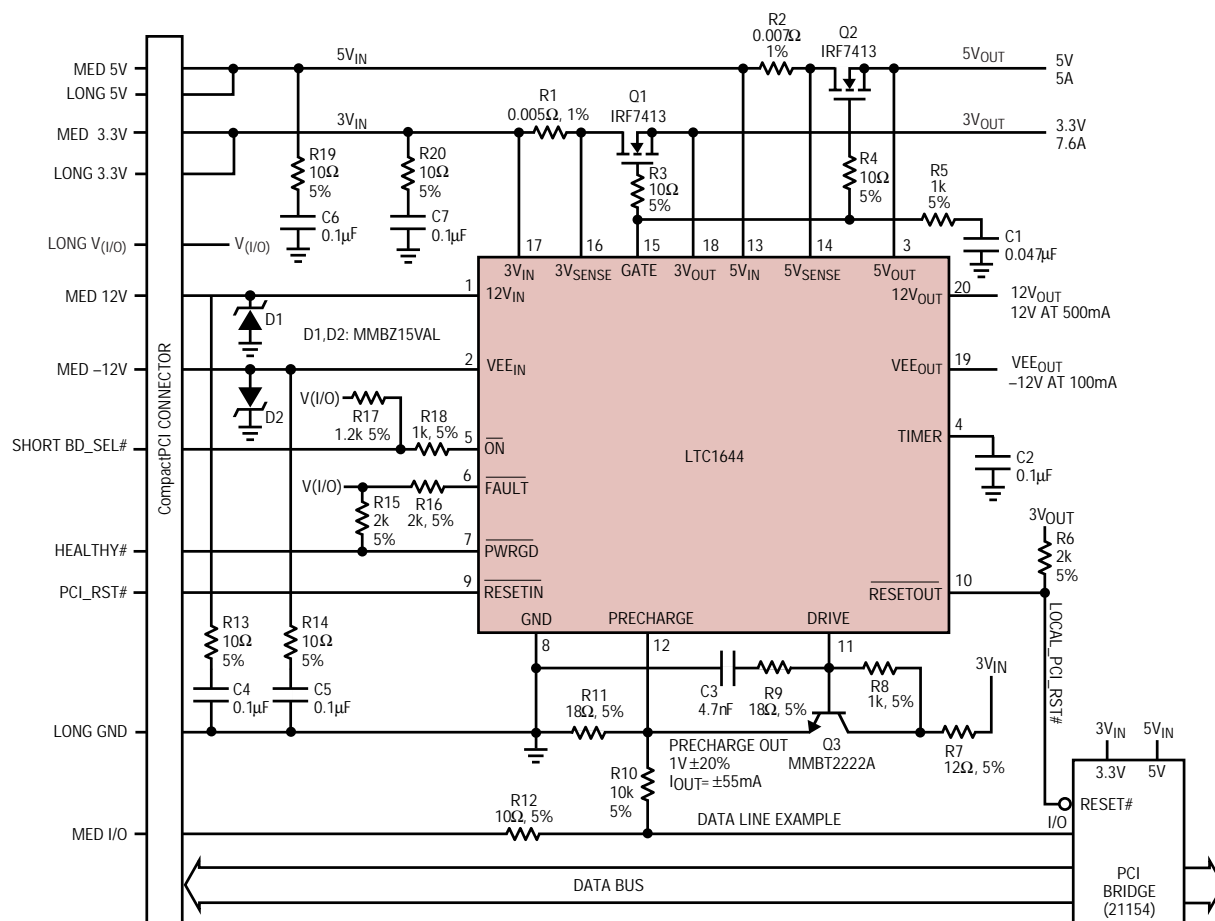


Figure 1. LTC1644 typical application

Typical CPCI Hot Swap Applications

Figures 1 and 2 show the LTC1644 and LTC1646, respectively, in typical CPCI Hot Swap applications. In both applications, transistors Q1 and Q2 limit the 3.3V and 5V supply currents when a board is inserted into a hot backplane. The currents through Q1 and Q2 are sensed across resistors R1 and R2. Resistors R3 and R4 prevent high frequency oscillations in Q1 and Q2. By ramping the gates of Q1 and Q2 up at a controlled rate, the transient surge current ($I = C \cdot dv/dt$) drawn from the main backplane supply is limited to a safe value when the board is inserted. In addition, the LTC1644 contains internal pass transistors for both the 12V and -12V supplies that have fixed current limits. A current foldback limit feature also protects all of the supplies. If an output voltage is shorted to ground, the current limit drops in order to keep power dissipation and supply glitches to a minimum.

Transistor Q3 and its associated components form the precharge circuit in both applications. The voltage at the DRIVE pin is varied in order to maintain a constant 1V at the PRECHARGE pin. Resistor R10 biases the example I/O line to 1V during hot insertion and extraction, thus minimizing glitches on the backplane I/O line as the connector pin makes/breaks its connection.

The LTC1644 and LTC1646 are designed to fully support the CPCI backplane-to-daughtercard signaling environment. The $\overline{\text{BD_SEL\#}}$ signal is connected to the $\overline{\text{ON}}$ pin while the $\overline{\text{HEALTHY\#}}$ signal is connected to the $\overline{\text{PWRGD}}$ pin. In the event that any of the output voltages fall below their power-good thresholds, the $\overline{\text{PWRGD}}$ pin is pulled up to $V_{(I/O)}$, causing the $\overline{\text{HEALTHY\#}}$ signal to deassert. The global PCI_RST\# signal is combined on-chip with the $\overline{\text{HEALTHY\#}}$ signal in order to generate the $\overline{\text{LOCAL_PCI_RST\#}}$ signal at the $\overline{\text{RESETOUT}}$ pin. The $\overline{\text{LOCAL_PCI_RST\#}}$ signal is

pulled low whenever the $\overline{\text{HEALTHY\#}}$ signal is high; it can also be pulled low when the PCI_RST\# input signal is low.

When a board is inserted into a CPCI connector, the long $V_{(I/O)}$, 5V, 3V and GND pins make contact first and power up the $V_{(I/O)}$ pull-up resistors, bus precharge circuitry inside the LTC1644 and LTC1646 and the PCI bridge chip. During the next stage of insertion, the medium length 5V, 3.3V, 12V, -12V and I/O pins make contact, pulling the $\overline{\text{ON}}$ pin voltage to GND, and a power-up sequence begins.

Power-Up Sequence

The timing for a typical power-up cycle for the LTC1644 is shown in Figure 3 (the LTC1646 waveforms are similar except for the absence of the 12V and -12V input and output voltages). The gates of the FETs (GATE pin) are pulled up by an internal

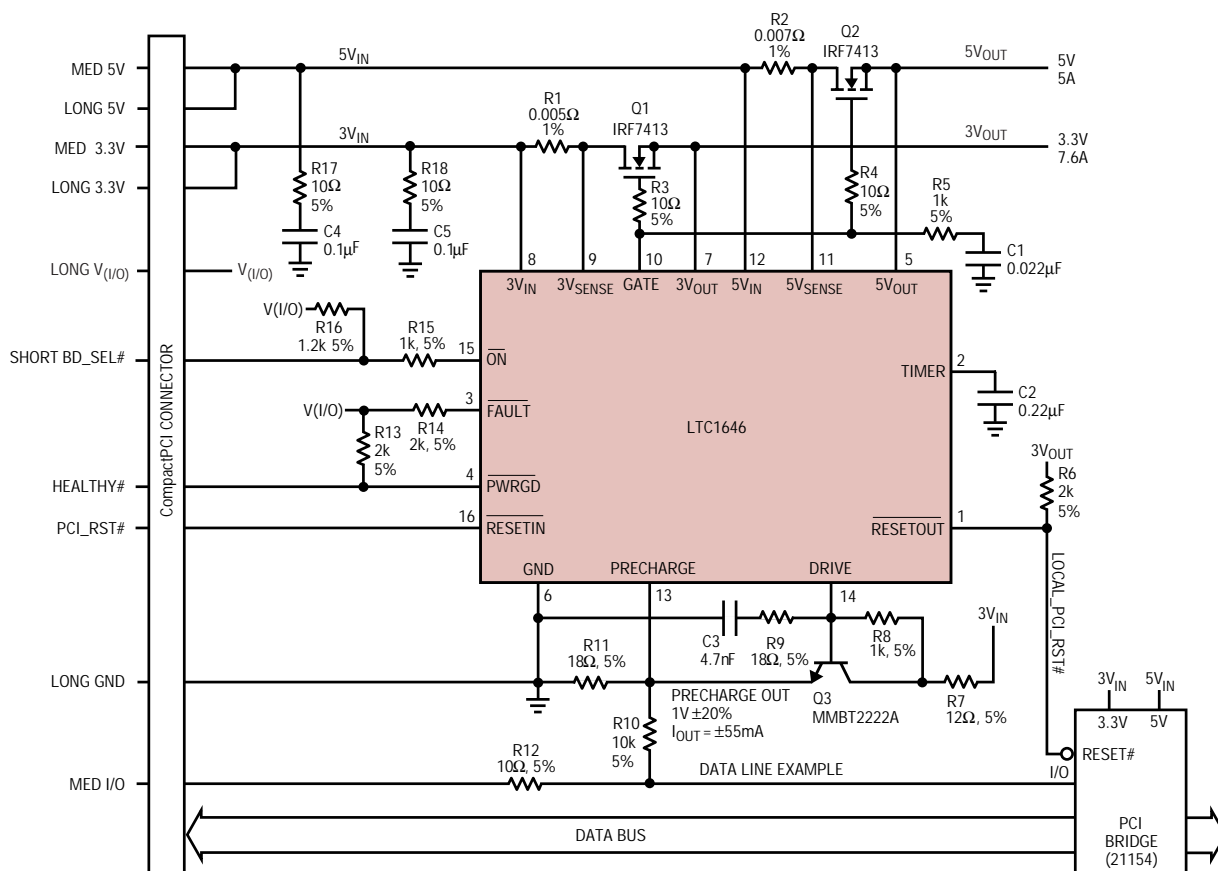


Figure 2. LTC1646 typical application

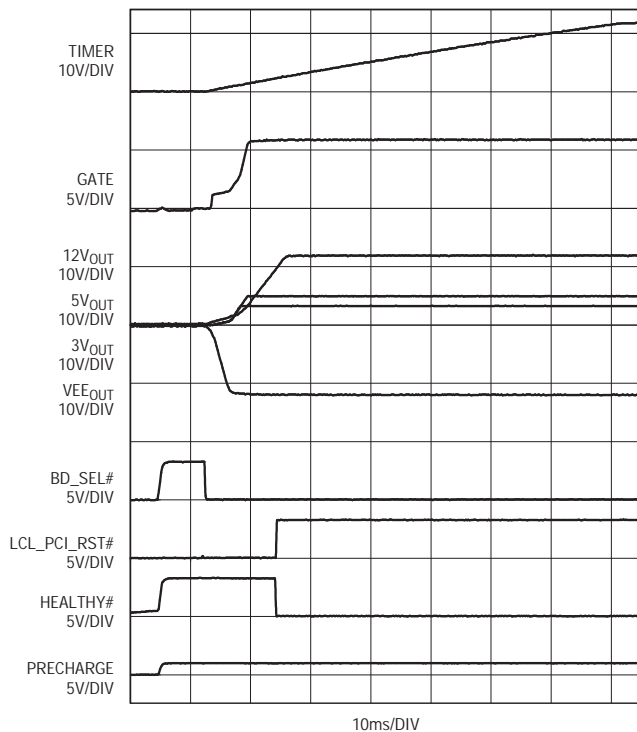


Figure 3. Typical power-up sequence

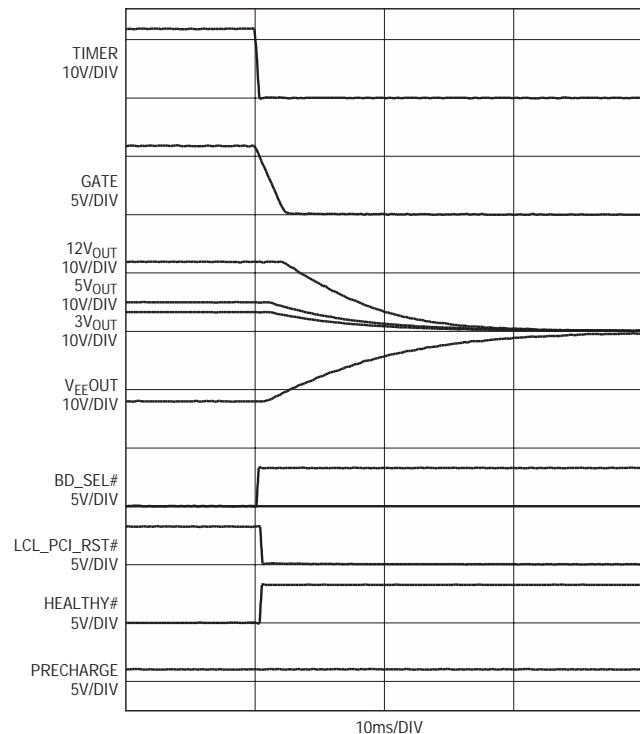


Figure 4. Typical power-down sequence

current source. Simultaneously, the capacitor connected to the TIMER pin is also charged by an internal current source ($5\mu\text{A}$ for the LTC1646, $20\mu\text{A}$ for the LTC1644). Each supply is allowed to power-up at the rate $dv/dt = I/C1$ (where I is $20\mu\text{A}$ for the LTC1646 and $50\mu\text{A}$ for the LTC1644) or as determined by the current limit and the load capacitance, whichever is slower. Current limit faults are ignored while the TIMER pin voltage is ramping up and is less than the timer threshold voltage. Once all the output supply voltages have crossed their power-good thresholds, the HEALTHY# signal is pulled low and LOCAL_PCI_RST# can follow PCI_RST#. The power cycle is complete after the TIMER pin voltage exceeds the timer threshold voltage (1.2V for the LTC1646, $V_{12VIN} - 1\text{V}$ for the LTC1644).

Power-Down Sequence

When the $\overline{\text{ON}}$ pin is pulled high, a power-down sequence begins (see Figure 4). Internal pull-down switches are connected to each of the output supply voltage pins to discharge the bypass capacitors to ground. The

TIMER pin is immediately pulled low and the voltage on the GATE pin is discharged by a $200\mu\text{A}$ current source to prevent the load currents on the 3.3V and 5V supplies from going to zero instantaneously and causing glitches on the power supplies. When any of the output voltages dips below its power-good threshold, the HEALTHY# signal is pulled high. The PRECHARGE pin voltage is held at 1V by the LTC1644 and LTC1646 independent of the state of the $\overline{\text{ON}}$ pin voltage.

Timer

During a power-up sequence, a current source ($5\mu\text{A}$ for the LTC1646, $20\mu\text{A}$ for the LTC1644) is connected to the TIMER pin and current limit faults are ignored until the voltage on this pin exceeds the timer threshold voltage (1.20V for the LTC1646 and $12V_{IN} - 1\text{V}$ for the LTC1644). This feature allows the chip to power-up CPCI cards with widely varying capacitive loads on the supplies. The timer period should be set longer than the maximum supply turn-on time but short enough not to exceed the maximum safe operating area of the pass

transistors in the event of a short circuit. The TIMER pin voltage is immediately pulled low when the $\overline{\text{ON}}$ pin voltage is pulled high.

Short-Circuit Protection

During a power-up cycle, the LTC1644 and LTC1646 rely on analog current limit to protect the supplies against short-circuit faults. To prevent excessive power dissipation in the pass transistors and prevent voltage spikes on the supplies during short-circuit conditions, the current limit on each supply is designed to be a function of the output voltage. As the output voltage drops, the current limit decreases. Unlike a traditional circuit breaker function, where huge currents can flow before the breaker trips, the current foldback feature guarantees that the supply current will be kept at a safe level and prevent voltage glitches while applying power into a short.

Contemporary hot swap controllers also rely on analog current limit as a means of protecting against short-circuit faults once a board has powered-up. In addition, these controllers tend to delay opening the

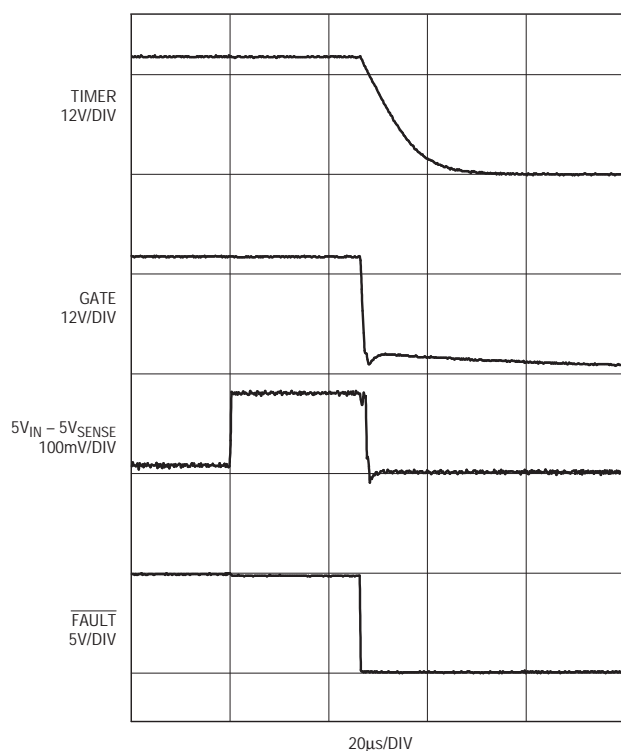


Figure 5. Overcurrent fault on 5V

circuit breaker for a period of time in order to prevent brief overcurrent conditions from triggering a fault. Although this approach guarantees that the supply current will not exceed the design limit, it has an inherent flaw: the hot swap controller deliberately compromises output voltage compliance in order to regulate supply current during an overcurrent glitch. As a result the output voltage may drop out of tolerance causing a variety of potential problems on the CPCI board, among them being the potential for asserting the LOCAL_PCI_RST# signal.

The LTC1644 and LTC1646 provide a simple solution to this problem. Both the 5V and 3.3V supplies use dual-level circuit breakers to guard against overcurrent and short-circuit faults once the power-up cycle is completed. Overcurrent faults are defined here as the condition where the voltage across the terminals of an external sense resistor exceeds 50mV but is less than 150mV. A sense resistor voltage differential greater than 150mV qualifies as short-circuit fault. During an overcurrent event, an internal timer is started, but no

attempt is made to limit current by reducing the gate voltage of the external 3.3V and 5V pass FETs. If the overcurrent condition remains after 20µs, the circuit breaker is tripped, the GATE pin is pulled down to ground and the chip latches-off (Figure 5). In the event of a short-circuit fault, however, the circuit-breaker trips without delay causing the GATE pin to be pulled to ground, and the chip latches-off (Figure 6). Toggling the /ON pin voltage low-high-low causes another power cycle to begin and resets the circuit breakers.

Power-Good and Resetout Outputs

Both the LTC1644 and the LTC1646 monitor the status of the output voltages using the /PWRGD pin. For CPCI applications, the HEALTHY# back-

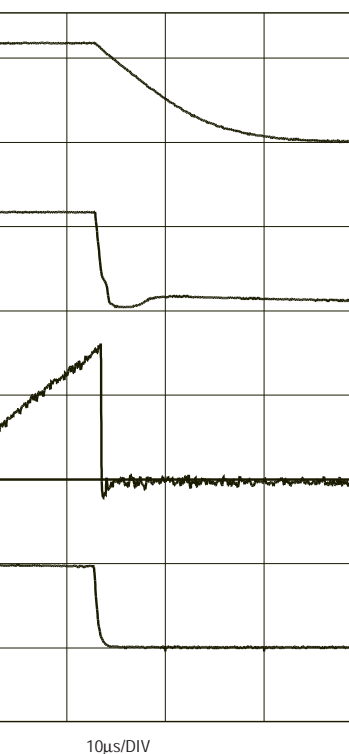


Figure 6. Short-circuit fault on 5V

plane signal should be connected to the PWRGD pin and the PCI_RST# backplane signal should be tied to the RESETIN pin. The HEALTHY# and PCI_RST# signals are combined on chip to yield the LOCAL_PCI_RST# signal (see Table 1), which is available at the RESETOUT pin. In the event that any of the output voltages drop below their power-good thresholds for more than 20µs, the HEALTHY# signal is pulled high, and the LOCAL_PCI_RESET# signal is pulled low. The delay feature prevents a system reset from occurring as a result of brief glitch on the output supply voltage.

Precharge

During hot insertion and extraction, the bus I/O connector pins will bounce before a solid connection is made or broken. The charging and discharging of these three-stated pin capacitances result in glitches that can potentially interfere with bus transactions that are occurring while a CPCI board is being inserted into or removed from the system. In order to minimize these glitches, these bus I/O pins should be precharged to 1V before the

Table 1. LOCAL_PCI_RST# truth table


PCI_RST#	HEALTHY#	LOCAL_PCI_RST#
Low	Low	Low
Low	High	Low
High	Low	High
High	High	Low

medium length CPCI connector pins make or break contact with the back-plane connector. The LTC1644 and the LTC1646 offer a solution to the precharge requirement for CPCI applications. Both parts provide a PRECHARGE pin and a DRIVE pin that are intended for use with the precharge application circuit, as shown in Figures 1 and 2. The precharge application circuit is capable of sourcing and sinking up to 55mA of current and can bias up to 128 I/O connector pins operating from $V_{(I/O)}$ voltages as high as 5V while still maintaining $1V \pm 20\%$ at the PRE-

CHARGE pin. Power for this circuit should be derived from the long $5V_{IN}$ or $3V_{IN}$ connector pins in order to guarantee that the 1V precharge output is available to bias the medium length connector pins during CPCI board insertion and extraction.

Conclusion

The LTC1644 and LTC1646 provide comprehensive solutions for CPCI Hot Swap applications. These devices incorporate several features that are tailored for CPCI, such as bus precharge and on-chip intercept of the global $PCI_RST\#$ signal. They are ca-

pable of powering up CPCI boards with wide ranges of load capacitance in foldback current limit. Once the power-up cycle is completed, dual-level circuit breakers for the 5V and 3.3V supplies offer fast, effective current limiting in the event of a short circuit without compromising output voltage compliance during brief over-current conditions, thus offering CPCI board designers a level of short-circuit protection that is unique to LTC's Hot Swap family. 

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