

Digitally Programmable Low Noise Filter/Gain Block Requires No External Parts

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Introduction

Designers of instruments and DSP-based systems now have at their disposal a continuous-time, “brick-wall” lowpass filter with digital control of the cutoff frequency (10kHz to 150kHz in 10kHz steps). The LTC1564 also offers digitally programmable gain of up to 24dB (implemented in a noise-efficient way) for dynamic range to 122dB (20 equivalent bits), and operates from a supply voltage of

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2.7V to 10.5V total (single or split supplies). No additional analog components or calculations are needed. A simple, on-chip, latching digital interface can store frequency and gain settings or can be overridden to directly control the part from its pins.

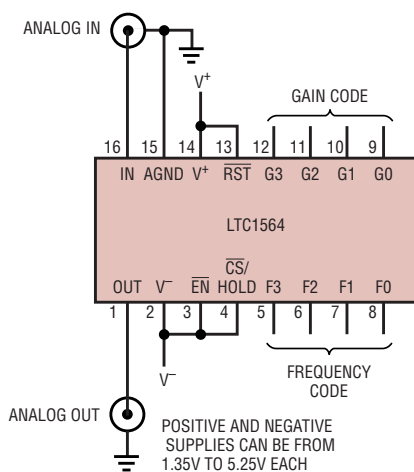


Figure 1. A high performance filter/gain block using the LTC1564 (dual-supply connection shown)

Table 1. Programming the corner frequency and gain of the LTC1564

F3	F2	F1	F0	G3	G2	G1	G0	Mode
0	0	0	1	0	0	0	0	$f_c = 10\text{kHz}$, Passband Gain = 1V/V (0dB)
1	1	1	1	0	0	0	0	$f_c = 150\text{kHz}$, Passband Gain = 1V/V (0dB)
0	0	0	1	1	1	1	1	$f_c = 10\text{kHz}$, Passband Gain = 16V/V (+24dB)
0	0	0	0	Don't Care				Mute State, Zero Gain

No programming or clocking is required beyond the straightforward frequency and gain settings. This single-chip product eliminates expensive, precision analog circuitry in applications demanding sharp roll-off, high dynamic range, amplification or programmability. The LTC1564 comes in a 16-pin plastic SSOP package.

The LTC1564 is a rail-to-rail, high resolution filter. The 8th order low-pass response with two stopband notches gives approximately 100dB attenuation at 2.5 times the passband-edge frequency, f_c (f_c range 10kHz to 150kHz), making it suitable for high resolution antialias filtering. Despite the high filter order, the wideband noise is only $33\mu\text{V}_{\text{RMS}}$ (typical) at a 20kHz corner frequency (unity gain setting, $\pm 5\text{V}$ supplies), which is 100dB below the rail-to-rail maximum signal level. Moreover, the LTC1564 incorporates a unique feature that is useful with low or wide-ranging signal levels: the output-referred noise rises only slightly at higher gain settings, so the input-referred noise floor drops significantly at these settings. At the maximum 24dB (16V/V) gain setting, the same 20kHz response just quoted has an input noise level of $2.5\mu\text{V}_{\text{RMS}}$, which is 122dB (20 equivalent bits) below the maximum unity-gain input level. (These noise levels rise by 3dB–4dB at the higher f_c settings). This dynamic range reflects the way in which the

gain is implemented. Gain control in the LTC1564 is an integral part of the filter, using a proprietary method that deliberately minimizes the total noise. This feature would be difficult to achieve with separate VGA and filter circuits. The LTC1564 is also DC-accurate, with a typical input referred offset voltage of 3mV at unity gain and 1mV at a gain of 10V/V.

Ease of Use

You don't have to be a filter expert or analog designer to use the LTC1564. There are only three analog pins: Input, Output, and a half-supply reference voltage point, AGND (Figure 1). The other pins are digital controls and power supply.

You can imagine the LTC1564 as an instrument in a box, with analog input and output jacks and two rotary switches labeled “Frequency” and “Gain.” In use, the product is not far from this metaphor. The frequency setting (“F”) and gain setting (“G”) are each four-bit codes entered through the F and G digital input pins (Table 1). Also, setting the F code to 0000 engages a “mute” state where the filter remains fully powered but the gain is a hard zero (typically –100dB), the input pin is disconnected inside the LTC1564 and output noise becomes even lower than in normal filter operation. (Those who enjoy exotic specifications can compare the maximum signal level out of the filter, using a nonzero F code, to the noise in

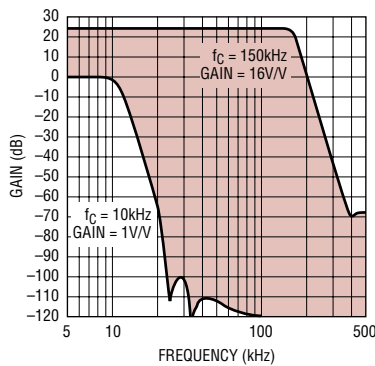


Figure 2. Measured response over range of frequency and gain codes

the “mute” state with zero F code; this ratio is typically 120dB.)

A logic 0 on the $\overline{\text{CS}}/\text{HOLD}$ pin makes the internal latches transparent so that the F and G pins control the filter directly, whereas $\overline{\text{CS}}/\text{HOLD} = 1$ freezes the F and G latches and those pins no longer influence the filter. The RST pin resets the internal F and G latches to zero at any time. $\overline{\text{EN}}$ is the chip enable pin; logic 1 disables the chip and imposes a low power standby mode. These CMOS input pins accept CMOS logic levels, either rail-to-rail or, alternatively, 0V and 5V when the part is operated from $\pm 5\text{V}$ supplies.

To make application as simple as possible, each of the CMOS digital inputs includes a small pullup or pulldown current source, nominally $10\mu\text{A}$. These current sources cause the digital input pins to float to useful logic levels by default if the pins are left unconnected. With the exception of the $\overline{\text{EN}}$ pin, which must be explicitly set to logic 0 for normal filter operation, the other digital inputs can be left open if their default values are the desired settings. The default values program the filter for a 20kHz passband edge and unity passband gain (0dB), or in other words, $F = 0010$, $G = 0000$, $\text{RST} = 1$ and $\overline{\text{CS}}/\text{HOLD} = 0$. Any of these default bits can be overridden by connecting the pin as desired. Although the digital pins would normally be connected in a printed circuit production layout, this feature minimizes the wiring necessary in prototyping or experimentation.

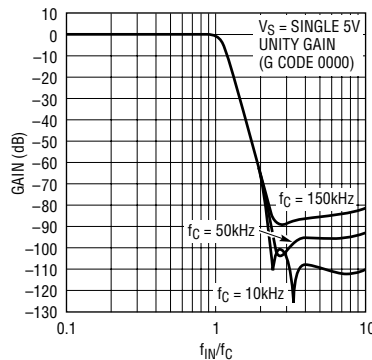


Figure 3. Overall frequency response (frequency scales normalized to f_c)

What Makes the LTC1564 Tick?

The LTC1564 contains a proprietary active-RC filter architecture (realizing eight complex poles and two imaginary-axis zero pairs) for a sharp-roll-off lowpass gain response. The architecture limits noise sources to nearly the fundamental minimum “ kT/C ” bounds, which in turn are constrained by the requirement of keeping the power consumption to manageable levels (15mA–22mA in the LTC1564). Internal capacitors are laser trimmed for precision. Internal operational amplifiers were designed “from the ground up” for this product and, in particular, for constant characteristics over the wide supply voltage range of 2.7V to 10.5V total. The LTC1564 addresses a demand for filters with roughly “100–100–100” performance: 100dB stopband attenuation, 100+dB signal-to-noise ratio (SNR) and cutoff frequencies on the order of 100kHz.

The LTC1564 architecture supports robust deep notches in the stopband. For example, with an LTC1564 set for $f_c = 20\text{kHz}$, a notch depth of -150dB was measured at approximately 52kHz using careful narrowband techniques (this measurement requires care because it exceeds the dynamic range of most test instruments).

Filtering Performance

Figure 2 compares measured frequency responses at the low and high extremes of F code (0001 for $f_c = 10\text{kHz}$ and 1111 for $f_c = 150\text{kHz}$) and

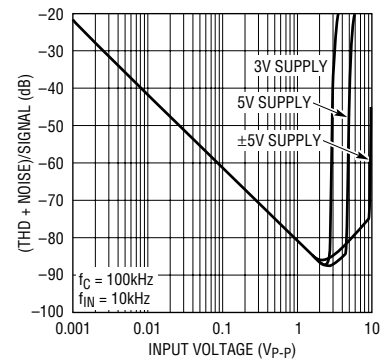


Figure 4. LTC1564 THD plus noise referred to the signal output

G code (0000 for 1V/V gain and 1111 for 16V/V gain). f_c is the passband corner, where the gain response is nominally 1dB down from its low frequency value. Figure 3 shows unity-gain response at different f_c settings on a normalized frequency scale of f_{IN}/f_c .

Large-signal linearity performance can be seen from Figure 4, showing total noise and distortion in dB referred to signal level, for a 10kHz signal with $f_c = 100\text{kHz}$, at three supply voltages (3V, 5V and 10V total supplies). This curve shows a peak signal-to-distortion ratio of 86dB to 87dB and a small-signal (noise-limited) performance of approximately 98dB below the rail-to-rail input level at 10V total supply.

Application Example: Two-Chip “Universal” DSP Front End

In Figure 5, an LTC1564 filter drives an LTC1608 16-bit 500ksps (kilo-samples/second) analog-to-digital converter (ADC) for a highly flexible, complete 16-bit analog-to-digital signal interface with variable gain, variable sampling rate and variable analog bandwidth up to 150kHz. Signal bandwidth and antialias filtering are programmed with a combination of the LTC1564’s frequency-setting “F” code and the rate of sampling controlled by the LTC1608’s $\overline{\text{CONVST}}$ clock input. Low level signals can also be amplified by the LTC1564 for high SNR, as described previously.

With the LTC1564 passband corner (f_c) set to, for example, 100kHz, a

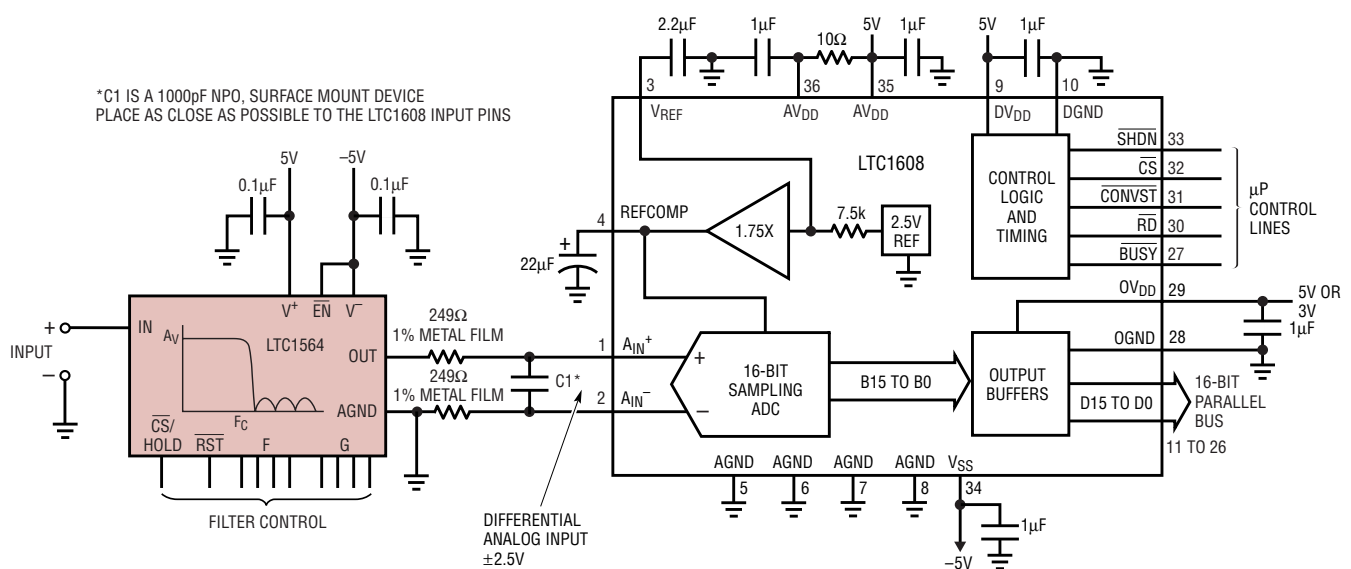


Figure 5. A universal DSP front end

sampling rate (f_s) of 500ksps in the LTC1608 ADC provides 100dB of anti-alias protection at the critical analog folding frequency of $f_s/2$, or 250kHz. This represents 2.5 times oversampling above the mathematical minimum nondistorting (or "Nyquist") sampling rate of 200ksps for a 100kHz analog bandwidth. After the ADC step, digital lowpass filtering and decimation within a DSP can reduce the sampling rate closer to the fundamental Nyquist limit without loss of information, if desired. (It can even reduce some of the ADC quantization error, though this is application-specific.)¹ Another independent option is to sample at a rate (f_s) that is lower than $5 \times f_c$. This will move the folding frequency ($f_s/2$) down from $2.5 \times f_c$ to somewhere within the analog filter's roll-off band, where the filter's rejection will not be as high as 100dB. This reduces the antialias rejection for signals at and above $f_s/2$, but still provides sufficient antialias protection in many applications, particularly

if, as is often true, the aliasable signals at and above $f_s/2$ have lower levels than the desired signals at and below f_c . The circuit of Figure 5 can accommodate either or both of these options by suitable choice of ADC sampling rate and filter F code.

Figure 6 shows a measured FFT spectrum of the digital output of Figure 5's circuit. A low level signal ($100mV_{RMS}$) was preamplified by the LTC1564 to nearly fill the input range

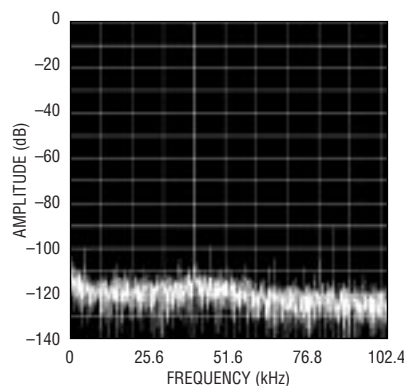



Figure 6. FFT plot of the digital output of Figure 5's circuit

of the LTC1608 ADC (the ADC output is $\pm 32,000$ counts out of a full scale of $\pm 32,768$). The input signal is 40kHz, $100mV_{RMS}$, f_{SAMPLE} is 204.8kHz for the ADC and the LTC1564 is set for a cutoff frequency of 50kHz and a gain of 16V/V ($F = 0101$, $G = 1111$). THD is 86dB, HD_2 is -88dB and SNR is 85dB. This represents a dynamic range (maximum input to minimum noise) of 115dB.

Conclusion

Featuring continuous-time filtering under digital control, only three analog pins, 122dB dynamic range and a wide power supply voltage range of 2.7V to 10.5V total, the LTC1564 is a new type of user-friendly analog filter suitable for high resolution antialiasing, reconstruction, band-limiting or instrumentation requirements. 

Note:

1. Hauser, Max W. "Principles of Oversampling A/D Conversion," *Journal of the Audio Engineering Society*, volume 39, Number 1/2 (January/February 1991).

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