

Eliminate Pipeline Headaches with New 12-Bit 3Msps SAR ADC

by Dave Thomas and William C. Rempfer

A new 12-bit 3Msps ADC brings new levels of performance and ease of use to high speed ADC applications. By raising the speed of the successive approximation (SAR) method to 3Msps, it eliminates the many drawbacks of pipelined and subranging ADCs in that speed range. It is the first clean, simple to use alternative to pipelined ADCs for applications up to 3Msps.

The LTC1412 is an ultrafast SAR ADC that offers an ideal combination of performance, size and cost. Some of its features include:

- ❑ Complete low power 12-Bit 3Msps ADC
- ❑ Great AC performance: 72.2dB SINAD and -80dB THD at Nyquist
- ❑ Great DC performance: $\pm 0.25\text{LSB}$ typical INL and DNL ($\pm 1\text{LSB}$ max)
- ❑ Three-state output bus with no pipeline delay (parallel I/O with DSP interface signals)
- ❑ Tiny SSOP-28 package

Drawbacks of Pipelined ADCs

Pipelined ADCs are great for what they do: giving the fastest speed short of using a full-flash converter. In fact, LTC manufactures both pipelined and subranging ADCs. However, these architectures do have a number of fundamental drawbacks that can cause headaches for the user. If they can be avoided, they should be. Until now, there was no alternative for 12-bit converters faster than 1.25Msps. Now there is: the LTC1412. It does everything a pipelined ADC does, but doesn't have the drawbacks.

We will look at a number of headaches experienced by users of pipelined ADCs and then look at how the new SAR ADC can eliminate them.

Headache #1: Unpredictable Behavior

Because pipelined ADCs are more complex, they have more things to go wrong and often are more prone to temperamental behavior. First, because they contain flash ADCs, they can be susceptible to sparkle code problems that historically have occurred in flash ADCs. Also, because they contain multiple flash ADCs that are pieced together with sample-and-holds, errors can occur during the piecing together process at the points where they are joined. Often, these devices include correction circuitry to try to correct any errors that occur, but errors may change with reference voltage, temperature, supply voltage or other conditions and exceed the correction range. Behavior may change and errors result as reference voltage is varied, for instance.

Headache #2: Poor Noise and SNR

Because pipelined ADCs have a series of stages, the signal is passed down many times before it reaches the end

of the pipe. In addition to the errors described above, each pass will introduce noise into the signal and degrade the SNR and noise of the converter. SNR numbers for 12-bit pipelined ADCs range as low as 64dB typical (only 10.3 effective bits). Even the best SNR is only 70dB typical (11.3 effective bits). That is several dB (or one-half of a bit) below what is possible with a good SAR ADC (see Figure 1).

Headache #3: Poor Linearity

Pipelined ADCs are often resistor-string based and therefore suffer from INL problems that result from nonlinearities in the resistor string. These nonlinearities are impossible to trim or correct for, so they remain to degrade linearity. Linearity errors reported for these ADCs can be as bad as 4LSBs.

Headache #4: Complex Reference Circuitry and Weird Biasing Schemes

Pipelined ADCs usually require multiple reference pins for their internal flash ladders. They often require weird biasing schemes for driving the top and bottom of the reference ladder. Extra hardware is often required to provide low impedances to the multiple reference pins. On some converters, fast buffer amps are required; others require multiple bypass caps (see Figure 2).

In addition to the extra hardware to generate the multiple reference voltages, the ADC range is no longer controlled by a single reference voltage. This means that more complicated circuitry may be required to change the ADC's full scale range.

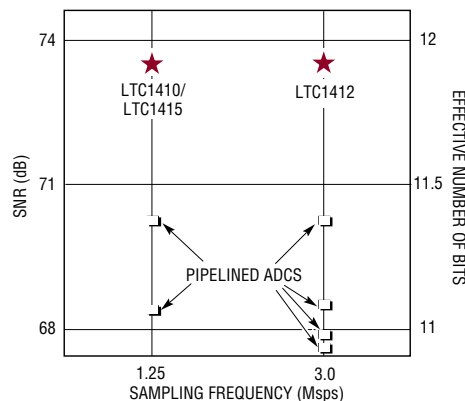


Figure 1. Because the input signal to a pipelined ADC passes from stage to stage and is resampled each time, the noise will not be as good as in a SAR ADC where the signal is sampled once and then converted. A collection of pipelined ADCs shows inferior SNR to the new 3Msps LTC1412.

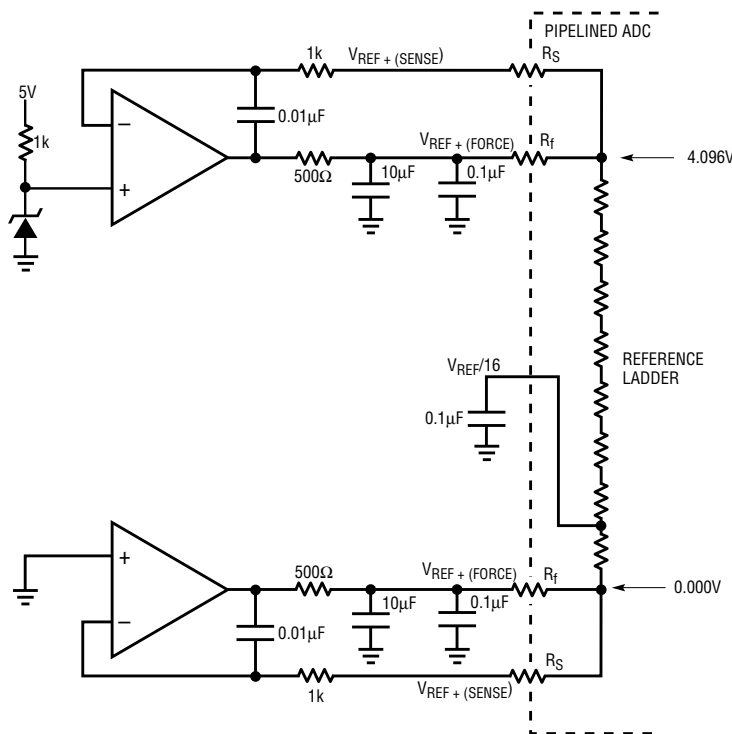


Figure 2. Multiple reference pins are required for the top and bottom of the internal flash ladders on most pipelined ADCs. Extra hardware is required to provide low impedance to the reference pins. In addition, input scaling can not be accomplished by varying a single reference voltage.

Headache #5: Complicated Input Circuitry

Another complication with pipelined ADCs is the input circuitry. Some of these ADCs require complementary differential input signals to perform correctly. Two signals 180° out of phase must be applied. Further, the signals must have an accurate common mode voltage. This means that complicated level shifting circuitry must be used to manipulate the signal into a form suitable for the ADC (see Figure 3a). Transformers are often required to get good performance from the ADC, as shown on the product data sheets (see Figure 3b).

Headache #6: Pipeline Delay

Pipeline converters have pipeline delay, which is a latency between the input sample and the corresponding data at the ADC output. Latencies can be as high as seven clock cycles. This latency can ruin the device's usefulness in many types of applications, including high speed servo-loop control systems, motor control, asynchronous or event driven sampling,

multiplexing systems and others that require a one-to-one time correspondence between each sample and the corresponding data.

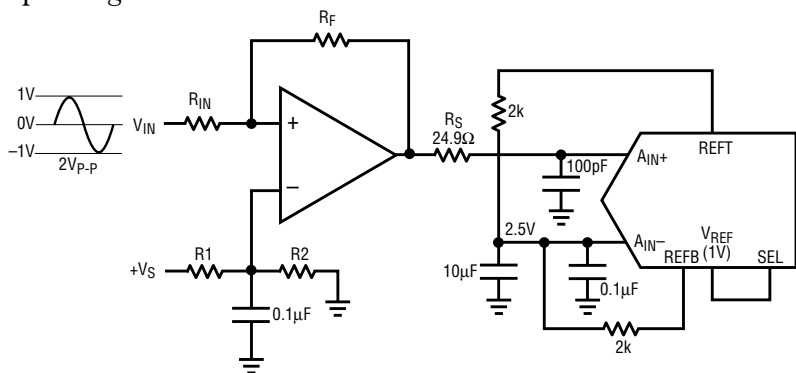


Figure 3a. Example of a pipelined ADC input-drive circuit

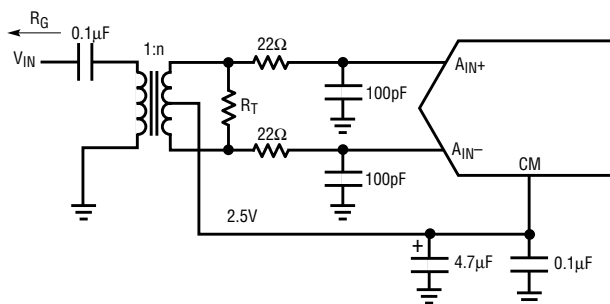


Figure 3b. Example of a transformer-coupled input-drive circuit for a pipelined ADC

In addition, these ADCs require continuous sampling and do not operate well when sampling stops and starts. When sampling stops, the internal sample-and-holds droop and samples in the pipeline are lost. Figure 8 shows how accuracy is lost as the sample rate is reduced. When conversions restart, the pipeline has to be flushed before accurate data can be received.

Moreover, many devices have dynamic internal biasing, which gets lost when the clock stops. In this case, even the biasing for the internal amplifiers is lost. This requires even more clock cycles to restore the bias in addition to those required to flush the pipeline.

**Headache #7:
No Three-State on Data Outputs**
Pipeline converters typically don't provide a way to disable the output bus. They can only be connected to a single DSP or receiving logic and cannot share a bus or have their outputs MUXed with those of other ADCs.

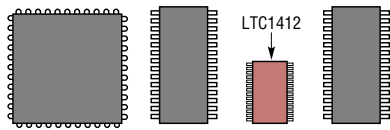


Figure 4. Package size is another disadvantage of pipelined ADCs. The more complex and much larger chips require much larger package sizes than high performance SAR devices.

Headache #8: Poor Frequency Domain Performance

Pipelined ADCs have a variety of problems that degrade frequency domain performance. First, because the signal passes from stage to stage and is resampled each time, the noise will not be as good as with a SAR ADC, where the signal is sampled once and then converted. As mentioned earlier, SNRs can be very poor for these ADCs. The best ones give up several dB (one-half bit) relative to a good SAR converter.

Some devices show terrible high frequency dynamic performance because the input signal is sampled at different times by the different parts of the internal circuitry. Because the delays of the internal circuits are not the same, the input signal is sampled at different times. Severe distortion results when high frequency signals are digitized by these devices.

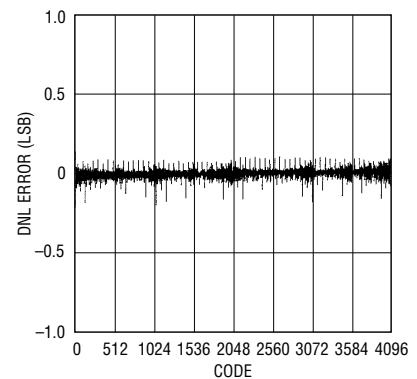
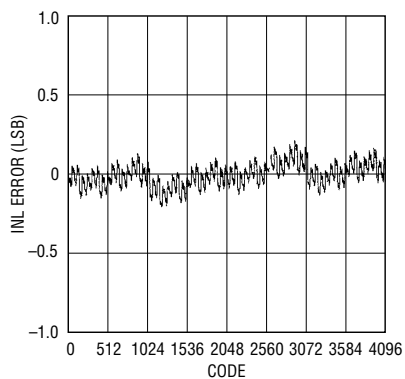


Figure 5. Because the LTC1412 depends solely on capacitor matching for accuracy (unlike pipelined ADCs), both its INL and DNL are typically 0.25LSB and do not drift with time, temperature, supply voltage or reference voltage. Maximum DNL and INL are both ± 1 LSB.

Headache #9: DC vs AC Performance Compromises

Some pipelined ADCs can't deliver good DC and AC performance at the same time. They require a low reference voltage and small input span to deliver good AC performance, but DC performance is unspecified and noise is poor. On the other hand, they require a large input span and high reference voltage to get good noise and specified DC performance, but the AC performance is poor under these conditions. In these devices, good AC and DC performance cannot be achieved simultaneously.

Headache #10: Large Package Size

Because they are complex and often have several large flash ADCs inside, the pipelined ADCs require larger package sizes than SAR converters. Package sizes range up to 44-lead PLCCs that are twice the size of the 28-lead SSOP of the LTC1412 (see Figure 4).

How Do You Spell Relief?... L-T-C-1-4-1-2

As we said, relief from pipeline headaches is now available for sample rates up to 3Msps. The new LTC1412 eliminates many of the drawbacks, as we will now see.

Excellent Linearity

Because it is a capacitively-based SAR ADC, the LTC1412 exhibits outstanding linearity, both DNL and INL. Because it depends solely on capacitor matching for accuracy (and not on amplifier gain or interstage S/H errors), both its INL and DNL are typically 0.25LSB and have virtually zero drift with time, temperature, supply voltage or reference voltage. Maximum INL and DNL are both ± 1 LSB. Figure 5 shows the outstanding INL and DNL of the LTC1412.

Simple Reference Circuitry (1 Cap) and 1-Pin Gain Adjust

Figure 6 shows the hookup of the new SAR converter. Because it is a SAR converter, a single reference voltage sets the full-scale range of the input. The range can be adjusted by driving the reference pin.

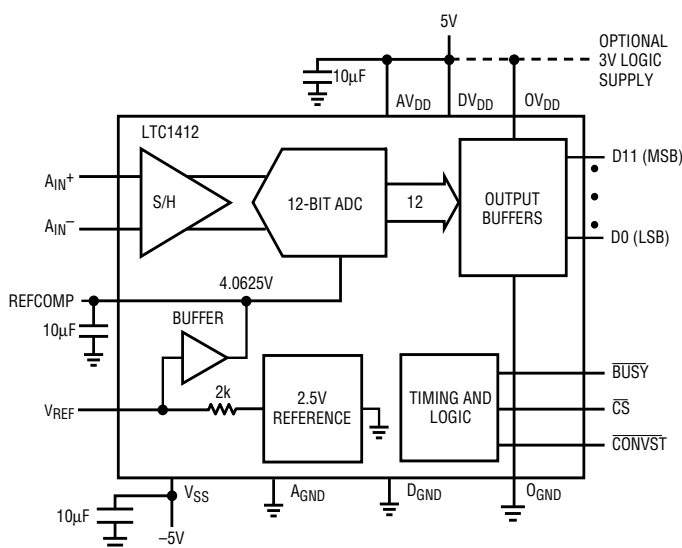


Figure 6. The hookup of the new SAR converter is simple. A single reference voltage (buffered to appear at the REFCOMP pin) controls the span of the ADC. The flexible differential input accepts differential or single-ended inputs equally well and operates without needing signal inversion circuitry or transformer coupling.

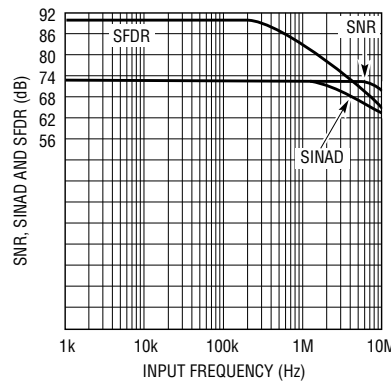
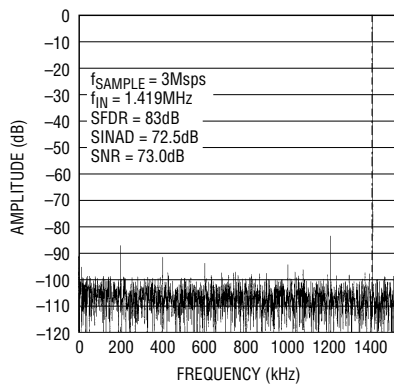


Figure 7. The LTC1412 has near perfect SNR, THD and SINAD even at the Nyquist input frequency of 1.5MHz. (a) shows SNR of 73dB. This, combined with the 80dB THD, gives a SINAD of 72.2dB at Nyquist. (b) shows how well the SNR, THD and SINAD hold up with high input frequencies.

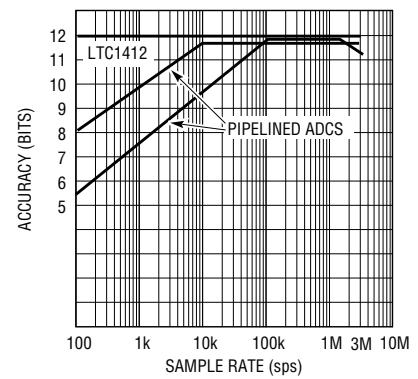


Figure 8. The zero pipeline delay of the LTC1412 makes it useful in time-domain applications such as high speed event driven sampling, DSP control loops and MUXed applications.

For slow adjustments in the span, the REF pin can be driven and the internal buffer will generate the REFCOMP voltage used by the ADC. This is appropriate in communications applications where the gain is adjusted and remains stable for a time. If fast adjustments are required, the REFCOMP pin can be driven directly. In this case, the V_{REF} pin is tied to ground to disable the buffer. This works well for applications such as imaging, where a pixel-by-pixel correction in gain is required. The capacitive SAR architecture provides inherently good linearity over a 2:1 range of reference voltages.

Very Low Noise

The LTC1412 has nearly perfect noise performance. Because of its SAR architecture, its single S/H and its single-pass conversion, it adds almost no extra noise to the input signal. Its 73dB SNR (11.83ENOB) is within 1dB of the theoretical quantization noise for a 12-bit ADC ($12 \text{ bits} \times 6.02\text{dB/bit} + 1.76\text{dB} = 74\text{dB}$ theoretical). And its low aperture jitter (<5ps) maintains this nearly perfect SNR even with inputs up to the Nyquist frequency.

No other ADC comes close to this performance at 3Msps. It is at least 3dB (one-half of an effective bit) better than any other product and is 12dB (two bits) better than some (see Figure 1). Figure 7a shows an FFT of the LTC1412 at Nyquist. The noise floor corresponds to an SNR of 73dB.

Along with the very low noise, the LTC1412 also has premier distortion performance of 80dB at Nyquist (see Figure 7a). Combined with the 73dB SNR, this gives a SINAD at Nyquist of 72dB, a figure unmatched by any competing 12-bit device and better than most 14-bit devices. Figure 7b shows that the SNR, SINAD and THD remain excellent at high input frequencies.

Outstanding AC and DC Performance Simultaneously

The LTC1412 provides the near perfect AC performance mentioned above and outstanding linearity at the same time. Figures 5 and 7 were generated without having to change the input range or any other part of the configuration.

No Pipeline Delay—Start/Stop OK—Instant Start-Up

The LTC1412 has no pipeline delay. This means that when a conversion is started, the result of that conversion is ready 300ns later. This is in contrast to converters that can have seven cycles of delay (2.3μs at 3Msps) between the conversion start and the data.

Although some applications are not sensitive to this delay, many are. For example, in many event-driven sampling systems, as each event occurs, it is sampled and the resulting data is required before the next event occurs. In these cases, the LTC1412 can digitize and provide the

result in 300ns and be ready for the next sample. In contrast, a pipelined ADC would not work in these applications because its seven cycles of delay would require 2.3μs and create the problem of flushing the pipeline for each sample.

High speed control loops are another area where data latency is unacceptable (for loop stability). The LTC1412 can support a full 3Msps data rate with no latency. Examples of this type are motor control and high speed DSP servo-control loops.

The problems with MUXing pipelined converters are gone with the LTC1412. Its zero pipeline delay makes MUXing easy because it is easy to keep track of what sample is being converted.

Finally, because there is no minimum sample rate, starting and stopping the sample clock causes no problems for the converter. The first conversion after a long pause will be fully accurate, just like any other conversion (see Figure 8). This makes the LTC1412 perfect for data acquisition systems where sampling is asynchronous and the ADC must convert after a long inactive period, without any start-up time.

Clean, Simple, Well Behaved... No Erratic Behavior

The LTC1412 is a clean machine and is easy to lay out and implement. The SAR architecture is not susceptible to sparkle codes or other erratic be-

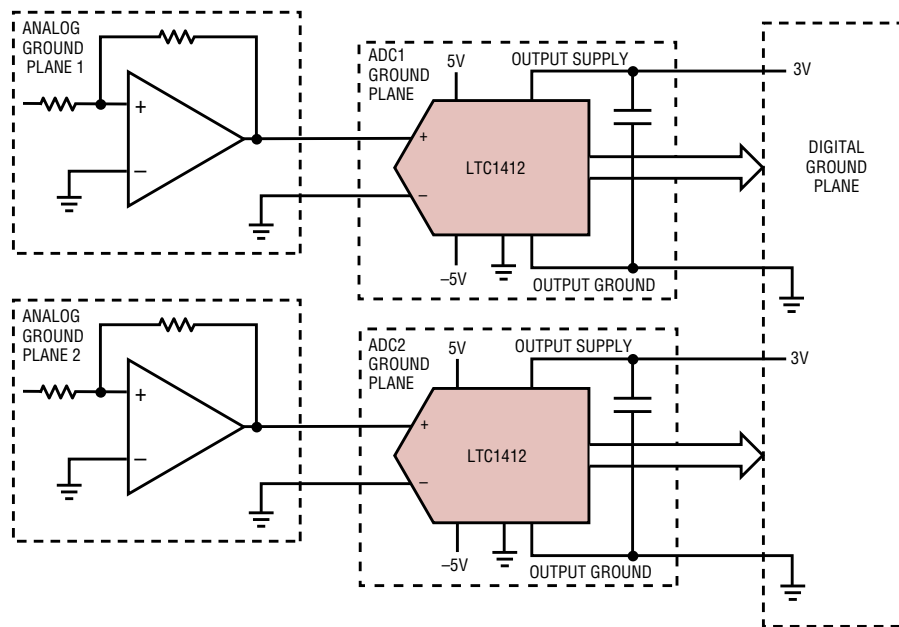


Figure 9. The LTC1412 simplifies grounding: differential inputs allow clean capture of signals, even from another board in the system. Output supply and ground allow multiple data converters to be combined at the logic section without creating system ground currents.

havior and performs very well, given reasonable care. Figure 6 shows a couple of nice features of the device. First, the differential inputs are great for eliminating noise. Routing them together on the board to the signal input will reject ground noise that may be present across the board. Second, the separate logic output supply and ground not only make for an easy interface to 3V, but simplify connections to the logic section as well.

Figure 9 shows how this can greatly simplify the grounding in large systems or multiple ADC systems. First,


the grounds in the vicinity of each ADC can be kept clean. Second, the differential inputs allow signals to be cleanly captured, even from another board in the system. Finally, the outputs of all the data converters can be combined at the logic section without generating ground currents throughout the system.

Efficient and Small Package

Because it is a simple, efficient architecture, the die size is small and the LTC1412 can fit in a tiny package. Instead of the very large packages used by pipelined parts, the LTC1412

comes in a tiny SSOP-28. A comparison to competitive pipelined parts is shown in Figure 4.

Conclusion

Pipelined ADCs are useful at very high sample rates but they do have drawbacks, as we have seen. Until now, designers had to use pipelined converters to get speeds up to 3Msps, but no more. Now there is a clean SAR alternative: the LTC1412. It does everything a pipelined ADC does, but doesn't have the drawbacks. It is a sure cure for pipeline headaches. 

for
the latest information
on LTC products,
visit
www.linear-tech.com