48 Volt Hot Swap Controller for Negative Voltages

by Henry Yun and Robert Reay

Introduction

As supply voltages for PC boards continue to drop, designers face the difficult task of minimizing the voltage drops through distributed power systems. At operating voltages of 3.3V or lower, the voltage drops across power busses, connector pins and inrush control circuitry can cause a supply voltage to drop out of tolerance. A solution to this problem is to distribute power at a high voltage, commonly 48V, and then step the voltage down to the final desired value on each board in the system, using power modules.

Most 48V power modules require an input bypass capacitor with a typical value of hundreds of microfarads. When the board is hot-plugged into a live 48V power rail, the input capacitor can draw huge inrush currents as it charges. The inrush current can cause permanent damage to the board's components and create glitches on the system power supply that can make the system function improperly.

The LTC1640H and LTC1640L provide a simple, flexible solution to –48V hot-swapping problems. The chips allow a board to be safely inserted into or removed from a live backplane with a supply voltage from –10V to –80V. They feature programmable inrush current control, programmable undervoltage and overvoltage protection, a programmable electronic circuit breaker and direct power-module-enable control.

Power Supply Control

A typical LT1640 application is shown in Figure 1. The input voltage of the power module on a circuit board is controlled by gradually increasing the gate voltage of the external N-channel pass MOSFET (Q1) in the power path. R1 provides current fault detection and R2 prevents high frequency oscillation. Resistors R4, R5 and R6 provide undervoltage and overvoltage sensing. Resistor R3 and capacitor C2 act as a feedback network to accurately control the inrush current. The waveforms are shown in Figure 2. The inrush current can be calculated with the following equation:

$$I_{INRUSH} = (45\mu A \times C_L)/\,C2$$

where C_L is the total load capacitance.

Resistor R3 helps keep Q1 off when the power pins first make contact. When the power pins make contact, they bounce several times. While the contacts are bouncing, the LT1640 senses an undervoltage condition and the GATE is immediately pulled low.

Once the power pins stop bouncing, the GATE pin starts increasing until when Q1 turns on and the GATE voltage is held constant by the feedback network of R3 and C2. When the DRAIN voltage has finished increasing, the voltage on the GATE pin then rises to its final value.

Electronic Circuit Breaker

The LT1640 features an electronic circuit-breaker function that protects against short circuits or excessive supply currents. By placing a sense

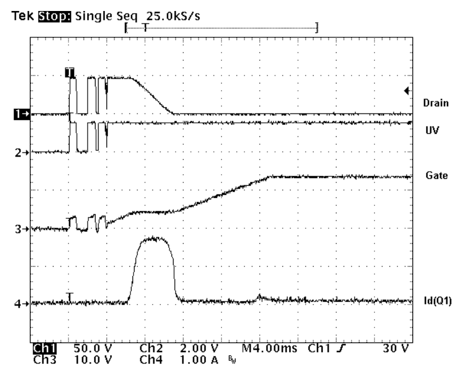

Figure 2. Inrush-current control waveforms

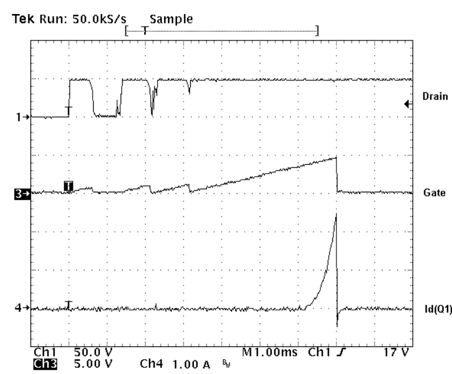

Figure 3. Short-circuit protection waveforms

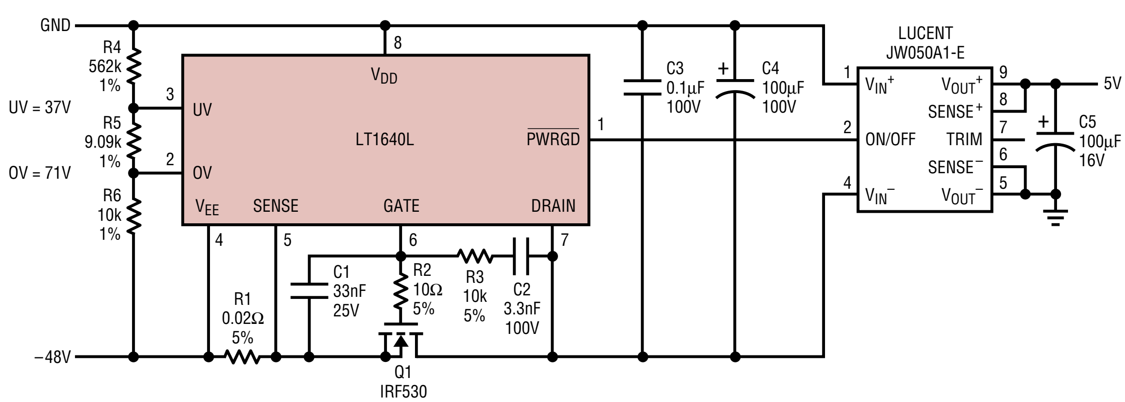

Figure 1. Typical LT1604 application with a power module

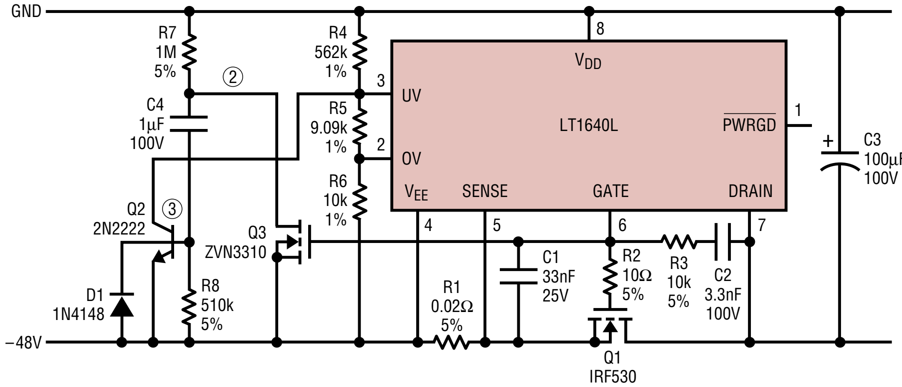

Figure 4a. This circuit resets the circuit breaker after a current fault.

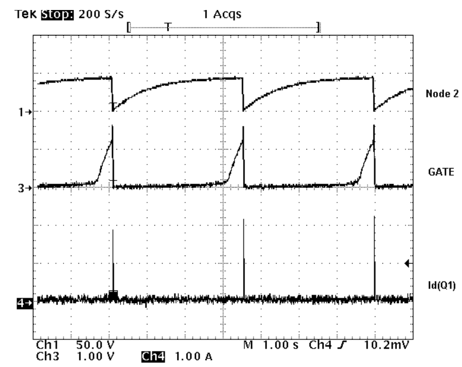

Figure 4b. Waveforms of Figure 4a's circuit

resistor between the V_{EE} and SENSE pins, the circuit breaker will be tripped whenever the voltage across the sense resistor is greater than 50mV for more than 3µs, as shown in Figure 3.

When the circuit breaker trips, the GATE pin is immediately pulled to V_{EE} and the external N-channel MOSFET is turned off. The GATE pin will remain low until the circuit breaker is reset by pulling UV low then high or cycling power to the part. A circuit that automatically resets the circuit breaker after a current fault is shown in figure 4.

Transistors Q2 and Q3, along with R7, R8, C4 and D1, form a programmable one-shot circuit. Before a short occurs, the GATE pin is pulled high and Q3 is turned on, pulling node 2 to V_{EE}. Resistor R8 turns off Q2. When a short occurs, the GATE pin is pulled low and Q3 turns off. Node 2 starts to charge C4, and Q2 turns on, pulling the UV pin low and resetting the circuit breaker. As soon as C4 is fully charged, R8 turns off Q2, UV goes high and the voltage on the GATE starts to increase. Q3 turns back on and quickly pulls node 2 back to V_{EE}. Diode D1 clamps node 3 one diode drop below V_{EE}. The duty cycle is set to 10% to prevent Q1 from overheating.

Undervoltage and Overvoltage Detection

The UV (3) and OV (2) pins can be used to detect undervoltage and overvoltage conditions at the power supply input. The UV and OV pins are internally connected to analog comparators with 20mV of hysteresis. When the UV pin falls below its threshold or the OV pin rises above its threshold, the GATE pin is immediately pulled low. The GATE pin will be held low until UV is high and OV is low.

The undervoltage and overvoltage trip voltages can be programmed using a 3-resistor-divider, as shown in Figure 5.

With R4 = 562k, R5 = 9.09k and R6 = 10k, the undervoltage threshold is set to 37V and the overvoltage threshold is set to 71V.

PWRGD/$\overline{\text{PWRGD}}$ Output

The PWRGD/$\overline{\text{PWRGD}}$ output can be used to directly enable a power module when the input voltage to the module is within tolerance. The LT1640H has a PWRGD output for modules with an active-high enable input, and the LT1640L has a $\overline{\text{PWRGD}}$ output for modules with an active-low enable input.

When the DRAIN pin of the LT1640H is more than V_{PG} (1.4V) above V_{EE} (see Figure 6), internal transistor Q3 is turned off and R7 and Q2 clamp the PWRGD pin one diode drop (~0.7V) above the DRAIN pin. Transistor Q2 sinks the module's pull-up current and the module turns off.

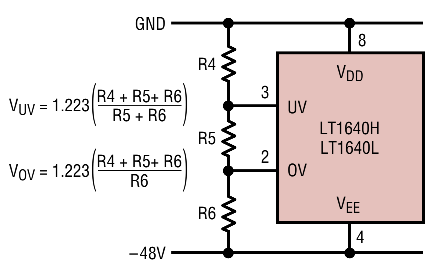

Figure 5. Undervoltage and overvoltage sensing

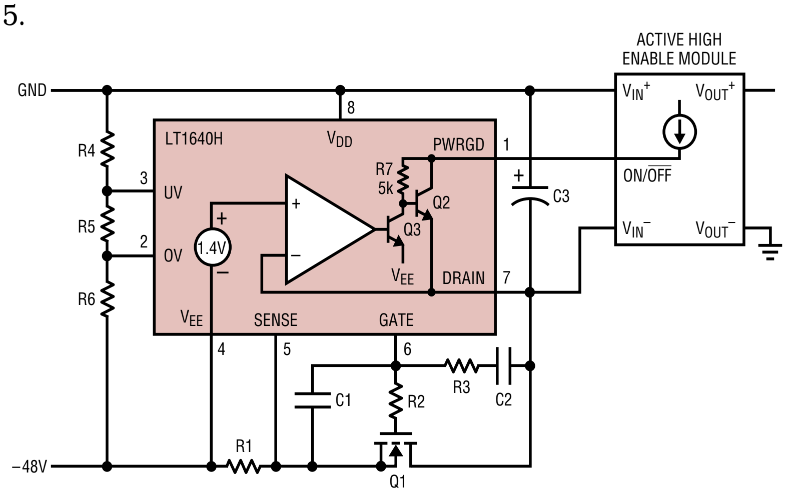

Figure 6. Active-high enable module

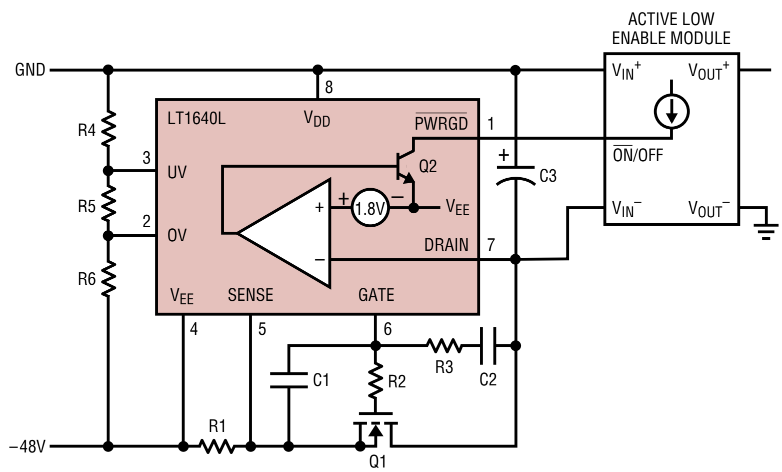

Figure 7. Active-low enable module

When the DRAIN pin drops below V_{PG}, Q3 will turn on, shorting the bottom of R7 to V_{EE} and turning Q2 off. The pull-up current in the module then flows through the R7, pulling the PWRGD pin high and enabling the module.

When the DRAIN pin of the LT1640L is more than V_{PG} (1.4V) above V_{EE}, the internal pull-down transistor, Q2, is off and the $\overline{PWRGD}$ pin is in high impedance state (see Figure 7). The $\overline{PWRGD}$ pin will be pulled high by the module's internal pull-up current source, turning the module off. When the DRAIN pin drops below V_{PG} , Q2 will turn on, and the $\overline{PWRGD}$ pin will be pulled low, enabling the module.

The $\overline{PWRGD}$ signal can also be used to turn on an LED or optoisolator to indicate that the power is good, as shown in Figure 8.

Gate Pin Voltage Regulation

When the supply voltage to the chip is more than 15.5V, the GATE pin voltage is regulated at 13.5V above V_{EE}. If the supply voltage is less than 15.5V, the GATE voltage will be about 2V below the supply voltage. At the minimum 10V supply voltage, the gate voltage is guaranteed to be greater than 6V and no greater than 18V for supply voltages up to 80V.

Conclusion

LT1640 provides a simple and flexible solution for hot swap applications. It is the first part that allows system designers to connect an 80V supply directly to the chip without any voltage step-down circuitry. It can be programmed to control the output voltage slew up rate and the inrush current. It has programmable undervoltage and overvoltage protection, and the PWRGD/$\overline{PWRGD}$ output can be tied directly to a power-module enable pin. The LT1640 simplifies the design of high voltage hot-swap control systems and combines all of these features in an 8-pin SO/PDIP package.

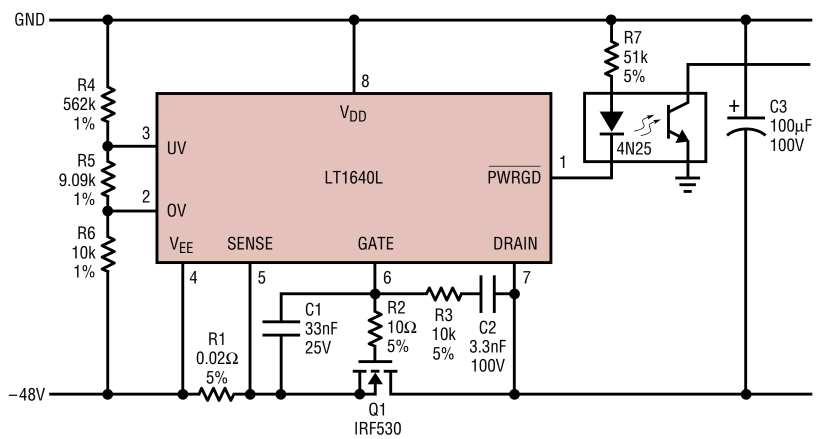

Figure 8. Using $\overline{PWRGD}$ to drive an optoisolator

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