

Complete 2-Cell-AA/USB Power Manager in a 4mm × 4mm QFN

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Introduction

One of the most popular battery solutions for consumer handheld devices is the venerable two-cell AA (alkaline or nickel-metal hydride) source, especially in GPS navigators, digital cameras and MP3 players. AA batteries are readily available, relatively low cost and offer high power density. Many of these same portable devices supplement battery power with plug-in wall adapter and offer a USB bus (for data transfer). The USB bus can also be used to provide power. The problem is how to seamlessly switch between these three disparate types of supplies: 2-cell AA, wall and USB. The solution is the LTC3456.

The LTC3456 is a complete system power IC that seamlessly manages power flow between an AC wall adapter, USB and 2-AA battery, while complying with USB power standards—all in a 4mm × 4mm QFN package (Figure 1). The device generates two separate power rails: a 3.3V (fixed) main supply and a 1.8V (adjustable) core supply. In addition, the

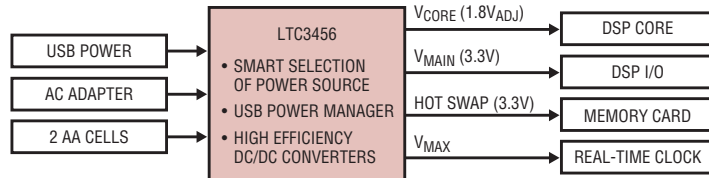


Figure 1. The LTC3456 is a complete system power management IC available in a tiny 4mm×4mm package.

LTC3456 contains a fully featured USB power manager, a Hot Swap output for powering memory cards and an un-

committed gain block suitable for use as a low-battery comparator or an LDO controller. The device also generates an always-alive V_{MAX} output, suitable

The LTC3456 squeezes a USB power manager, four high efficiency DC-DC converters, a Hot Swap controller, a low-battery indicator and much more into a 4mm × 4mm QFN package.

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About the LTC3456

The LTC3456 contains four high efficiency 1MHz fixed frequency switching regulators that operate with efficiencies up to 92%. Figure 2 shows a typical LTC3456 application. Most processors used in portable applications require dual power supply voltages. These voltages can be 3.3V for the I/O circuitry and 1.5V or, 1.8V for the processor core. Additionally, the processor might require that the power supplies startup in a specific sequence to prevent processor latch

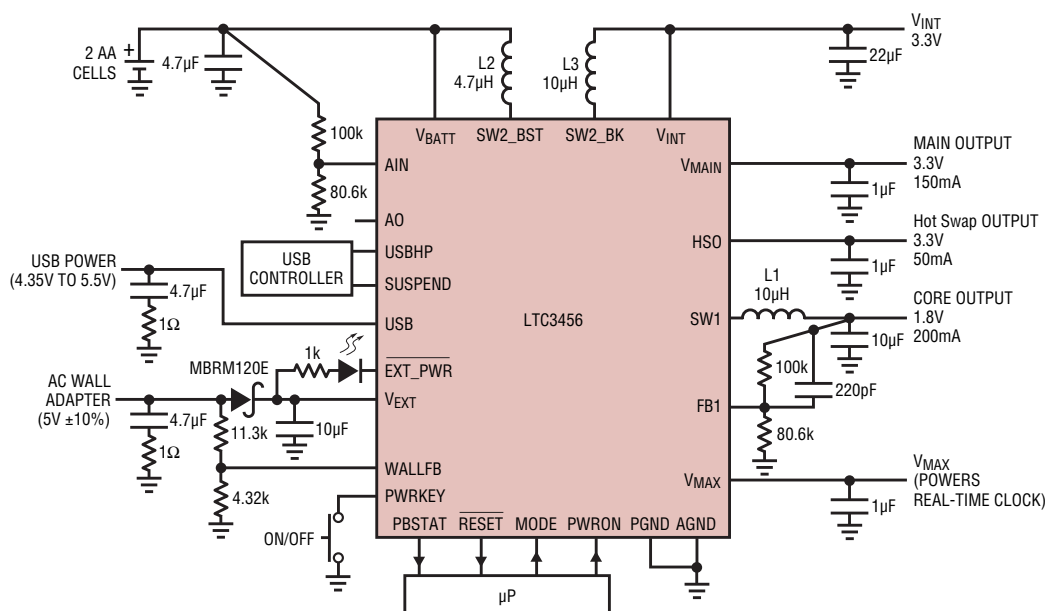


Figure 2. A LTC3456-based, complete power solution, including a 1.8V output for processor core, a 3.3V output for the I/O, a 3.3V Hot Swap supply for the memory card and a V_{MAX} output for RTC. This design uses all ceramic capacitors with minimal parts count.

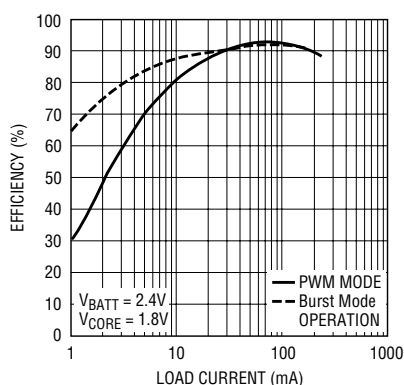


Figure 3. Core converter efficiency for Figure 2's circuit. LTC3456 is powered from the battery. Efficiency is shown for both PWM and Burst Mode operation.

up or improper initiation. Usually the core supply must come up before the I/O supply.

The LTC3456 has in built power supply sequencing for the core and main outputs. At power-up, the V_{INT} output, a fixed 3.3V supply, is the first one to power up. It supplies power to most of the internal circuitry. The amount of external loading at this output should be limited (Refer to the LTC3456 datasheet for more details). The core output, adjustable from 0.8V to 1.8V, comes up next followed by the V_{MAIN} output. The V_{MAIN} output, a fixed 3.3V supply, powers up with a delay of 0.8ms (typ) after the core output comes into regulation. The V_{MAIN} output is generated from the V_{INT} output through an internal 0.4 Ω (typ) PMOS switch and can be used to power the I/O circuitry. The 0.8ms delay gives sufficient time to the processor to stabilize the system clock and load internal registers before the peripheral circuitry powers up.

The LTC3456 produces a Core output, adjustable from 0.8V to 1.8V suitable for powering new low voltage processors (ARM and others). The LTC3456 control scheme allows 100% duty cycle operation for the core output. It provides low dropout operation when the core output is powered from the battery, thereby extending battery life. Both Main and Core converters offer Burst Mode operation (MODE Pin selectable) when powered from the battery resulting in high efficiency at light loads as seen in Figure 3. The Core converter features greater

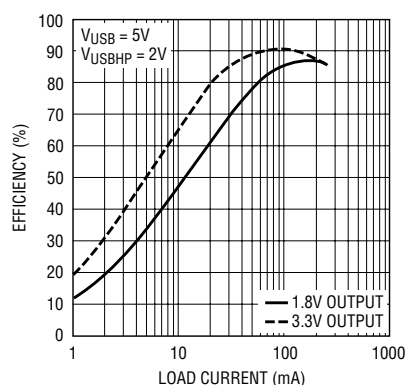


Figure 4. Core and Main converter efficiency for Figure 2's circuit. The LTC3456 is powered from the USB with the USB current limit set at 500mA (USBHP = High).

than 92% efficiency when powered from the battery. Burst Mode operation is disabled when powered from USB/wall power. Figure 4 shows the system efficiency when powered from the USB. The Main converter achieves up to 90% efficiency when powered from the USB.

The LTC3456 has a built-in Hot Swap output suitable for powering flash memory cards. The Hot Swap output features short-circuit and reverse voltage blocking capability. It allows memory cards to be hot swapped into and out of the system. It has a built-in 120mA(typ) current limit suitable for powering flash memory cards.

The LTC3456 features short-circuit protection for both the main and core outputs. It also provides output disconnect for all the outputs with the exception of the V_{MAX} output. The Core, Main and Hot swap outputs are

all discharged to ground in shutdown. The V_{MAX} output is the highest of the V_{BATT} , V_{INT} , V_{EXT} and USB voltages. This output can be used to supply a maximum of 1mA output current. The V_{MAX} output stays alive even when the IC is in shutdown and is suitable for supplying power to critical system blocks like a real time clock.

PowerPath Control

The LTC3456 contains a proprietary PowerPath control scheme that seamlessly switches over the system power from a 2-AA battery to USB/wall Power and vice versa. Figure 5 shows a simplified block diagram of the internal power-path. The AC adapter and the USB bus supply power to the switching regulators via the V_{EXT} pin. The LTC3456 contains a full featured USB power manager to control the flow of power from the USB pin via the state of the USBHP and SUSPEND pins. The current through the USB pin is accurately limited to 100mA or, 500mA depending on the state of the USBHP pin. All USB functionality can be disabled by pulling the SUSPEND pin high.

DC-DC conversion is a particularly challenging task when the 2 AA battery voltage (1.8V to 3.2V) must be boosted to generate 3.3V output, and the USB/wall power (4V to 5.5V) must be stepped down to generate the same voltage. The LTC3456 accomplishes this task via the BOOST and BUCK2 converters. This is the most efficient

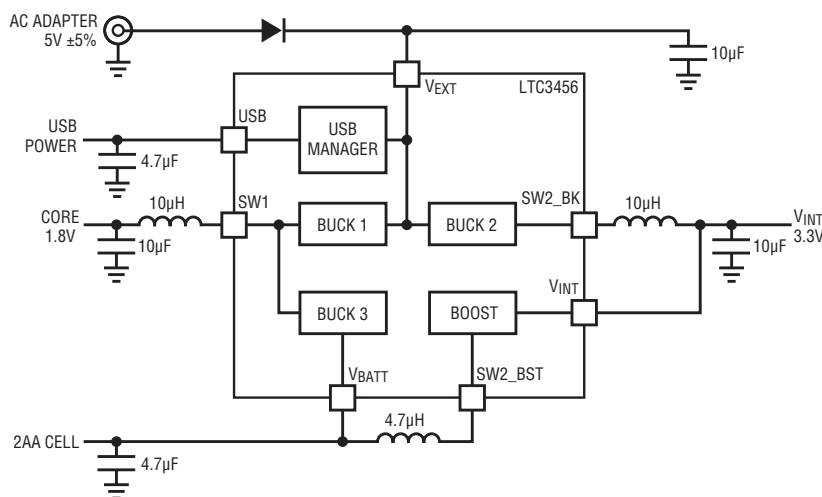
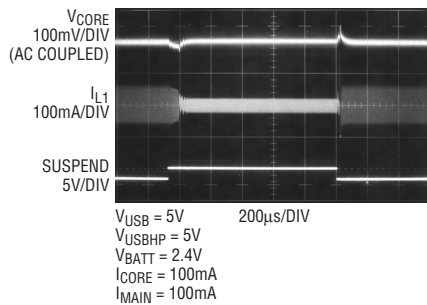
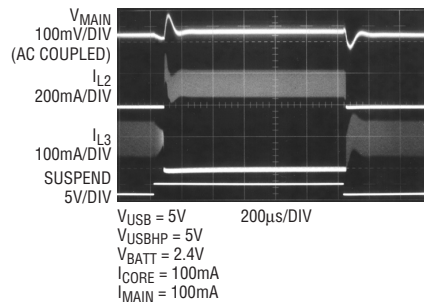


Figure 5. LTC3456's simplified block diagram showing internal PowerPath.



a. Core output transient waveforms



b. Main output transient waveforms

Figure 6. USB and 2AA Battery power supply switchover waveforms for Figure 2's circuit. The USB power is disconnected when the Suspend pin is taken high. Main and core outputs both exhibit less than $\pm 2\%$ total deviation at the time of switchover.

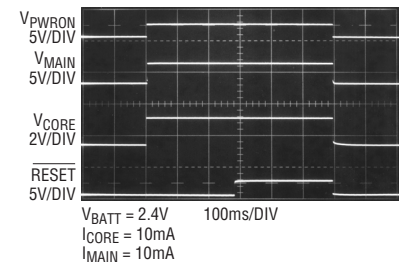


Figure 7. Power-up and power-down waveforms for Figure 2's circuit. Both V_{MAIN} and V_{CORE} outputs are discharged to ground during shutdown. Power-on reset (RESET) is held low for a delay of 262ms after V_{CORE} comes into regulation.

way of generating the 3.3V power rail. The LTC3456 achieves efficiency greater than 90% when generating 3.3V output from the battery or USB/wall adapter. The core output (1.8V) is generated via BUCK1 (USB/wall Powered) and BUCK3 (Battery Powered) converters. The unique topology of LTC3456 generates the 1.8V rail via a single inductor resulting in a cost and space saving. It achieves efficiency greater than 92% when generating the 1.8V output from the battery. The various operational modes of LTC3456 are summarized in Table 1.

Portable devices are required to seamlessly switch-over from the battery power to USB or wall power and vice versa to ensure smooth system operation. As an example, a user is playing music on a portable MP3 player with the USB cable connected. If the USB cable is suddenly yanked off the device, the user should be able to continue listening to the music without any interruption. The LTC3456 makes it possible through seamless switchover of system power.

Figure 6 shows USB and 2-AA battery power supply switchover waveforms for Figure 2's circuit. The USB power is unavailable when the Suspend pin is taken from low to high. Main and core outputs both exhibit less than $\pm 2\%$ total deviation at the time of switchover making the switchover seamless to the processor core and the peripheral circuitry.

Easy Interfacing with a Microprocessor

The LTC3456 simplifies the task of interfacing with a micro-processor. The PWRON, PWRKEY, PBSTAT and RESET pins provide all the required system information to the processor and simplify power sequencing. The PWRON, PWRKEY and PBSTAT keys simplify the task of orderly powering-up and shutting down the IC. The datasheet contains the timing diagram and gives detailed information about their operation.

The LTC3456 also contains power-on reset circuitry (accessed via pin RESET) that is active during both

power-up and shutdown. The power-on reset is required to hold the processor in its reset state at power-up and it must keep the processor from starting operation until all system power supplies have stabilized. The LTC3456's built in power-on reset circuitry monitors both the V_{INT} (3.3V) and Core (1.8V) voltages and interfaces to the processor via the RESET pin. The RESET pin is held low during initial power-up. When both the Main and Core outputs come into regulation, a reset delay timer gets activated. There is a full 262ms timeout before RESET is released and the processor is allowed to come out of reset and begin operation. The timeout delay of 262ms gives sufficient time for the processor to initialize the internal registers/RAMs. During power-off the RESET pin is again pulled low. This prevents the micro-processor from entering into any random operational modes.

Figure 7 shows the power-up and power down waveforms for the circuit of Figure 2 in battery powered mode. The RESET circuitry works similarly

Table 1. Summary of LTC3456 PowerPath operational modes and features

AC ADAPTER	USB POWER	2 AA CELLS
Highest priority for powering the IC	Medium priority for powering the IC	Lowest priority for powering the IC
Battery loading < 2 μ A	Battery loading < 2 μ A	Burst Mode operation (User Selectable) conserves battery energy
Internal soft-start circuitry limits current drawn from the adapter at start-up	USB pin current accurately limited to 100mA or 500mA	Battery inrush current regulated during power-up. Additionally, internal soft-start limits input current at start-up.
AC adapter (min) voltage set via the WALLFB Pin	USB (min) voltage set to 4V	Battery (min) voltage indicator set via the AIN Pin

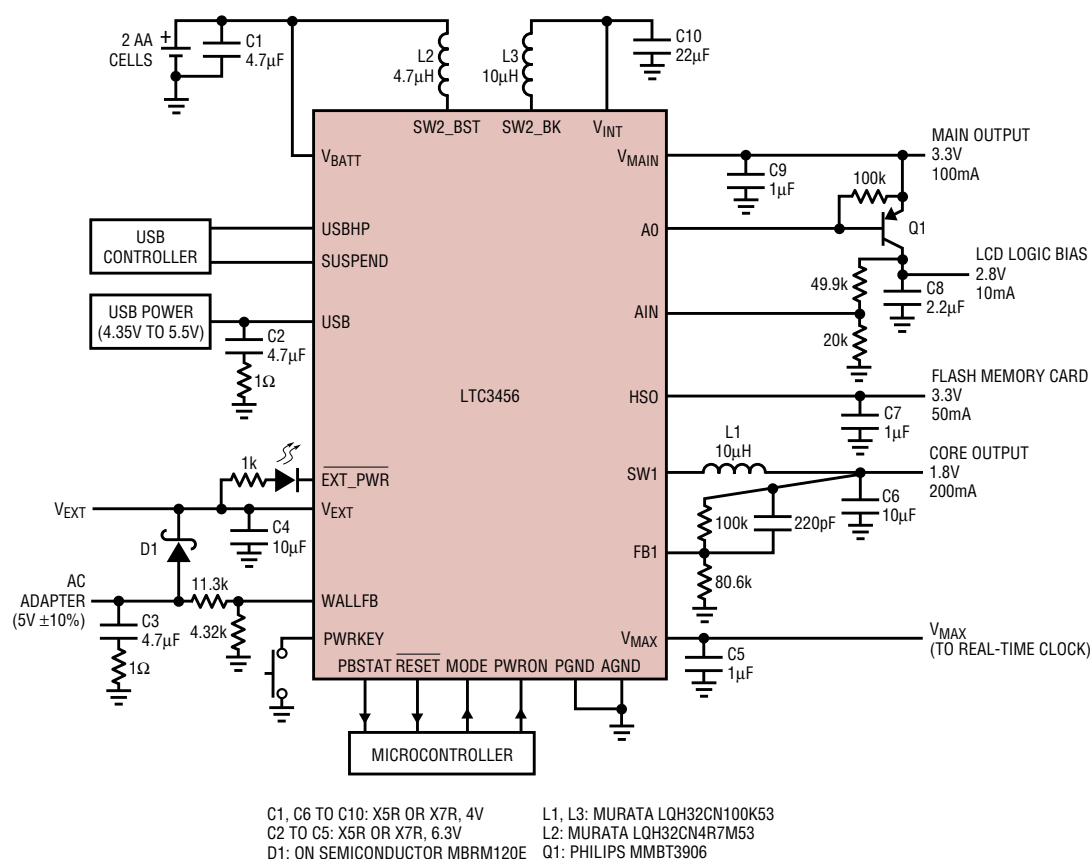


Figure 8. A 2-AA-cell-powered, complete power supply for GPS navigation system. Note that the uncommitted gain block (Pins AIN and AO) is configured as an LDO controller to generate an auxiliary 2.8V output.

when battery or externally powered. The $\overline{\text{RESET}}$ pin is held low for a delay of 262ms after V_{CORE} comes into regulation. When the IC is shut-down, both V_{MAIN} and V_{CORE} outputs are disconnected from the input power and discharged to ground. This prevents the outputs from being stuck in an indeterminate logic-level state and adversely affecting the operation of the microprocessor. It also ensures that the outputs rise in a predictable fashion during power-up.

Voltage Monitoring

The LTC3456 has an on-chip gain block that can be used for low-battery detection, with the low battery trip point set by two resistors (Figure 2) at the AIN pin. The nominal voltage at AIN is 0.8V. The AO pin is an open-drain logic output that sinks current whenever the voltage at the pin AIN falls below 0.8V. The gain block can also be configured to drive an external PNP or PMOS transistor to generate an auxiliary voltage.

In addition, the LTC3456 has on-board voltage comparator circuitry to detect the presence of USB or wall power, with a status output at the $\overline{\text{EXT_PWR}}$ pin. The open-drain logic output of $\overline{\text{EXT_PWR}}$ is capable of sinking up to 5mA, suitable for driving an external LED. The on-board voltage detectors continuously monitor the status of the USB voltage and AC adapter voltage (via the WALLFB Pin). Whenever the USB or, wall power is available and in regulation, the $\overline{\text{EXT_PWR}}$ pin is pulled low.

Portable GPS Navigator Power Supply

Today's portable GPS navigators run off two AA batteries or an AC adapter and come equipped with a USB bus (for data transfer). Long battery life and small system size are the key requirements for the power supply. The microprocessor used in GPS navigators usually require at least two different voltage supplies: typically 3.3V for the I/O circuitry and 1.5V or

1.8V for the processor core. The navigator might also require an auxiliary 2.8V supply voltage to bias the LCD display controller IC.

Figure 8 shows a complete, compact and efficient power supply for a portable GPS navigator. The V_{MAIN} (fixed 3.3V) provides power to the I/O circuitry. The power supply for the processor core, V_{CORE} , is set at 1.8V and can be adjusted by changing the feedback resistor ratio. The 3.3V Hot Swap output powers flash memory cards. The LTC3456 contains an uncommitted gain block (Pins AIN and AO) that can be used as a low-battery indicator or an LDO controller. The circuit in Figure 8 shows the gain block being used as an LDO with an external PNP to generate an auxiliary 2.8V output voltage from the Main output. The auxiliary 2.8V supply is being used to power an LCD controller IC. The V_{MAX} output of the LTC3456 stays alive even in shutdown and is used to supply power to a real-time clock.

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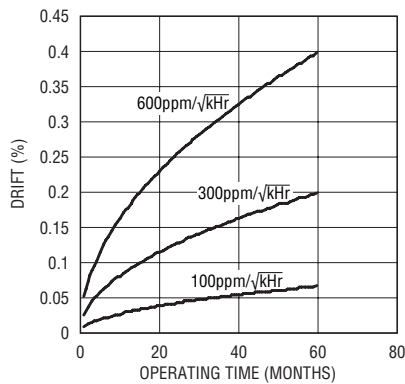


Figure 6. Comparison of 5-year drift at 100ppm/√kHz, 300ppm/√kHz and 600ppm/√kHz

Drift calculations assume that the part is in continuous operation during the entire time period of the calculation. The movements of ions which results in drift is usually aided by electric fields in the operating parts, and drift is substantially lower if the parts are not powered up during the entire period of drift. Conservative calculations would use a tenth of the drift specification for time when power is not applied to the part.

Switching the DIV Pin

The DIV input pin on the LTC6906, similar in many ways to the DIV pin on other LTC silicon oscillators, is a three state input, capable of resolving three different states: high, open and low. Three state input pins allow greater functionality in low pin-count packages, and are compatible with the tri-state outputs of many microcontrollers. Static configuration is easily accomplished by tying the pin to either the positive supply or ground, or leaving it floating.

In the OPEN state, the DIV pin of the LTC6906 is reasonably immune to noise commonly found on PC boards, but care should be taken to avoid routing a long floating trace off the pin, or

routing the pin driving that trace next to a line with strong AC signals. The noise immunity of the DIV pin can be easily improved by adding a capacitor to ground, or a series resistor of up to 100kΩ placed near the DIV pin.

In normal operation, the DIV pin uses a small current of about 1μA to pull the DIV pin voltage close to half of the power supply voltage. Therefore, if the pin is left open, any extra capacitance on the pin slows its settling to the OPEN state.

Applications that use the DIV pin to switch frequency in real time need to take into account that, because it is designed for low power operation, the DIV pin buffer circuit is slow, with delays up to around 12μs between activation of the DIV pin and changes in the output of the LTC6906. This switching delay must be accounted for in the application, or an external frequency divider can be substituted for the internal frequency divider in order to decrease the frequency change response time.

Manipulating the SET Pin

The LTC6906 can be configured in applications where the SET resistor needs to be changed for operation at different frequencies. When changing the SET resistor, best performance and accuracy is obtained by placing the switching mechanism between the set resistor and GND, not between the set resistor and the SET pin (see Figure 7).

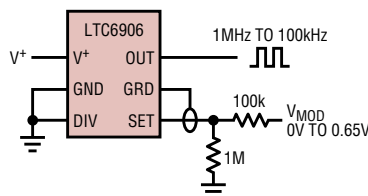


Figure 8. Modulating the SET pin current through a resistor provides greater immunity to noise coupling.

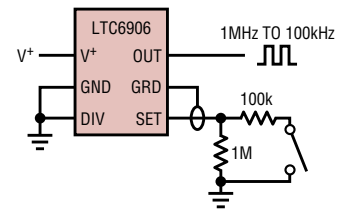


Figure 7. Switching in different SET resistors

The SET pin is sensitive to interference from external capacitance or signals, and isolation through the SET resistor reduces this sensitivity.

The LTC6906 is not ideally suited to current modulation through the SET pin because in order to save power, the voltage on the SET pin is not regulated over temperature or load. This results in the modulation of the frequency being a function of the set pin voltage as well as the set pin current. The frequency can still be modulated through the SET pin, but the relationship between the modulation current or voltage and the output frequency is not very accurate since it depends on the poorly defined SET pin voltage.

The circuit in Figure 8 shows a modulation method that results in low jitter and stable performance. By modulating the SET pin current through a resistor, the effects of parasitic capacitance on the initial frequency accuracy are reduced.

Conclusion

The LTC6906 is a micropower oscillator with 0.65% accuracy and very low jitter. Its small size, simple configuration and extremely low power consumption make it ideal for low power applications driving microcontrollers, FPGAs and providing a clock reference for battery powered devices.



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Conclusion

The LTC3456 is a complete system power management IC that seamlessly manages power flow between an AC adapter, USB cable and 2-AA battery supply. A host of features, including

an integrated USB power manager, high efficiency DC-DC converters, a Hot Swap controller and a Low-Battery Indicator, are squeezed into a 4mm × 4mm QFN package. The external components count and overall system

cost are minimized. Simplicity, design flexibility, a high level of integration and small size makes LTC3456 an ideal choice for powering many portable USB devices. 