

Quad IO-Link Master with Higher Current SIO Channels

Design Note 566

Eric Benedict

Introduction

IO-Link is a communication standard for a point-to-point, 3-wire interface to smart sensors and actuators found in industrial applications. IO-Link extends the traditional interface capabilities of these devices from a simple NC/NO switch interface (standard IO or SIO mode) to a bidirectional intelligent interface capable of sending additional information via coded switching at one of three different speeds (COM1—4.8kb/s, COM2—38.4kb/s or COM3—230.4kb/s). In addition to the data pin (C/Q), the IO-Link Type A interface has a 24VDC power supply pin (L+) and a common return pin (L-).

When an IO-Link master powers up, it interrogates each connected device to determine the proper operational mode for the device: SIO, COM1, COM2

or COM3. This allows for a mixture of legacy and IO-Link enabled devices to operate seamlessly in the same system.

The **LTC®2874**'s rated CQ output current is 110mA. Higher currents up to 440mA may be obtained by paralleling channels. While this exceeds the IO-Link specifications, some non-standard SIO applications may require even larger currents to be sourced and/or need to maintain the functionality of the four independent channels. This article shows how to repurpose the LTC2874's hot swap channels to source larger currents for SIO loads (referred to as SIO+ mode) while maintaining the IO-Link features and capabilities of the LTC2874.

LT, LT, LTC, LTM, Linear Technology and the Linear logo are registered trademarks of Analog Devices, Inc. All other trademarks are the property of their respective owners.

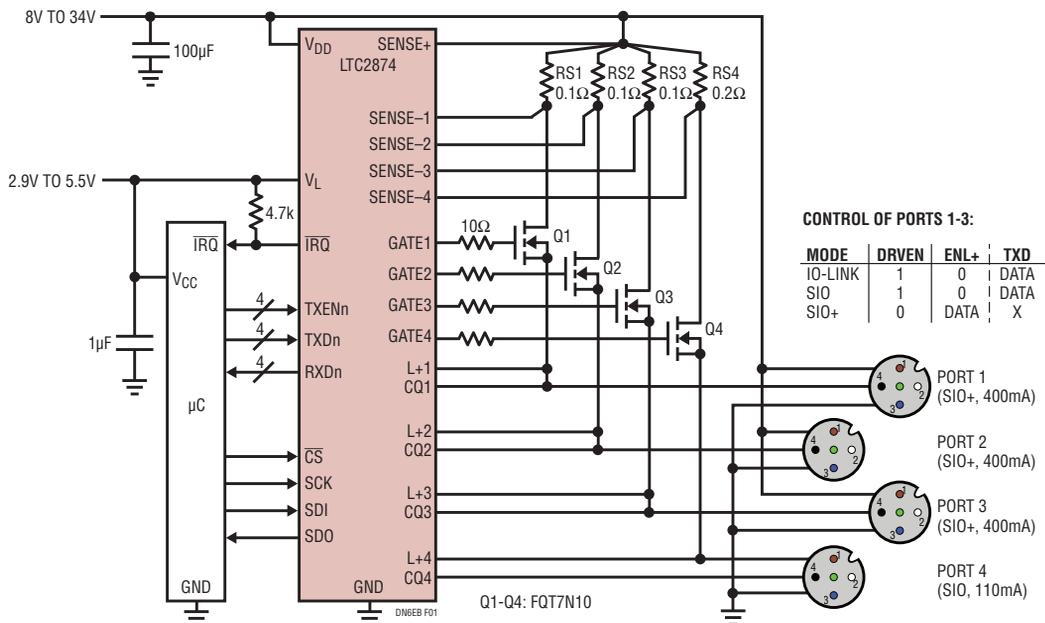


Figure 1. LTC2874, Quad IO-Link Master Configured with Three High Current SIO Ports (SIO+) and One Normal SIO Current Port with L+ Hot Swap

Circuit Description

Arbitrarily large sourcing currents are available in SIO+ mode by connecting the channel's hot swap controller output to its corresponding CQ pin as shown by ports 1–3 in Figure 1. For the high current port(s), the hot swap feature for L+ is not available; however, an external hot swap controller can be added for applications where this is desired. LTC2874 hot swap controllers not used for SIO output are available for normal L+ or other use, as shown by port 4 in Figure 1.

During normal IO-Link or SIO operation, the L+ MOSFET is OFF and the CQ output operates normally via TXEN, TXD and RXD. All IO-Link functionality is maintained, including full speed communications at COM3 speed and wake-up pulse generation.

During SIO+ operation, the L+ MOSFET is controlled via the SPI register interface and CQ is disabled (TXEN is low or under SPI register control). The upper nibble of register 0xE controls the L+ MOSFETs. During SIO+ mode, the switching frequency is limited to approximately COM1 speed.

While the LTC2874 will not be damaged if both the CQ and L+ outputs are active at the same time, this operating mode is not recommended since the output waveform's rise and fall trajectories are non-monotonic. These trajectories arise due to the interaction of the timing differences between the channels and the various current limits and source resistances.

The maximum output current for SIO+ mode is determined by the choice of MOSFET and sense resistor RS. The current limit is set by $50\text{mV}/R_S$. The typical current limit for the circuit in Figure 1 is 500mA. Accounting for tolerance and variation results in an output rating of 400mA for the port. The MOSFET must be selected to handle the voltage, current, and safe operating area (SOA) requirements. See the LTC2874 data sheet for more details.

The output capacitance of the MOSFET contributes approximately 60pF toward the maximum of 1nF that is permitted by the IO-Link standard.

Because this circuit parallels two drivers, the inactive driver acts as a capacitive load on the active driver.

When the active driver changes state, it will generate a charging current in the inactive driver. This effect is more noticeable during IO-Link operation due to the larger capacitance of the MOSFET and faster edge rate of the CQ driver. To prevent the charging current pulses from creating ringing when the active driver turns off, minimize the parasitic inductance between the MOSFET source and C/Q driver output.

Figures 2 and 3 show operational waveforms for a single SIO+ capable port driving a resistive load while operating in either SIO+ or normal IO-Link mode. The supply voltage is 24V and the resistive loads are 56 Ω and 200 Ω , respectively.

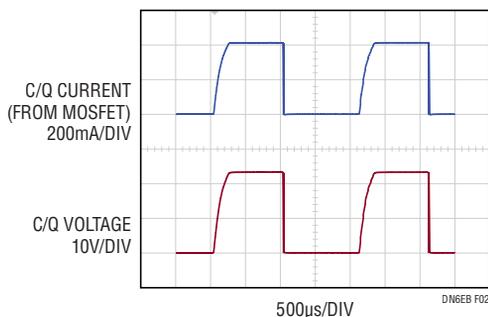


Figure 2. SIO+ Operation

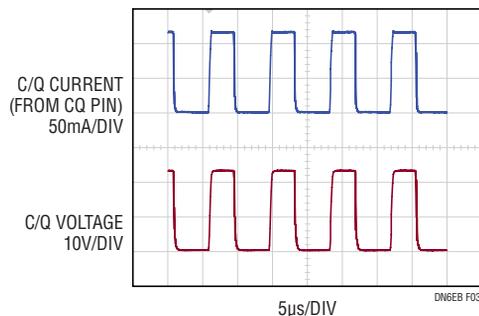


Figure 3. IO-Link Operation of a SIO+ Capable Port with C/Q at COM3 Speed

Conclusion

Arbitrarily large currents for LTC2874 operation in SIO+ mode may be obtained by repurposing the hot swap channels as higher current SIO drivers.

Data Sheet Download

www.linear.com/LTC2874

For applications help,
call (408) 432-1900