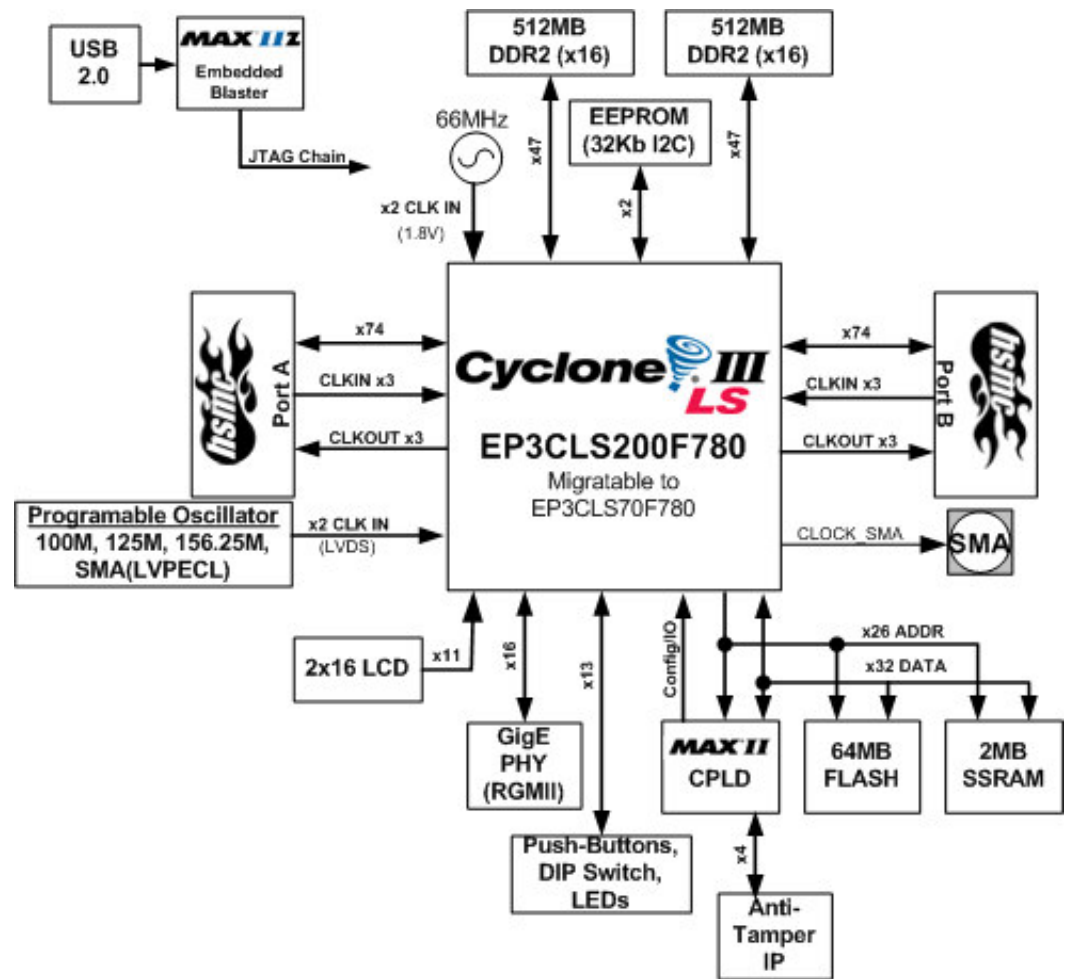


1. Project Drawing Numbers:	
Raw PCB	100-0320911-B1
Gerber Files	110-0320911-B1
PCB Design Files	120-0320911-B1
Assembly Drawing	130-0320911-B1
Fab Drawing	140-0320911-B1
Schematic Drawing	150-0320911-B1
PCB Film	160-0320911-B1
Bill of Materials	170-0320911-B1
Schematic Design Files	180-0320911-B1
Functional Specification	210-0320911-B1
PCB Layout Guidelines	220-0320911-B1
Assembly Rework	320-0320911-B1

Cyclone III LS F780 Development Kit Host Block Diagram

[illegible]

PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Revision History
2	C3 LS FPGA Package Top
3	Cyclone III LS Bank 1 & 2
4	Cyclone III LS Bank 3 & 4
5	Cyclone III LS Bank 5 & 6
6	Cyclone III LS Bank 7 & 8
7	Cyclone III LS Config, JTAG
8	Cyclone III LS Clocks
9	Clock Circuitry
10	EPM2210 System Controller
11	SRAM & FLASH
12	USB 2.0
13	10/100/1000 Ethernet (Port 0)
14	10/100/1000 Ethernet (Port 1)
15	DDR2 SDRAM
16	DDR2 SDRAM POWER & TERM
17	HSM Connectors
18	HSM Termination
19	User IO Cyclone III LS
20	User IO EPM2210
21	Power 1
22	Power 2
23	Power Monitor
24	Cyclone III LS Power
25	Decoupling
26	
27	

Title	Cyclone III LS FPGA Development Board
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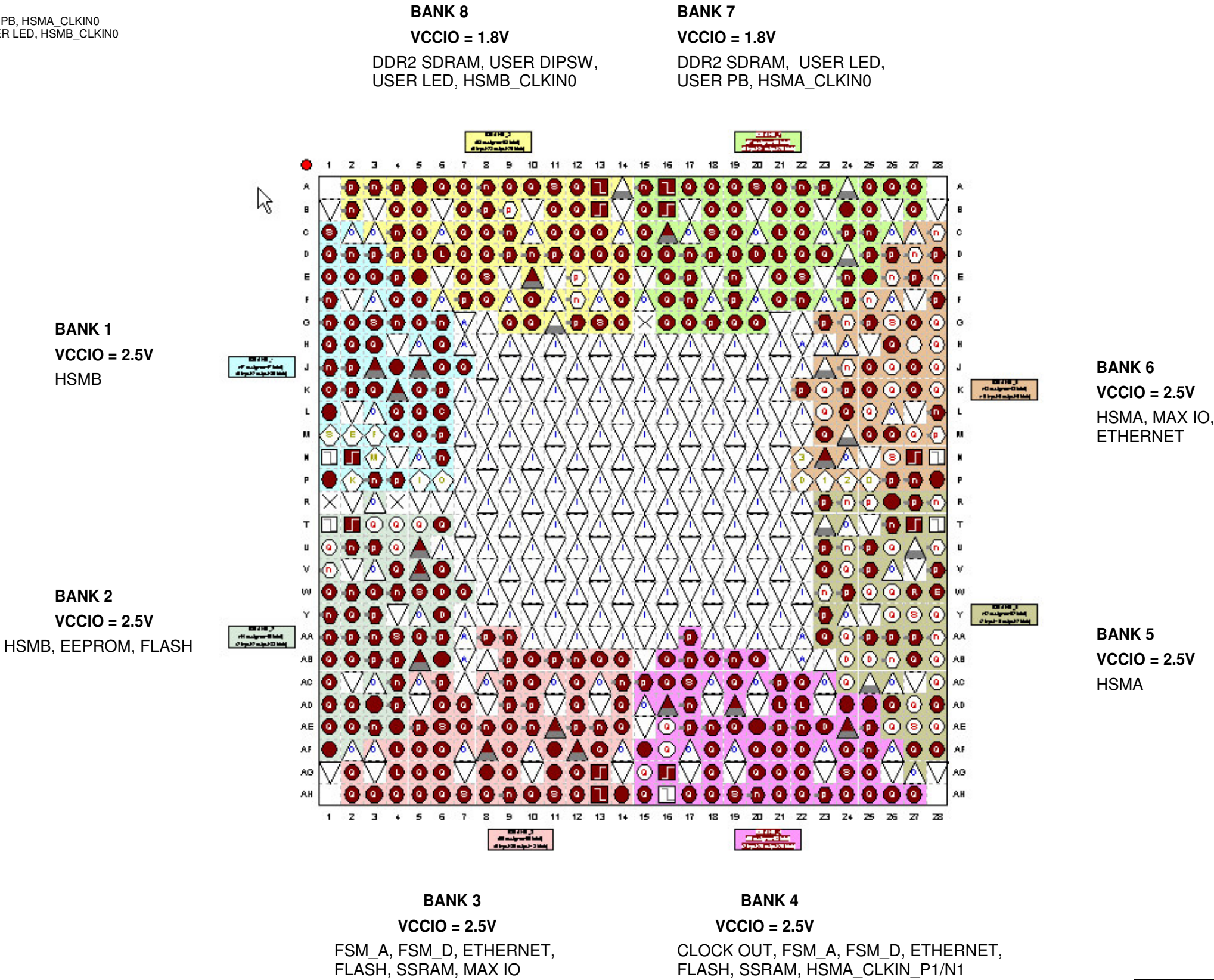
B	150-0320911-B1
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Date: Thursday, September 10, 2009 Sheet 1 of 25

Notes:

1. FPGA Schematic Symbol Breakdown:
- (A) Bank 1 - HSMB
 - (B) Bank 2 - HSMB, EEPROM, FLASH
 - (C) Bank 3 - FSM_A, FSM_D, ETHERNET, FLASH, SSRAM, MAX IO
 - (D) Bank 4 - CLOCK OUT, FSM_A, FSM_D, ETHERNET, FLASH, SSRAM, HSMA_CLKIN_P1/N1
 - (E) Bank 5 - HSMA
 - (F) Bank 6 - HSMA, MAX IO, ETHERNET
 - (G) Bank 7 - DDR2 SDRAM, USER LED, USER PB, HSMA_CLKIN0
 - (H) Bank 8 - DDR2 SDRAM, USER DIPSW, USER LED, HSMB_CLKIN0
 - (I) VCCINT
 - (J) VCCIO, VREF, VCCA, VCCD_PLL
 - (K) Ground, NC
 - (L) Clocks
 - (M) Configuration

Cyclone III LS FPGA Package Top

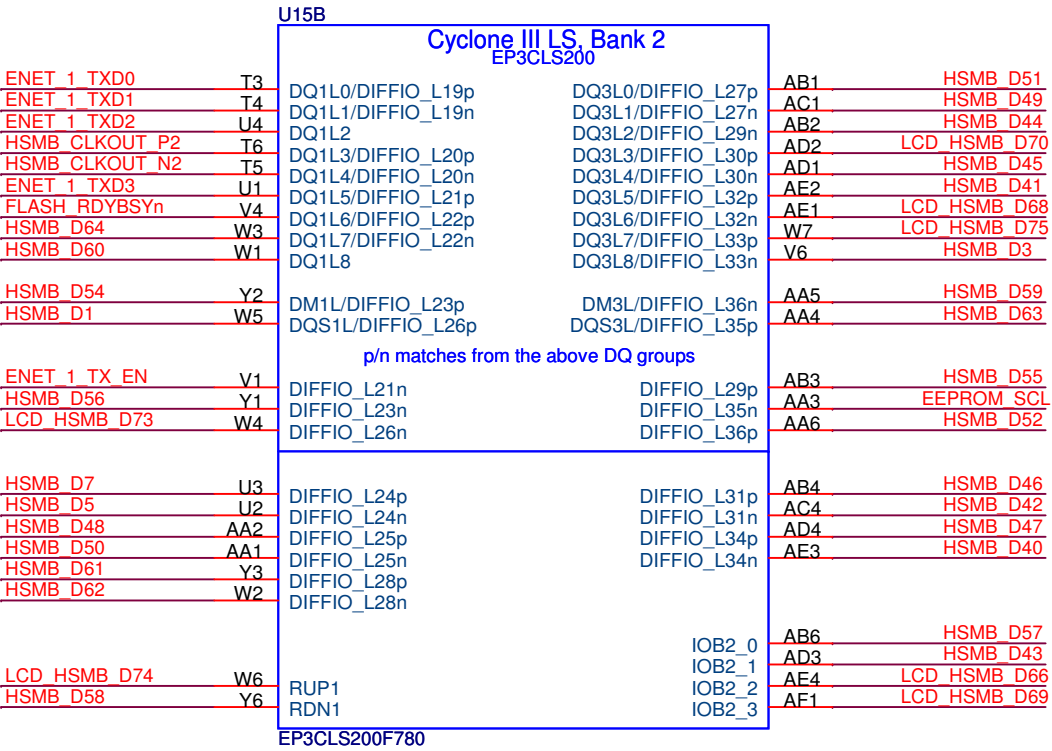
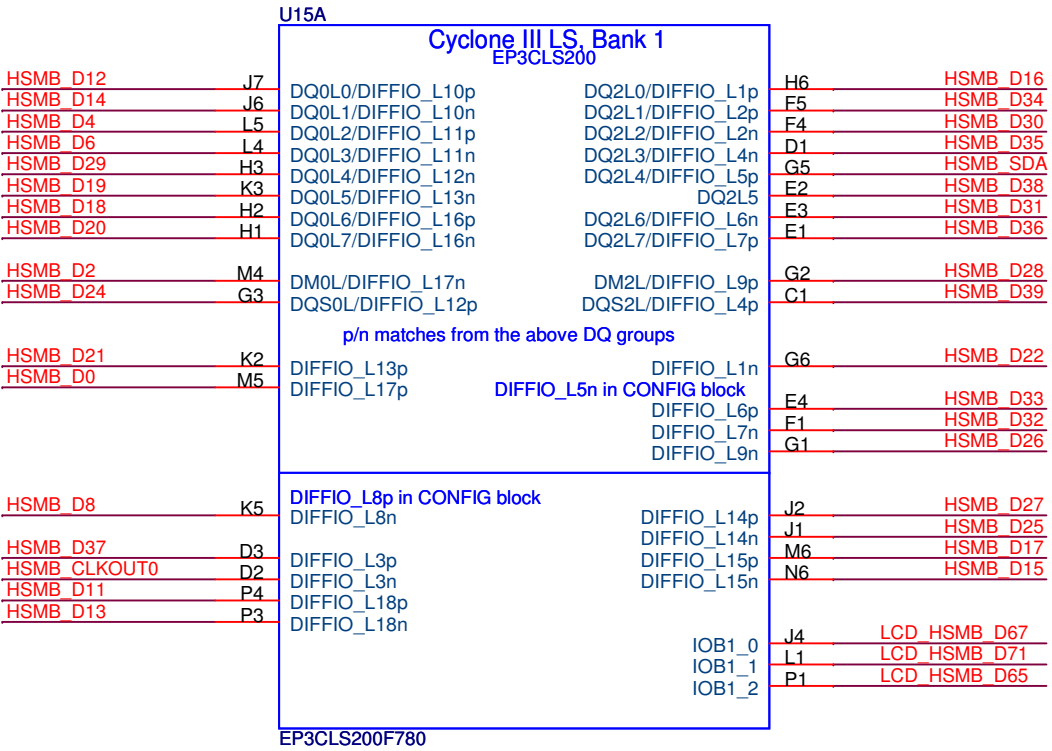


Pin Legend

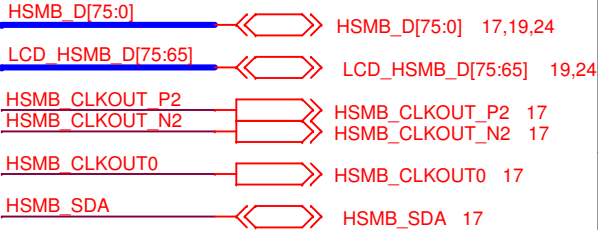
Sy...	Pin Type
	User I/O
	User Assigned I/O
	Filter Assigned I/O
	Unbonded Pad
	Reserved Pin
	Other Configuration
	DEV_OE
	DEV_CLR
	DIFF_n
	DIFF_p
	DQ
	DQS
	Other PLL
	Other Dual Purpose
	CLK_n
	CLK_p
	MSEL0
	MSEL1
	MSEL2
	MSEL3
	CONF_DONE
	nCE
	nCONFIG
	TDI
	TCK
	TMS
	TDO
	nSTATUS
	VREF
	VCCP/VCCR/VCC_T
	VCCA
	VCCINT
	VCCIO
	GND
	GND_A_PLL
	No Connect



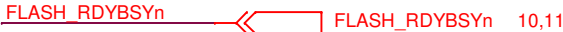
Cyclone III LS Bank 1 & 2



HSMB SIGNALS



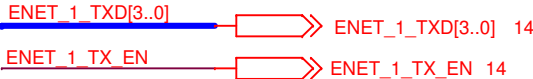
FLASH/LCD SIGNALS



EEPROM SIGNALS

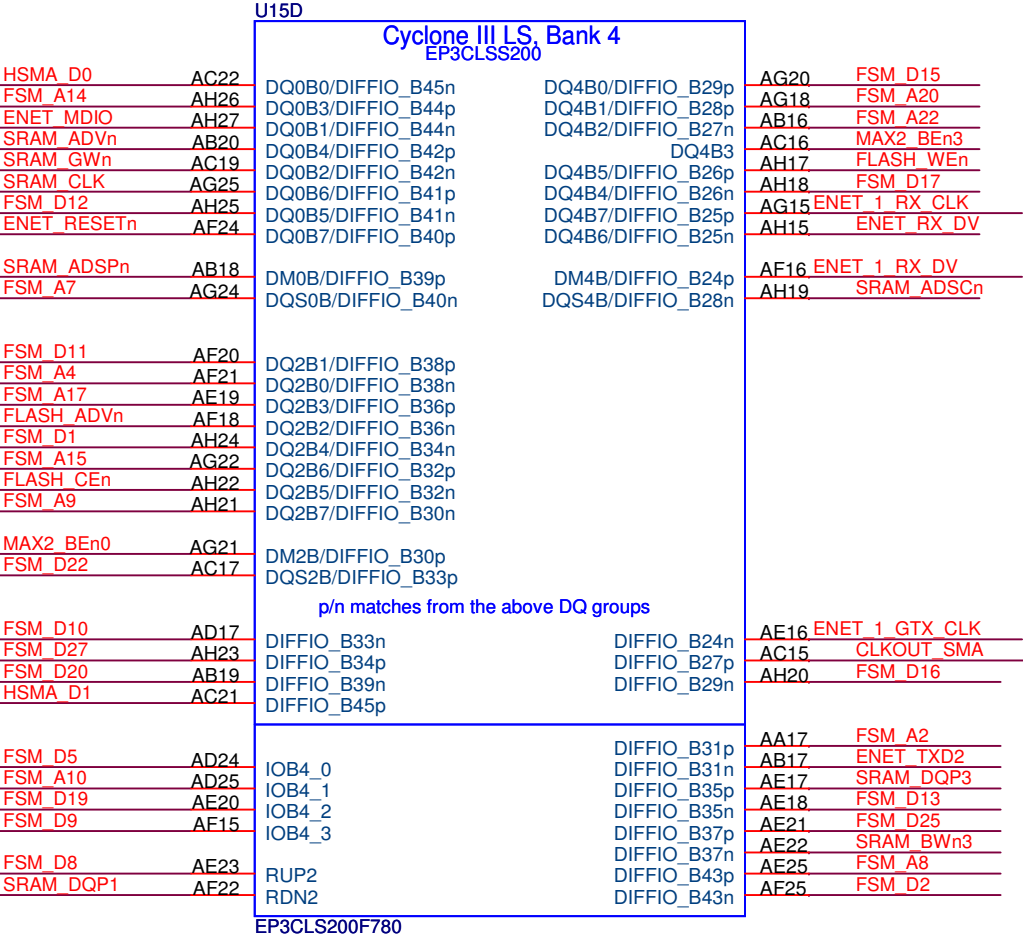
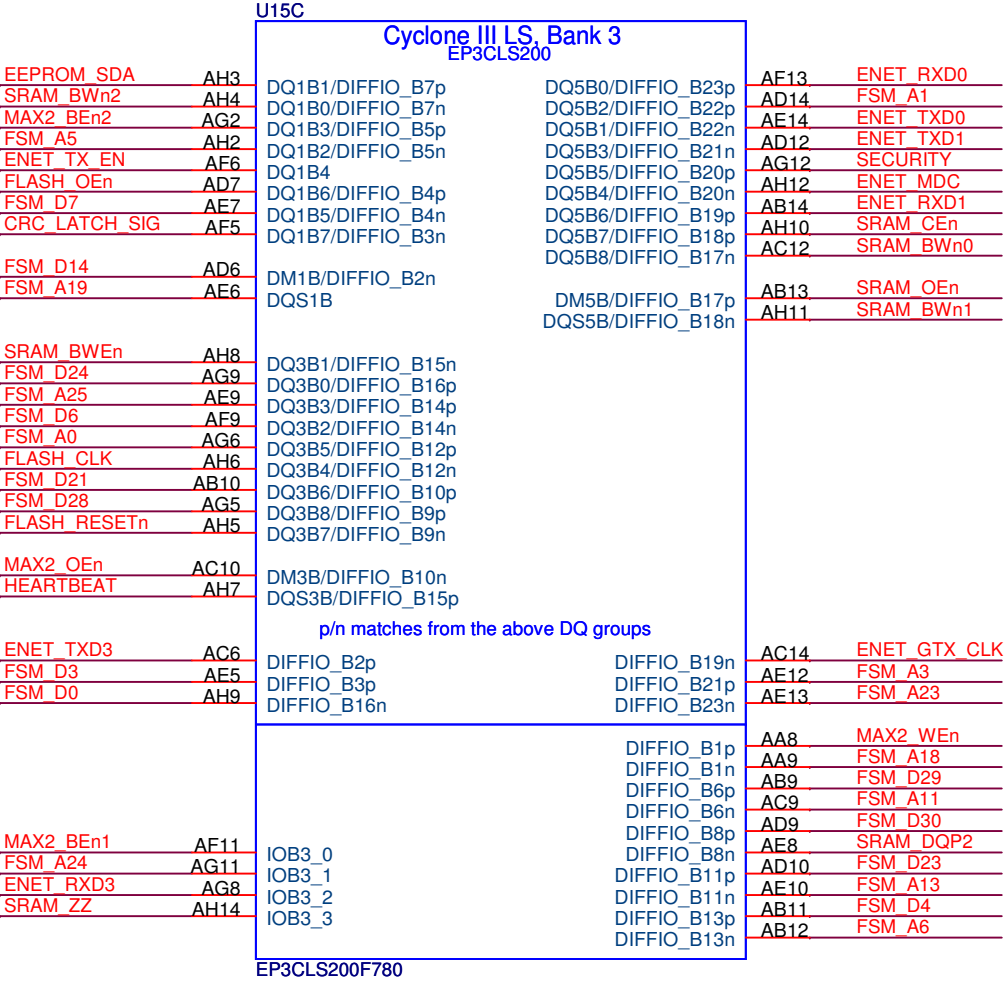


ETHERNET INTERFACE (Cyclone III)

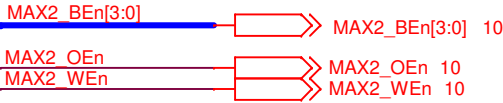


Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121			
Title		Cyclone III LS FPGA Development Board	
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Size B	Document Number 150-0320911-B1		Rev B-1
Date:	Thursday, September 10, 2009	Sheet 3 of 25	

Cyclone III LS Bank 3 & 4



MAXII CONTROL INTERFACE



EEPROM SIGNALS



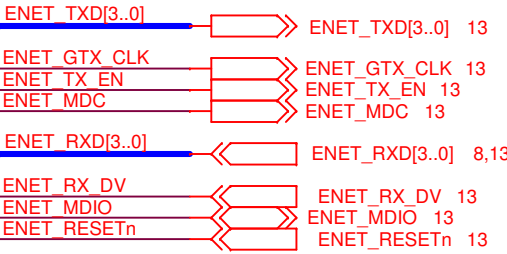
HSMC PORT A



ANTI-TAMPER INTERFACE



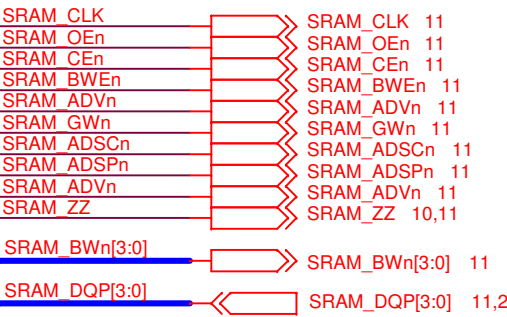
ETHERNET INTERFACE



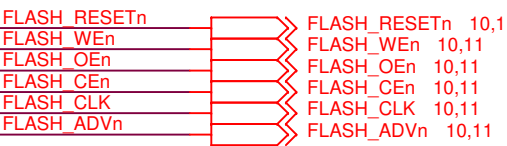
SHARED BUS



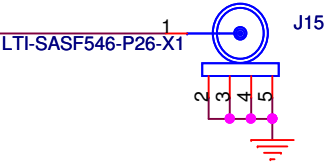
SSRAM INTERFACE



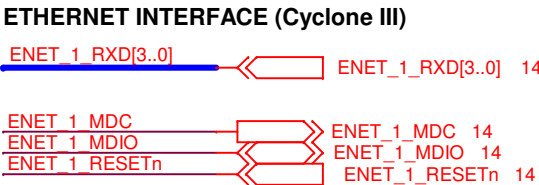
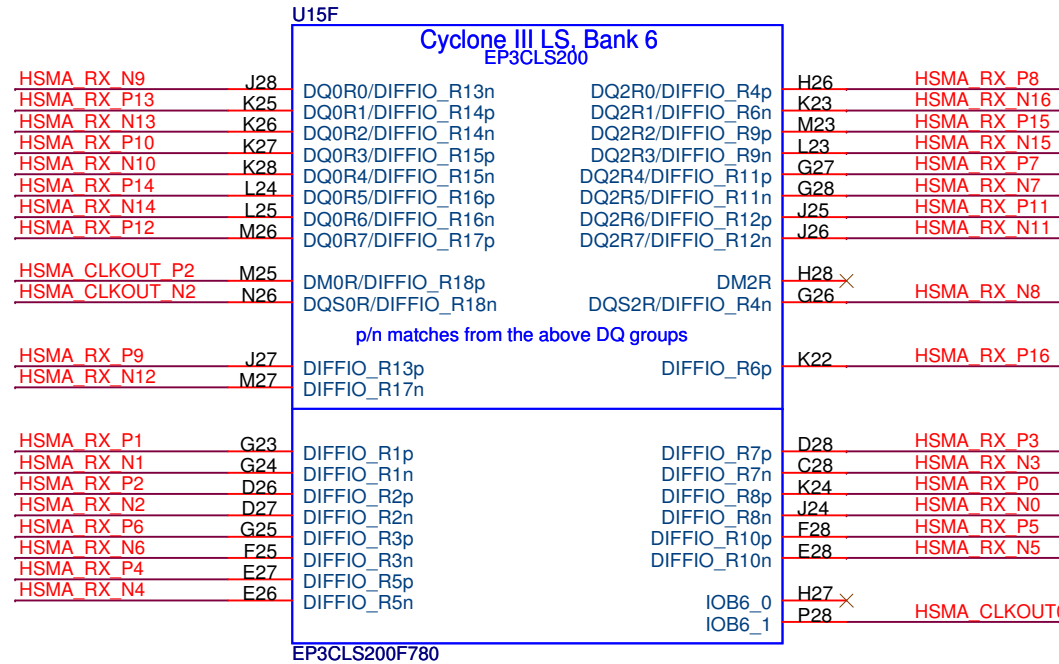
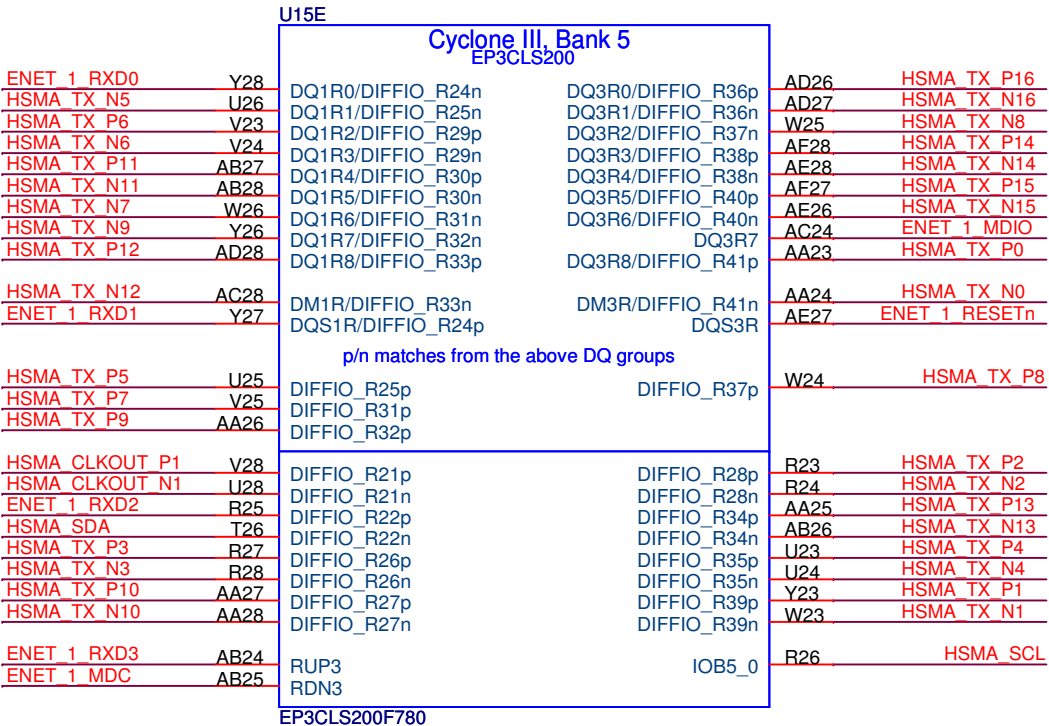
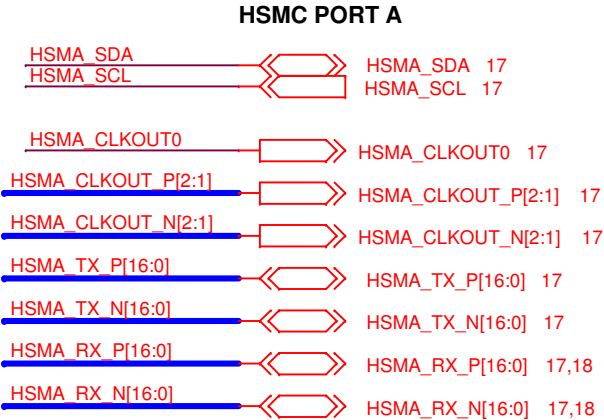
FLASH INTERFACE



ETHERNET INTERFACE (Cyclone III)



Cyclone III LS Bank 5 & 6



Cyclone III LS Bank 7 & 8

LCD_HSMB_SEL LCD_HSMB_SEL 19

DDR2 SDRAM SIGNALS

DDR2_DQ[31:0] DDR2_DQ[31:0] 7,15,16
DDR2_DQS[3:0] DDR2_DQS[3:0] 15,16
DDR2_DM[3:0] DDR2_DM[3:0] 7,15,16

DDR2 SDRAM BANK 7 SIGNALS

DDR2_B7_A[15:0] DDR2_B7_A[15:0] 15,16,24
DDR2_B7_BA[2:0] DDR2_B7_BA[2:0] 15,16
DDR2_B7_RASn DDR2_B7_RASn 15,16
DDR2_B7_CASn DDR2_B7_CASn 15,16
DDR2_B7_WEn DDR2_B7_WEn 15,16
DDR2_B7_CSn DDR2_B7_CSn 15,16
DDR2_B7_ODT DDR2_B7_ODT 15,16
DDR2_B7_CKE DDR2_B7_CKE 15,16

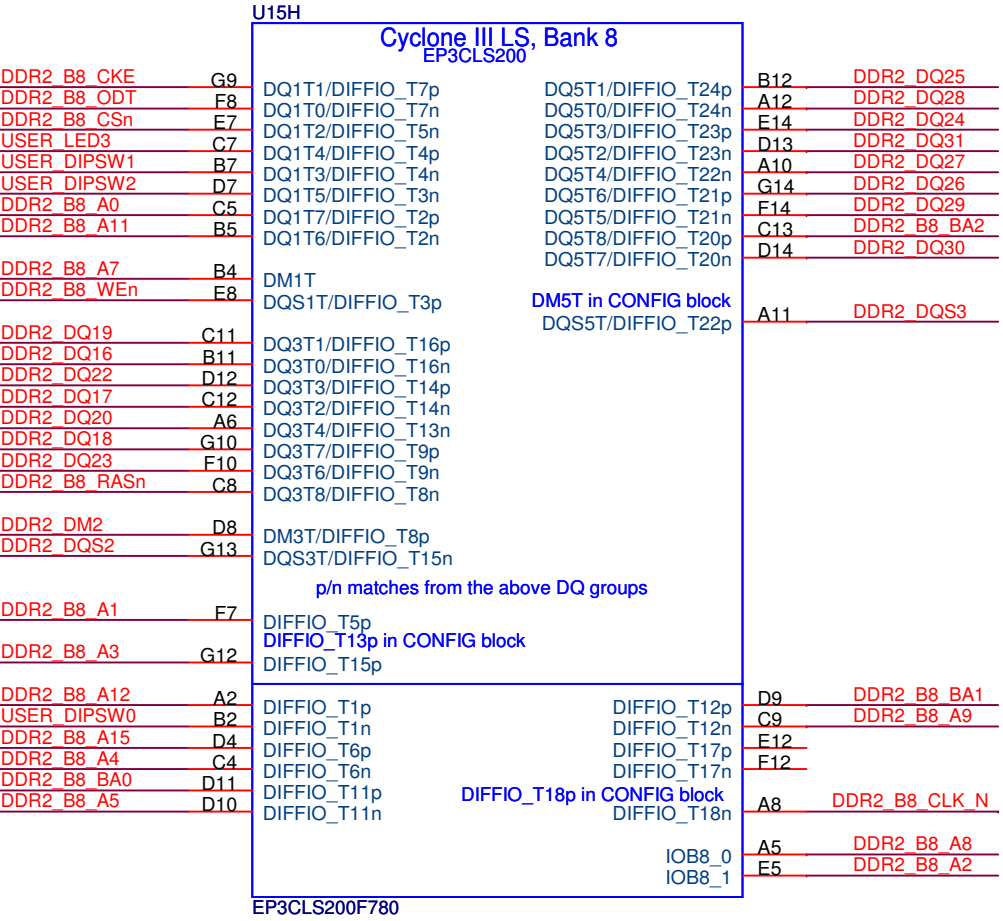
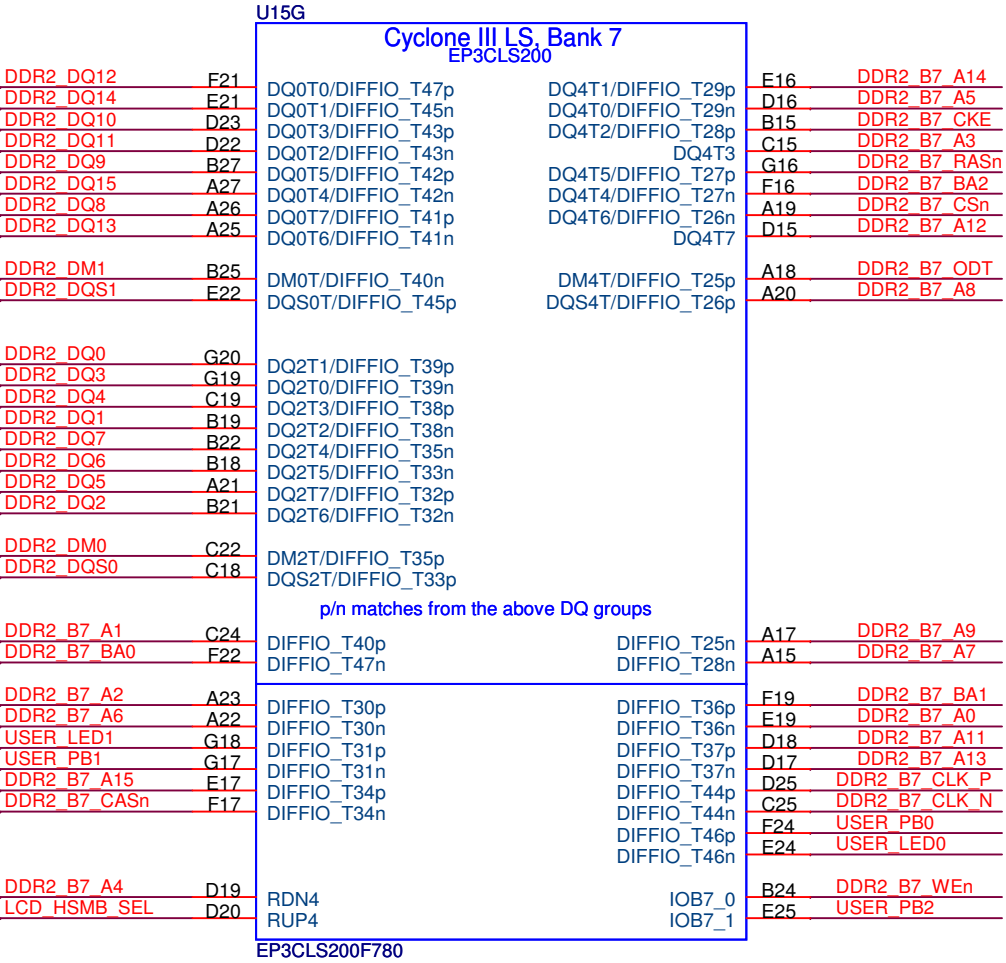
DDR2_B7_CLK_P DDR2_B7_CLK_P 15
DDR2_B7_CLK_N DDR2_B7_CLK_N 15

DDR2 SDRAM BANK 8 SIGNALS

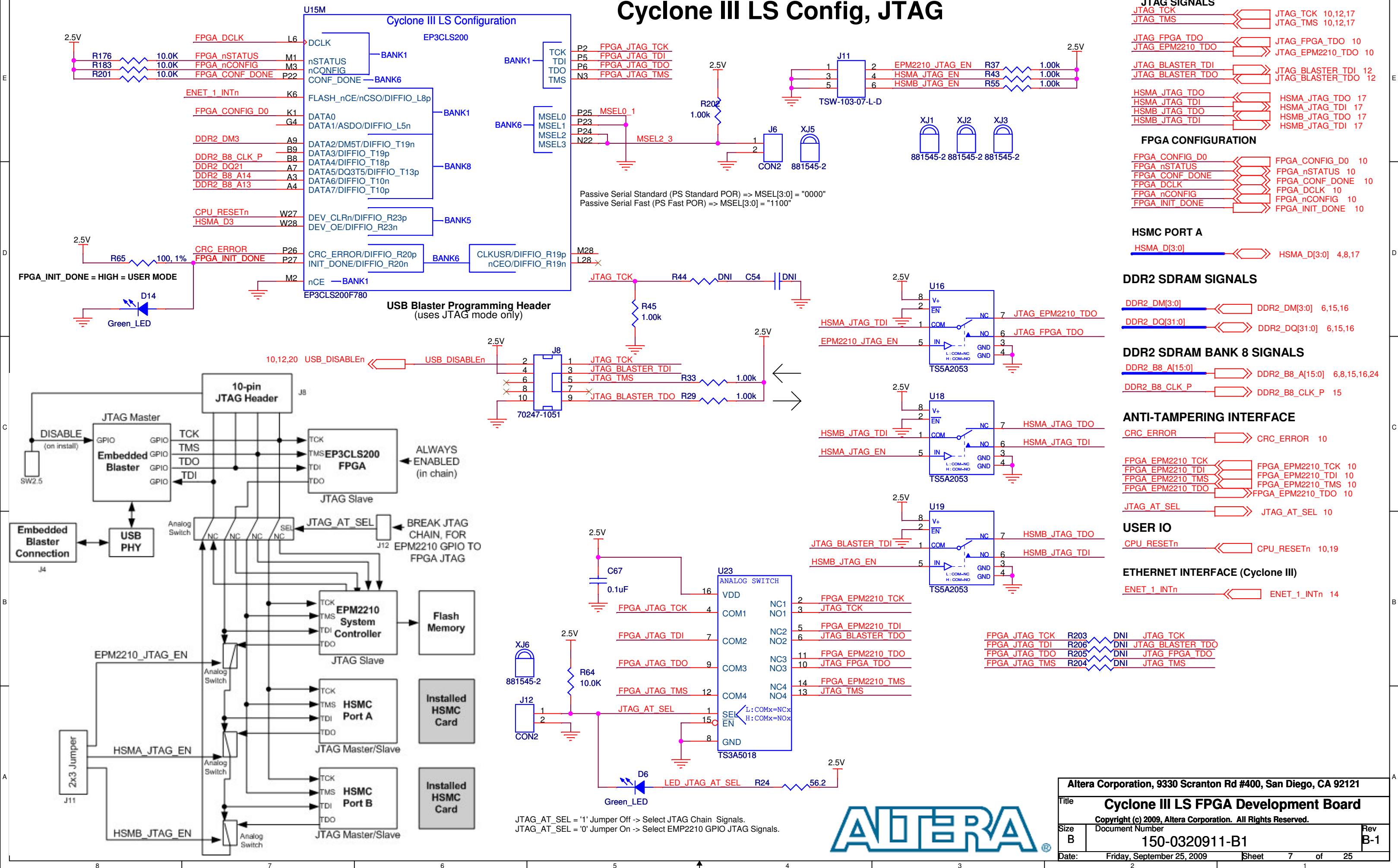
DDR2_B8_A[15:0] DDR2_B8_A[15:0] 7,8,15,16,24
DDR2_B8_BA[2:0] DDR2_B8_BA[2:0] 15,16
DDR2_B8_RASn DDR2_B8_RASn 15,16
DDR2_B8_CSn DDR2_B8_CSn 15,16
DDR2_B8_ODT DDR2_B8_ODT 15,16
DDR2_B8_CKE DDR2_B8_CKE 15,16
DDR2_B8_WEn DDR2_B8_WEn 15,16
DDR2_B8_CLK_N DDR2_B8_CLK_N 15

USER I/O

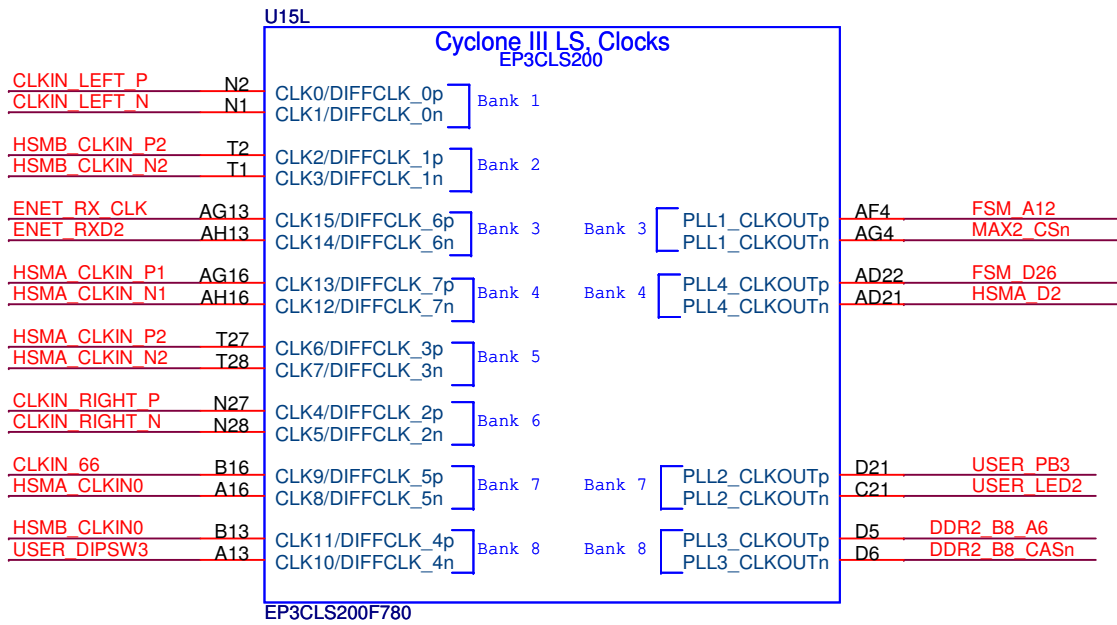
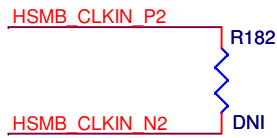
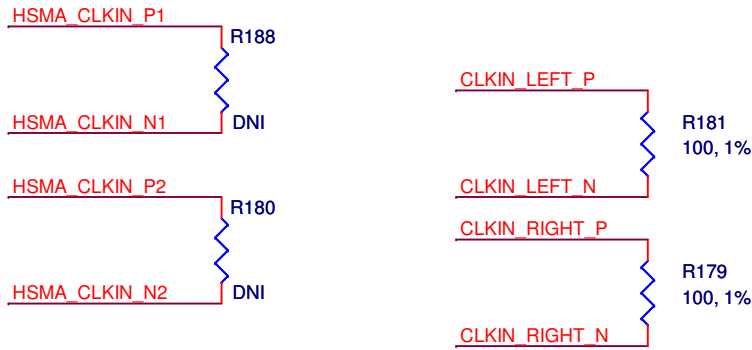
USER_LED[3:0] USER_LED[3:0] 8,19
USER_PB[3:0] USER_PB[3:0] 8,19
USER_DIPSW[3:0] USER_DIPSW[3:0] 8,19



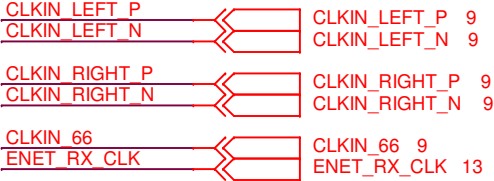
Cyclone III LS Config, JTAG



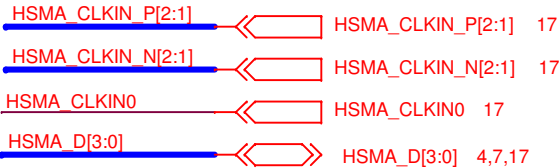
Cyclone III LS Clocks



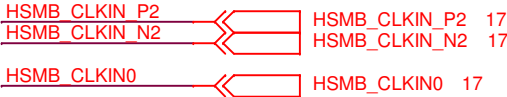
CLOCK SIGNALS



HSMC PORT A



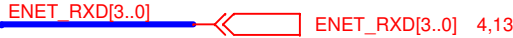
HSMC PORT B



DDR2 SDRAM BANK 8 SIGNALS



ETHERNET INTERFACE



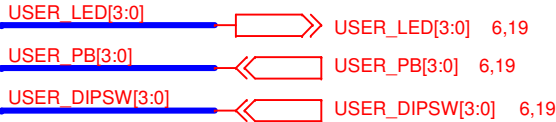
SHARED BUS



MAXII CONTROL INTERFACE

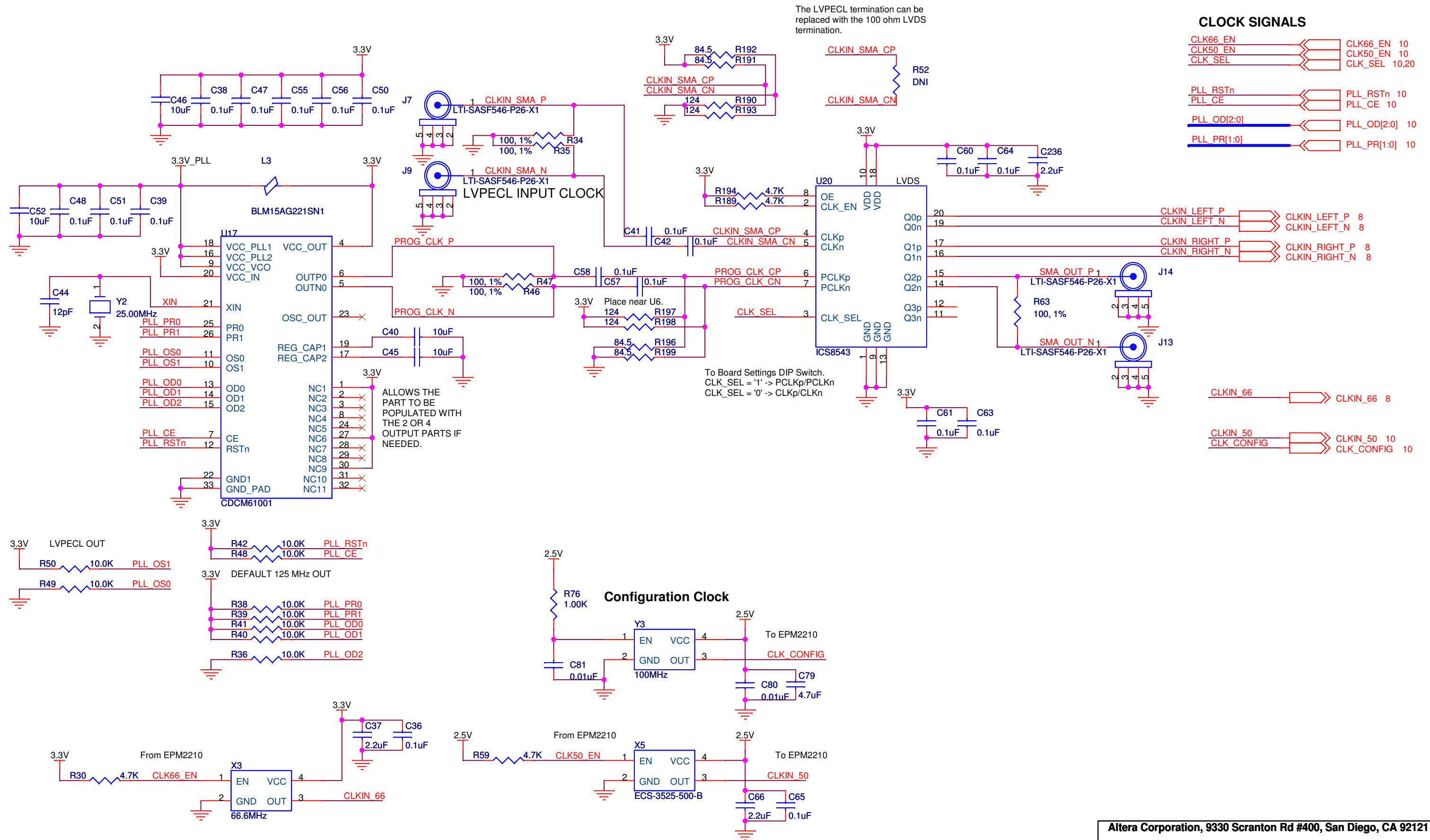


USER I/O

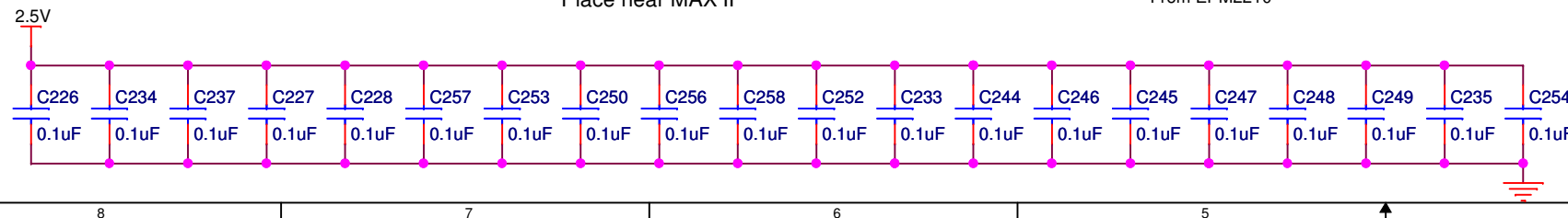
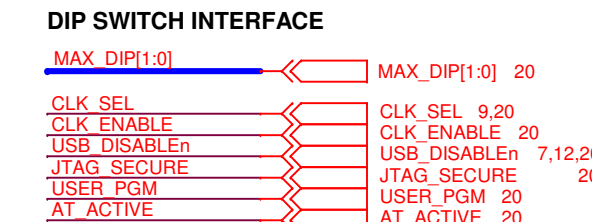
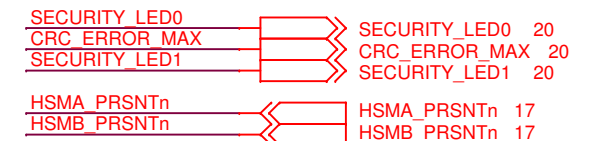
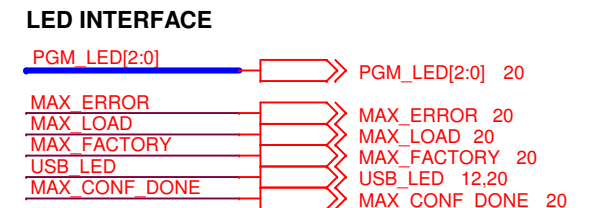
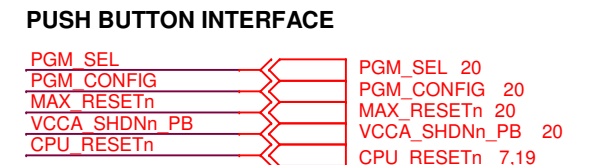
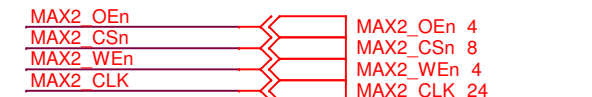
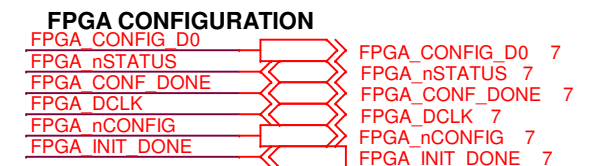
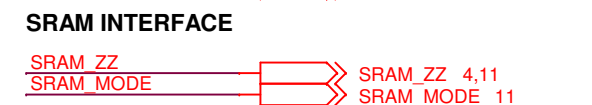
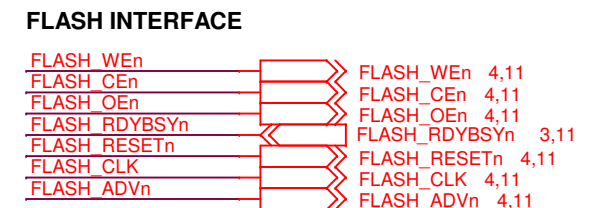
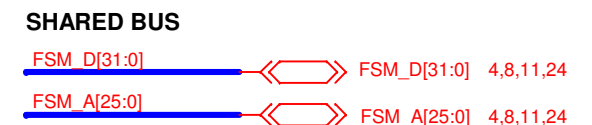
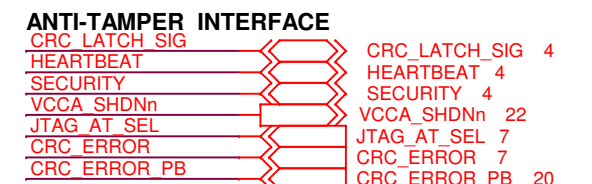
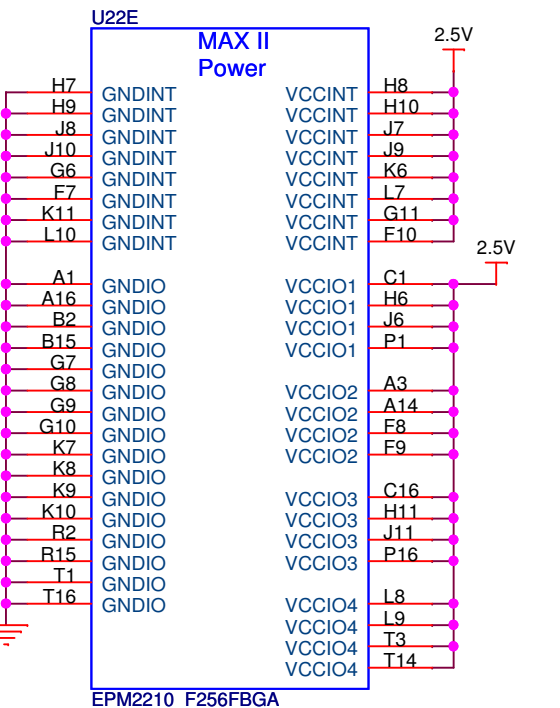
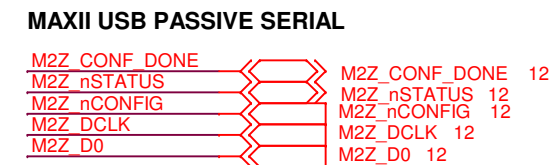
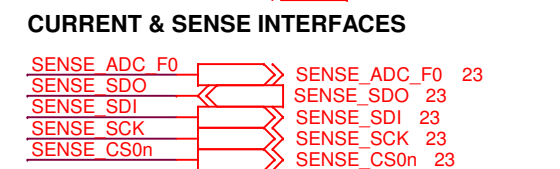
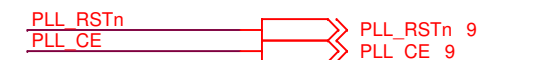
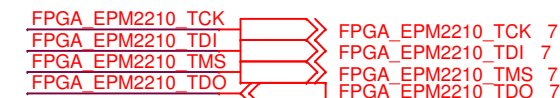
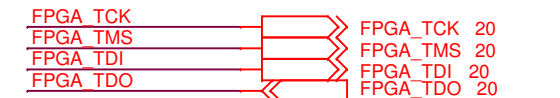
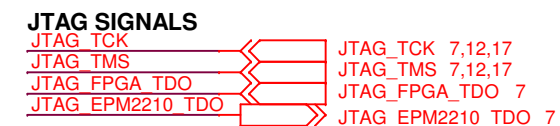
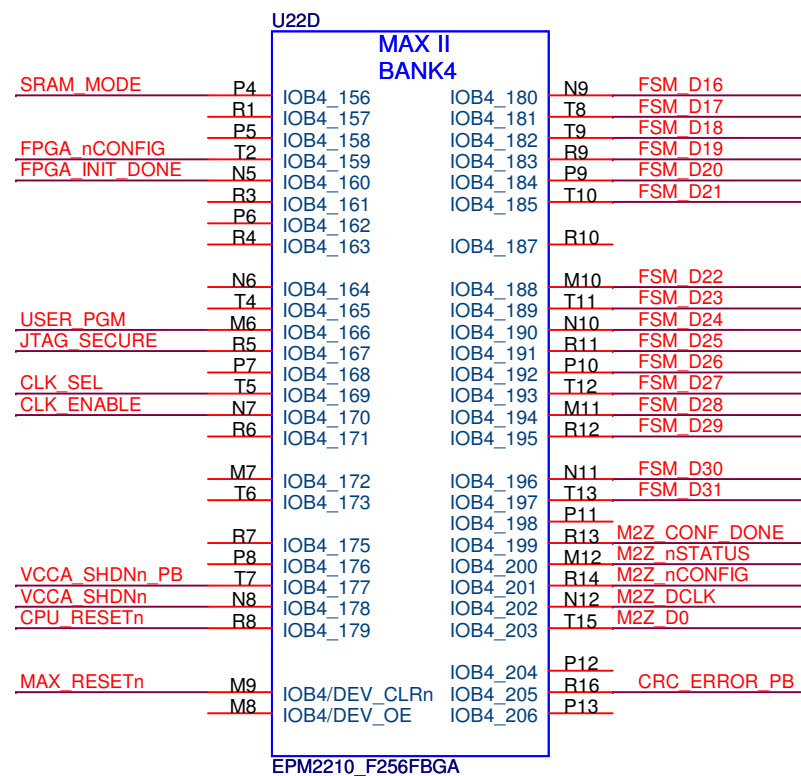
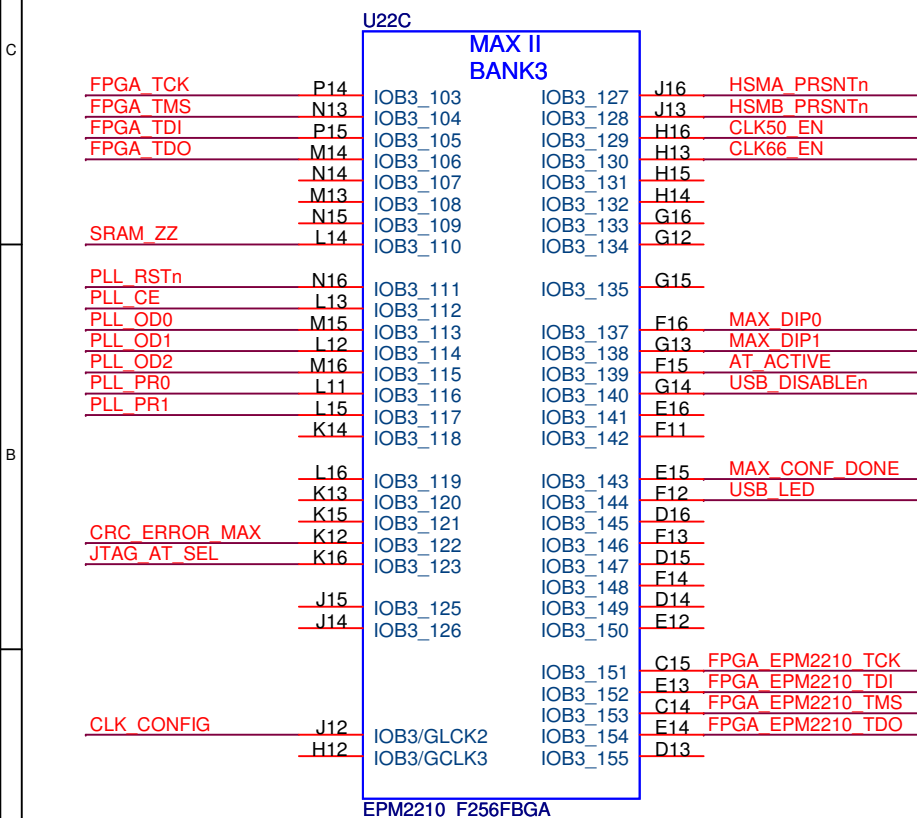
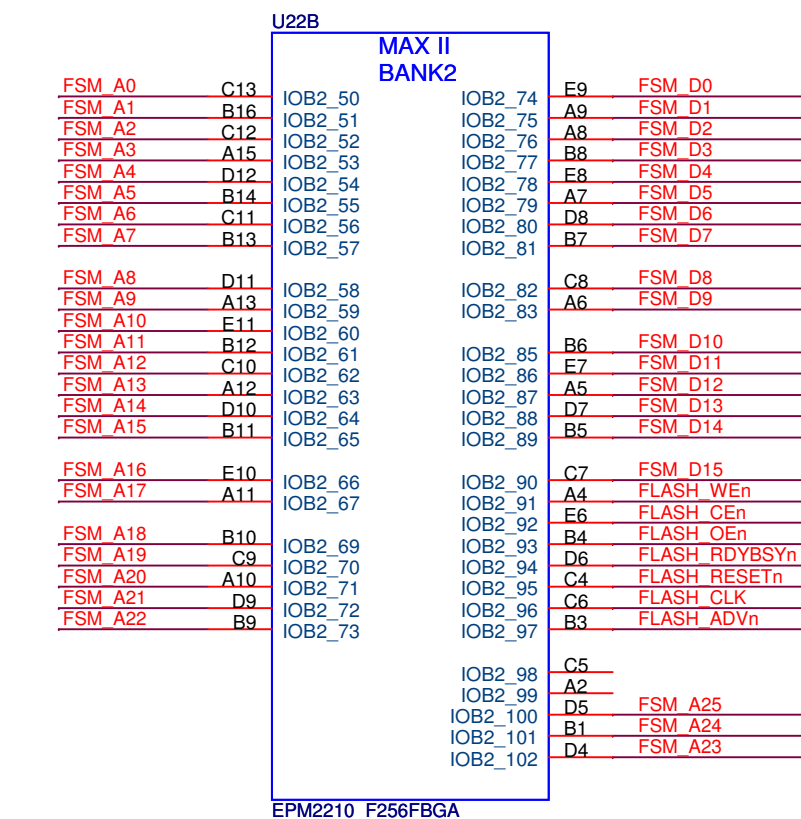
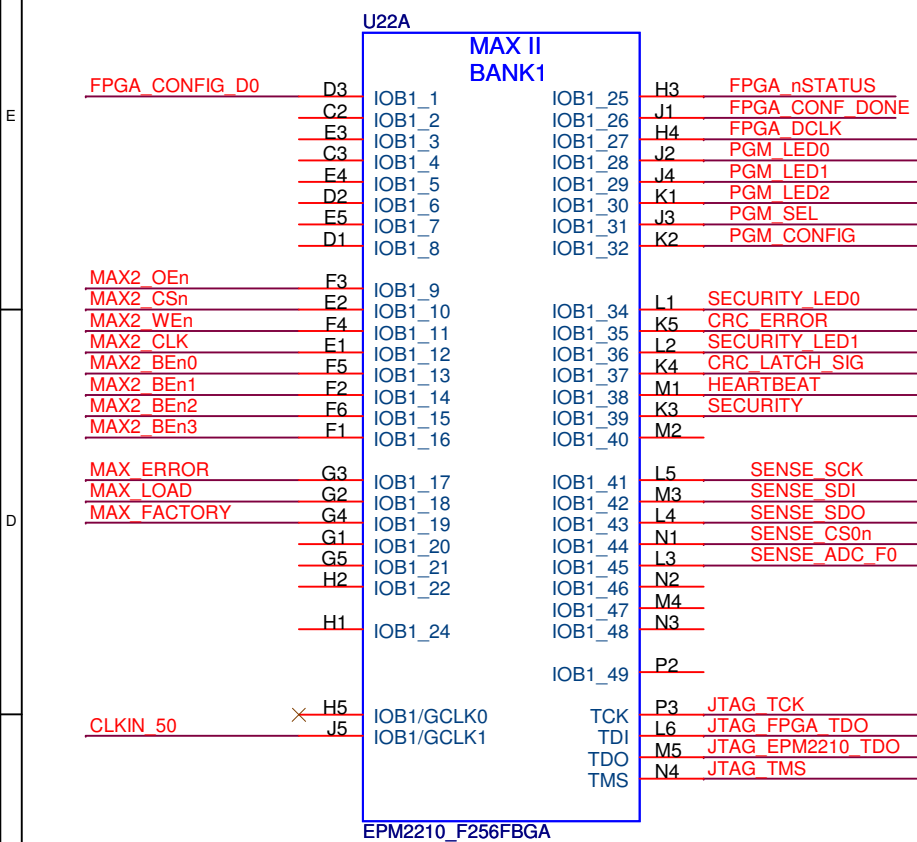


Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121			
Title		Cyclone III LS FPGA Development Board	
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Size B	Document Number 150-0320911-B1		Rev B-1
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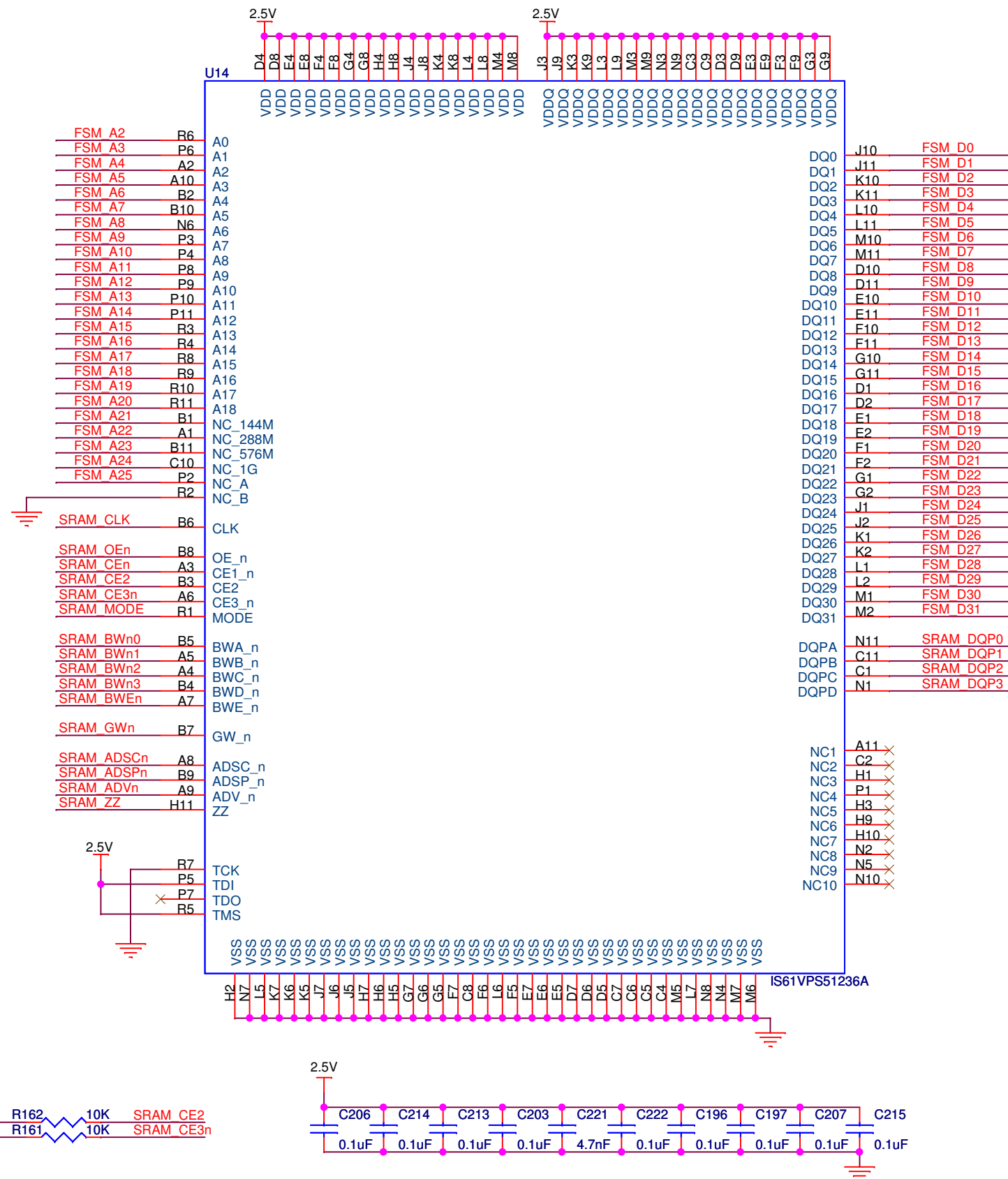
Clock Circuitry



EPM2210 System Controller



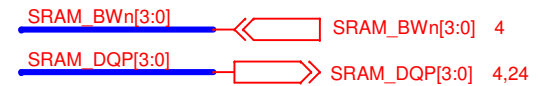
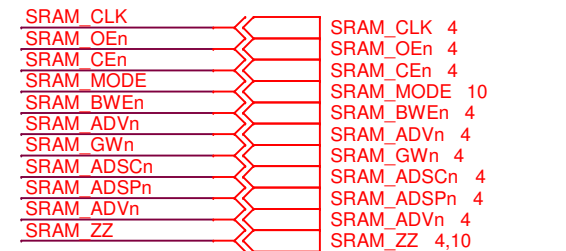
SRAM & Flash



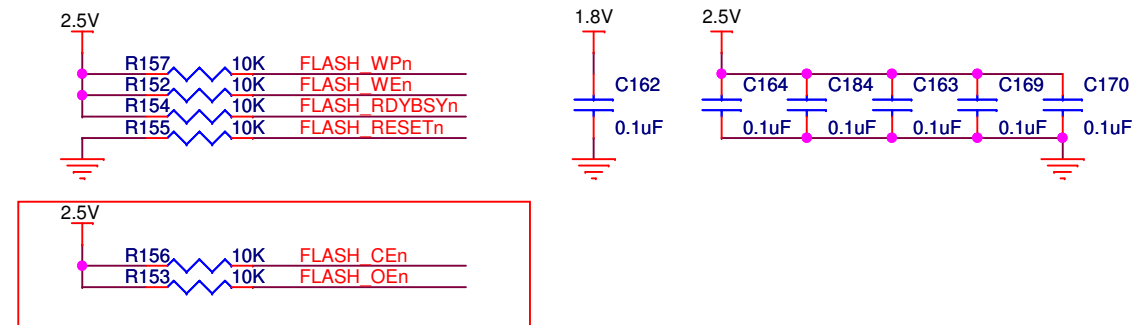
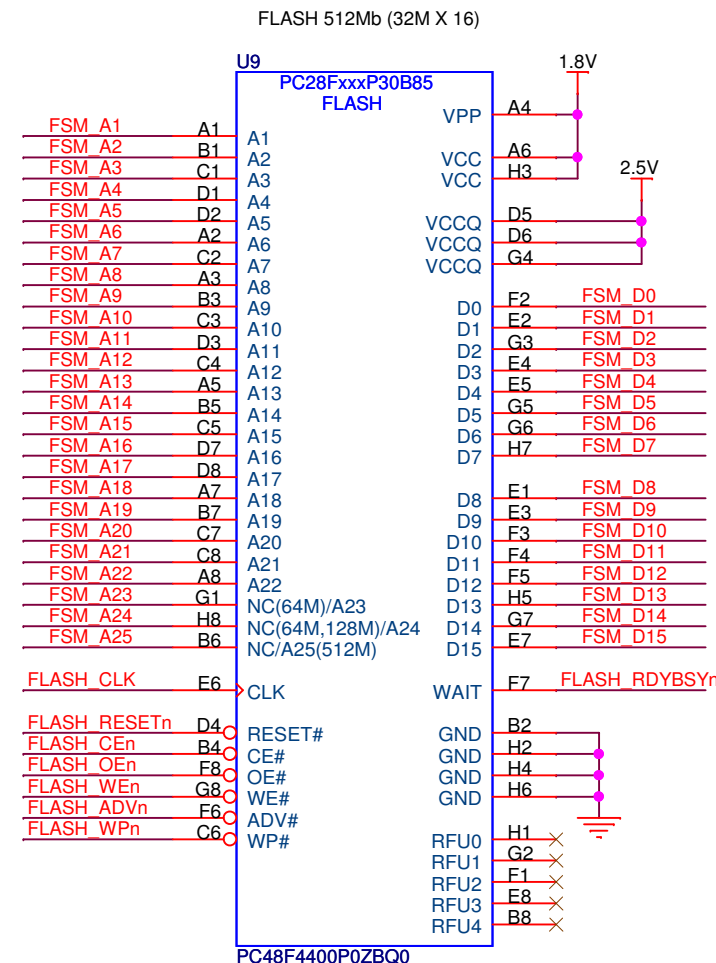
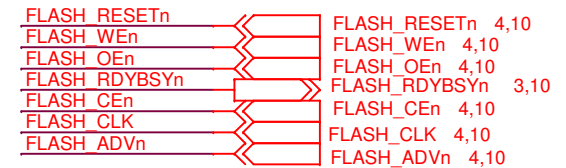
SHARED BUS



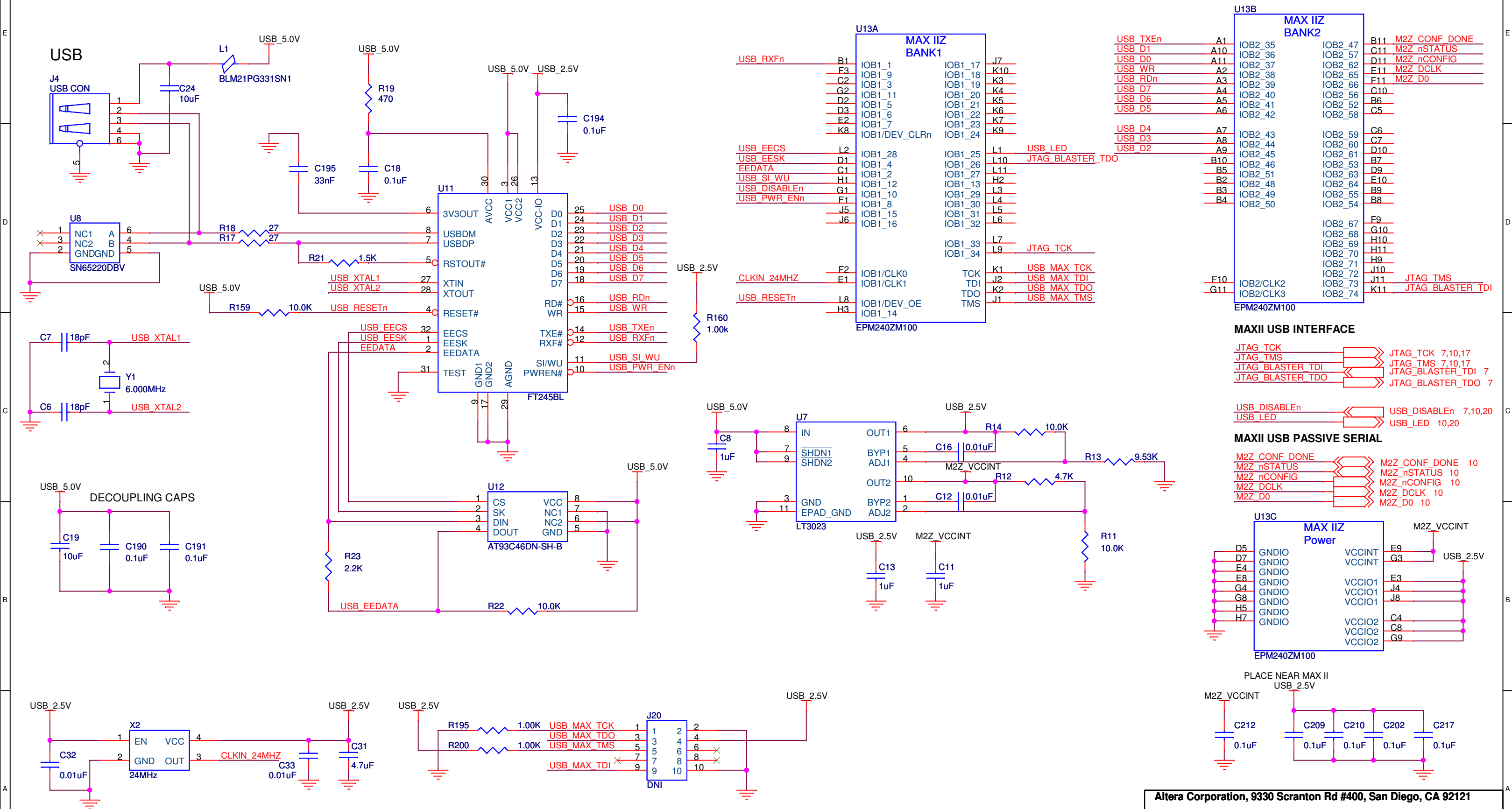
SSRAM INTERFACE



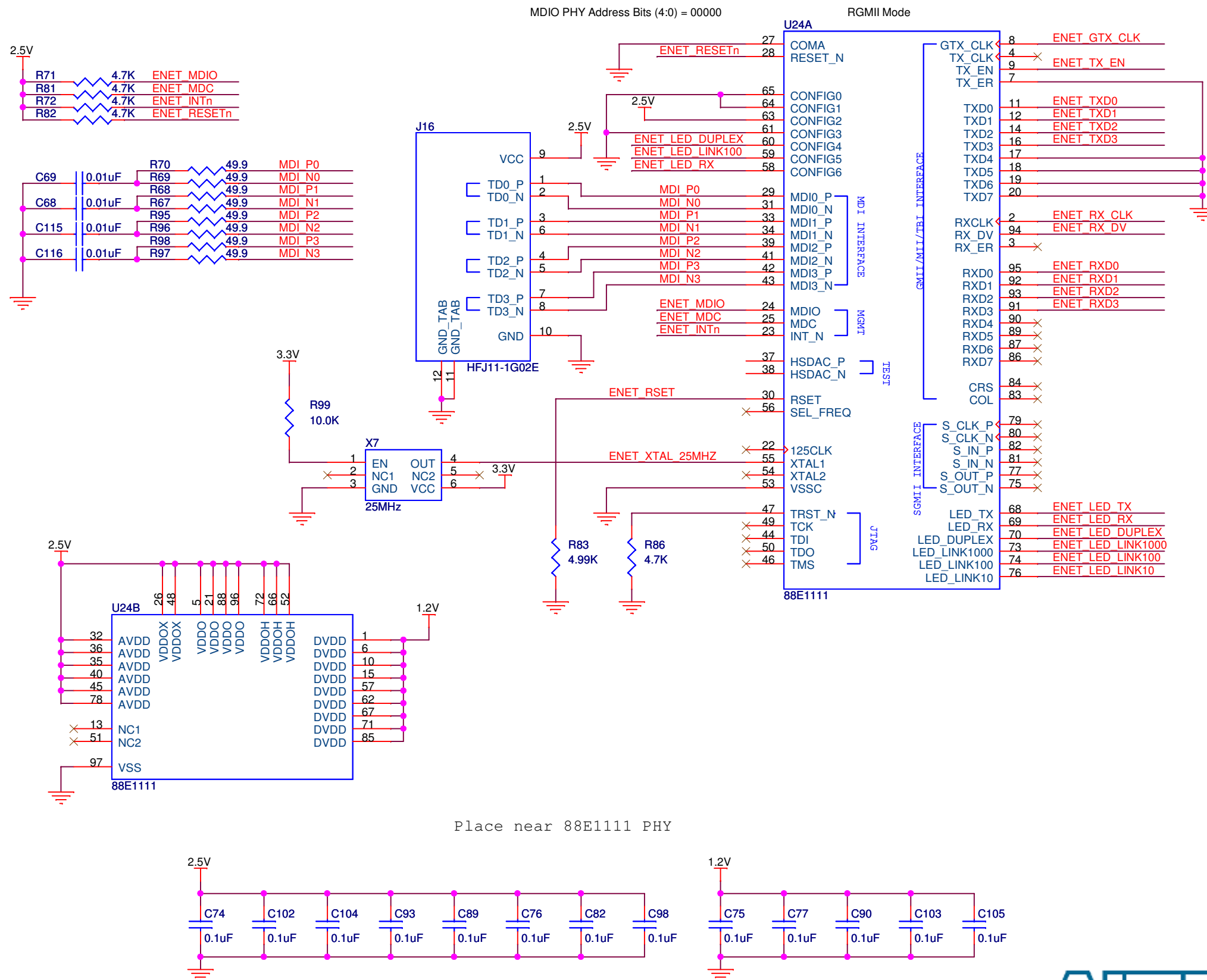
FLASH INTERFACE



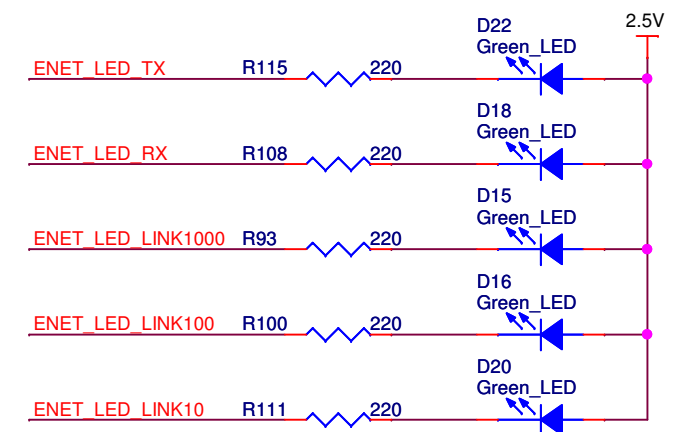
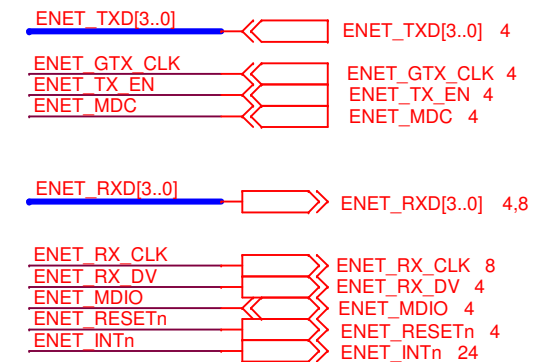
Embedded USB Blaster



10/100/1000 Ethernet (Port 0)

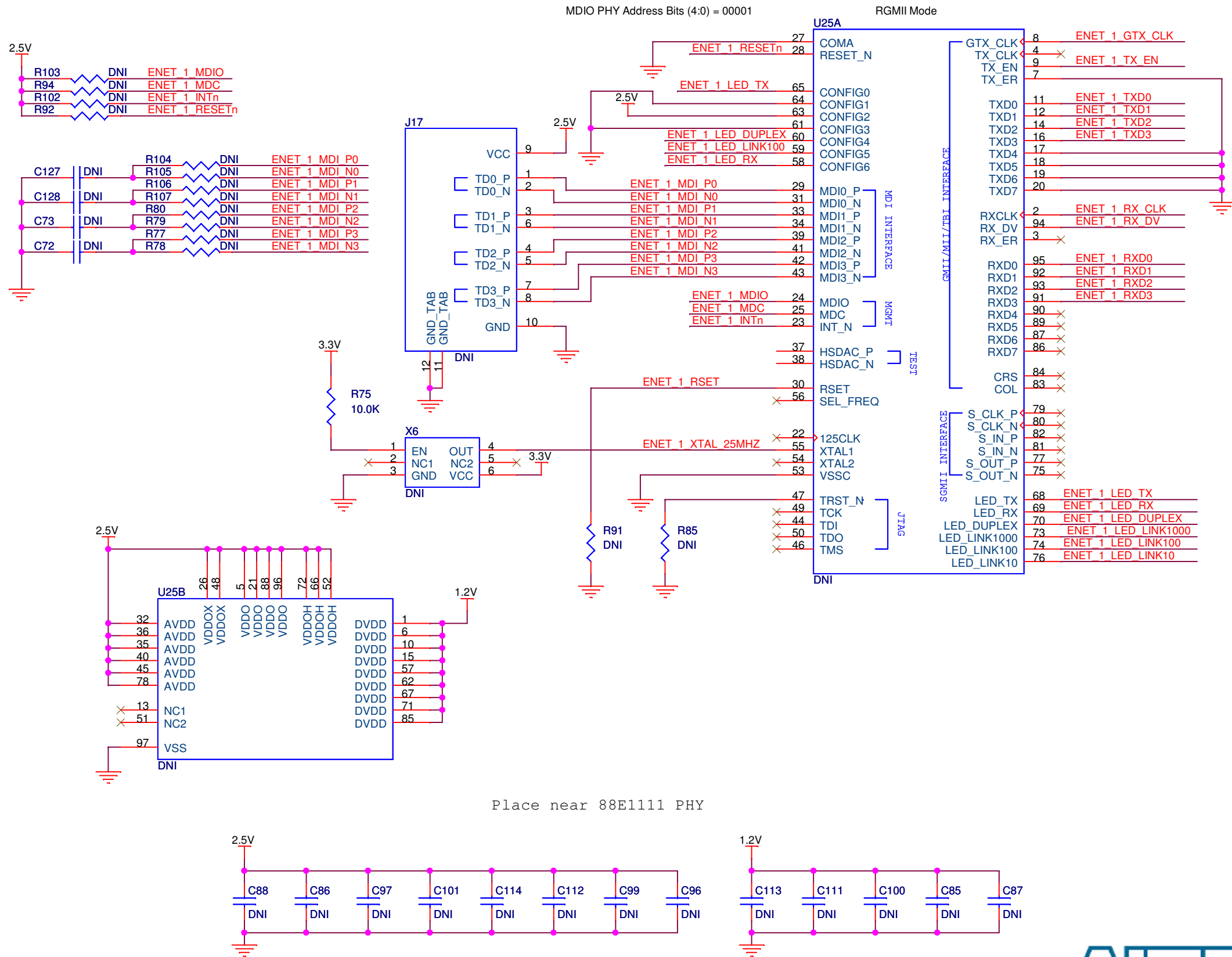


ETHERNET INTERFACE

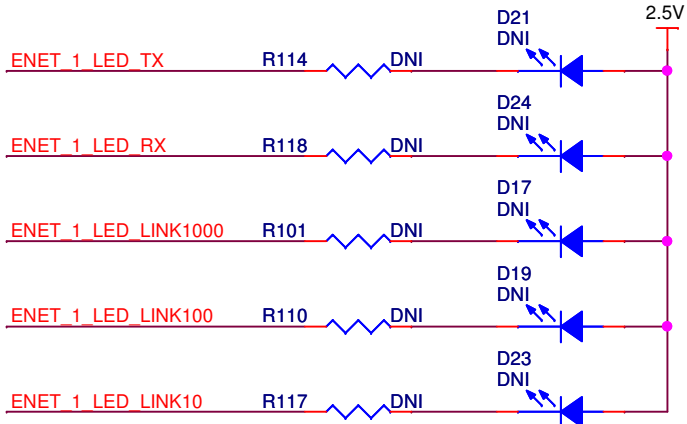
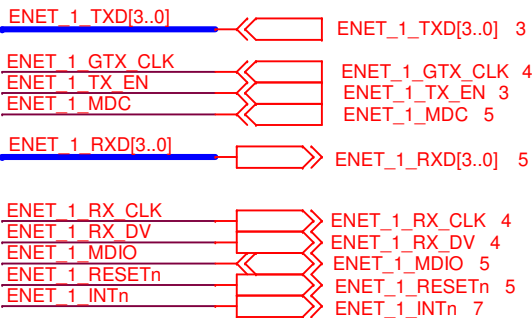


10/100/1000 Ethernet (Port 1)

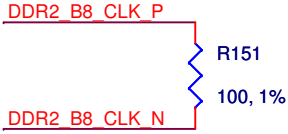
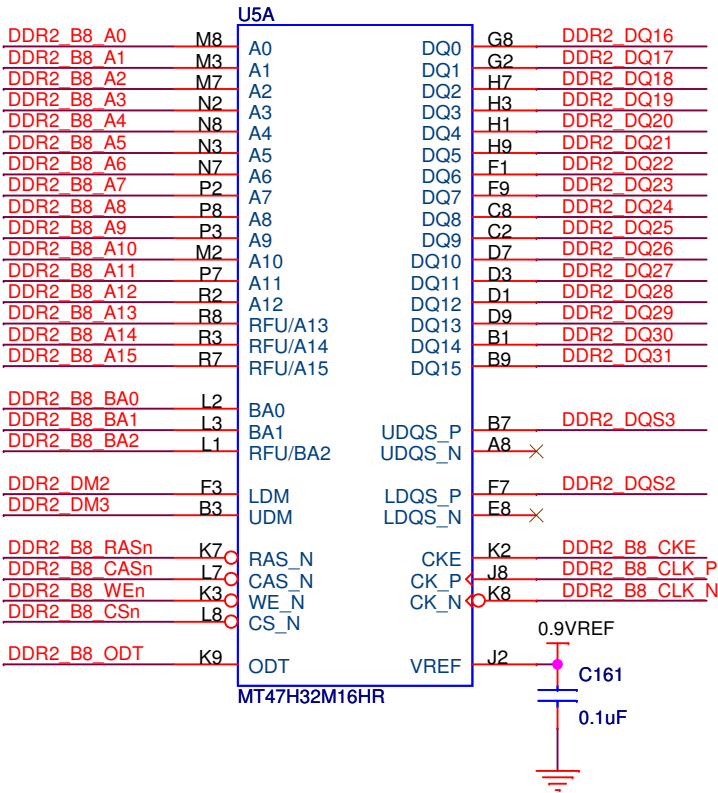
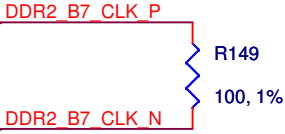
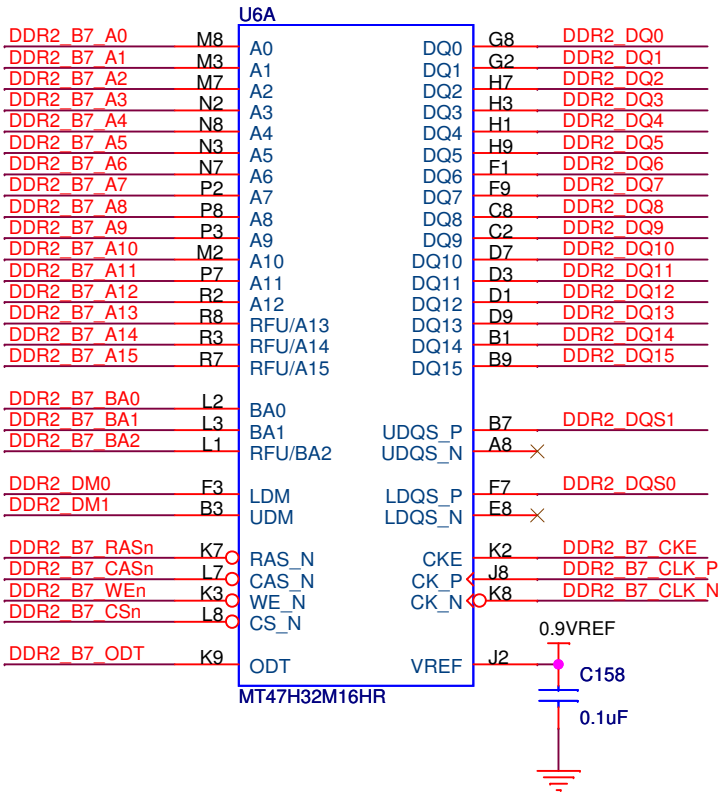
Only populated on C3 Industrial Board



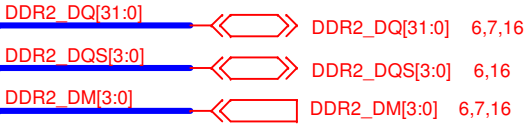
ETHERNET INTERFACE



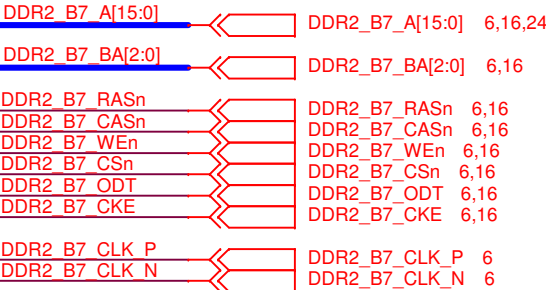
DDR2 SDRAM



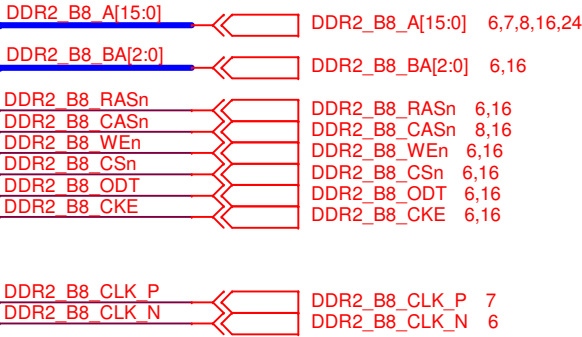
DDR2 SDRAM SIGNALS



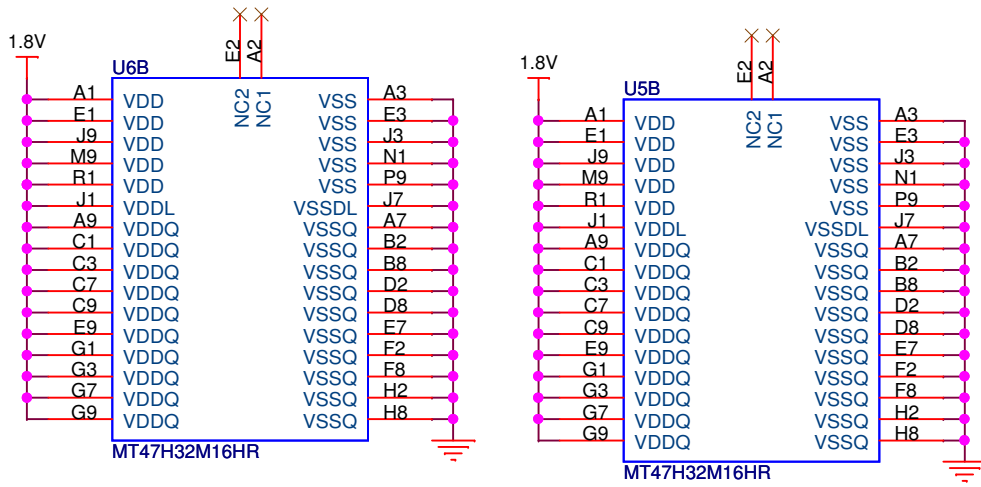
DDR2 SDRAM BANK 7 SIGNALS



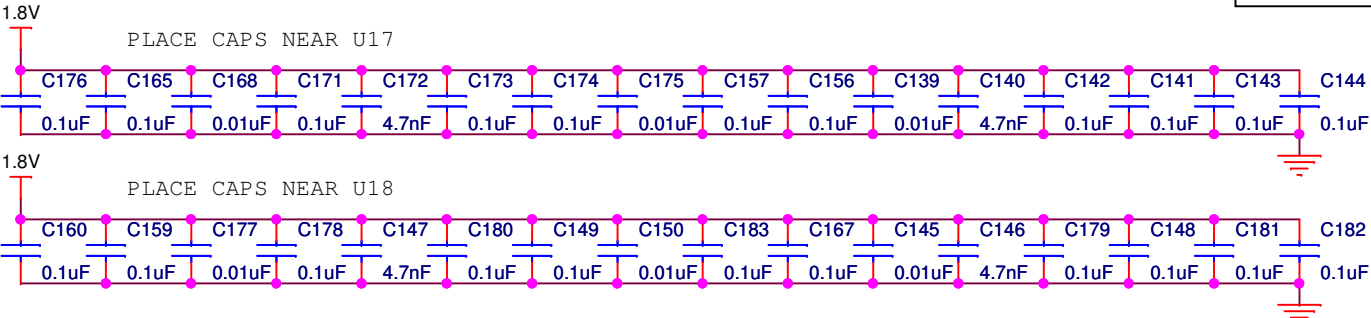
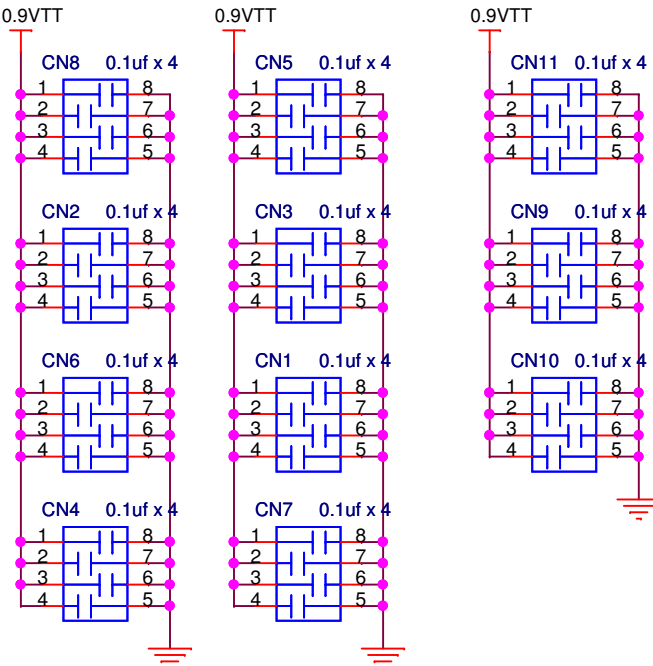
DDR2 SDRAM BANK 8 SIGNALS



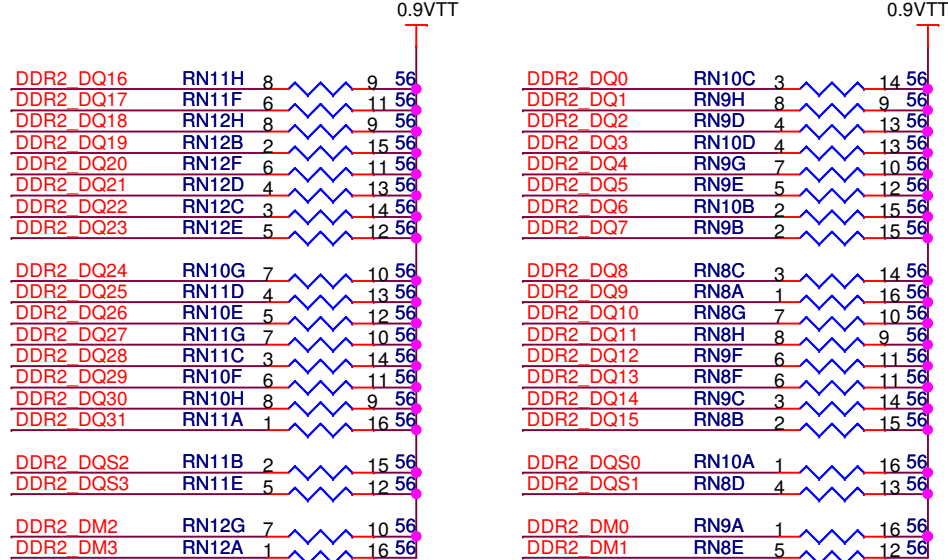
DDR2 SDRAM POWER & TERM



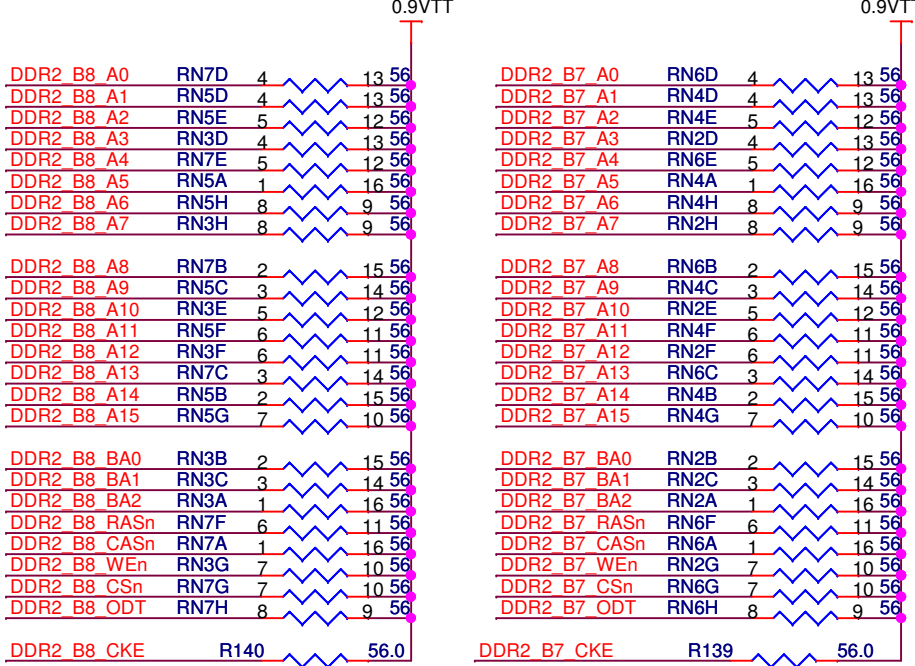
PLACE CAPS NEAR RESISTOR PACKS



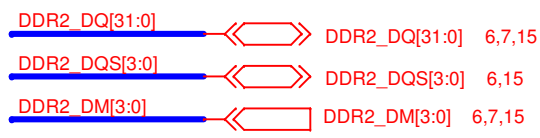
PLACE NEAR CYCLONE III LS



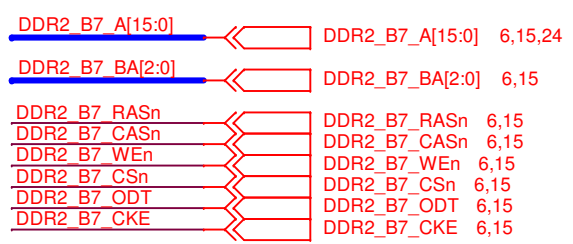
PLACE NEAR DDR2 DEVICES



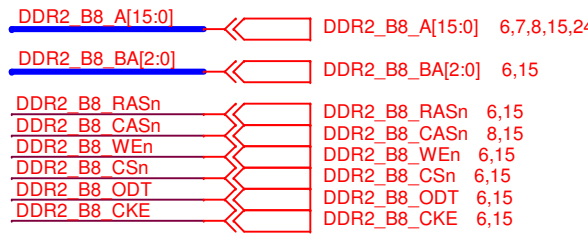
DDR2 SDRAM SIGNALS



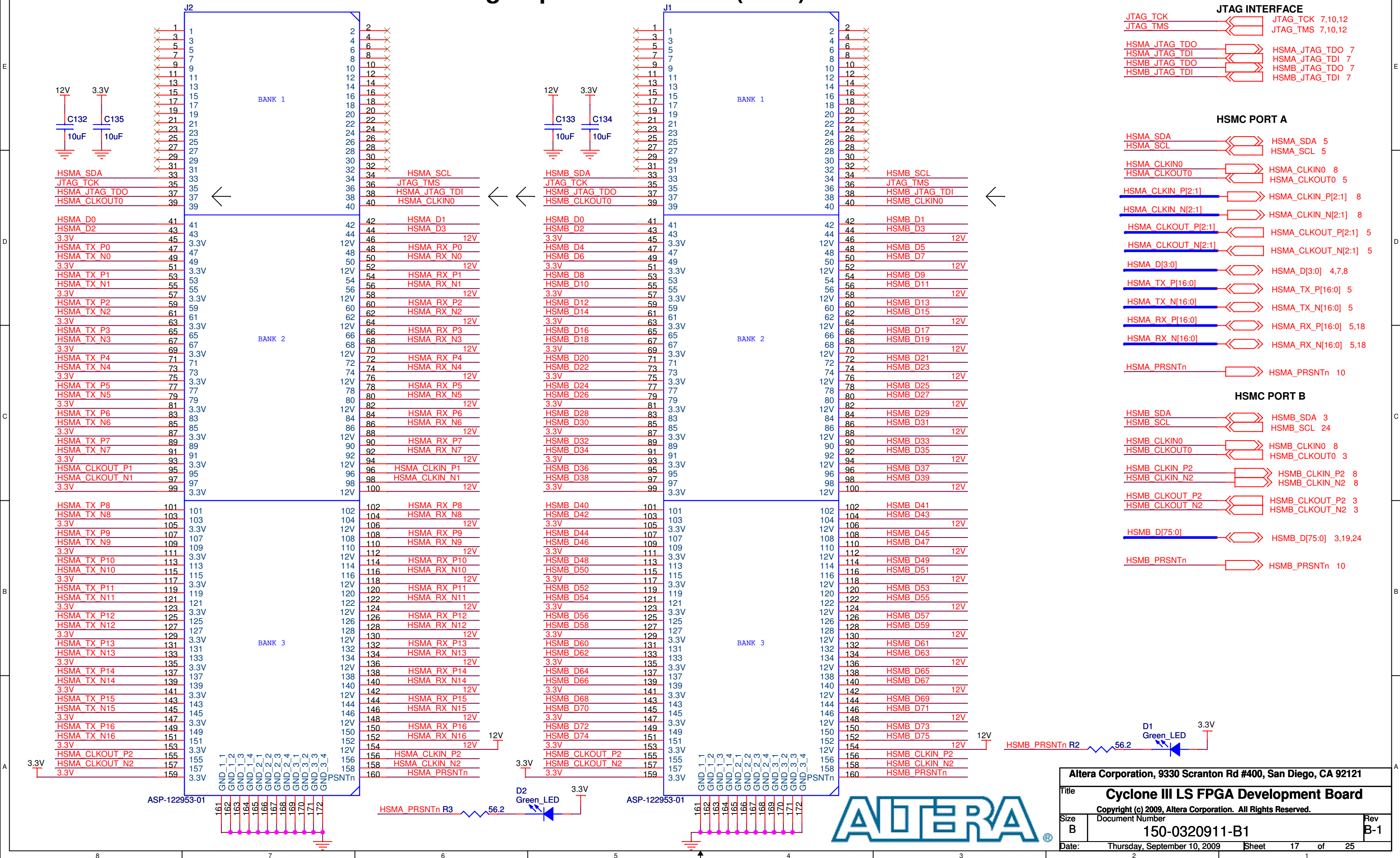
DDR2 SDRAM BANK 7 SIGNALS



DDR2 SDRAM BANK 8 SIGNALS

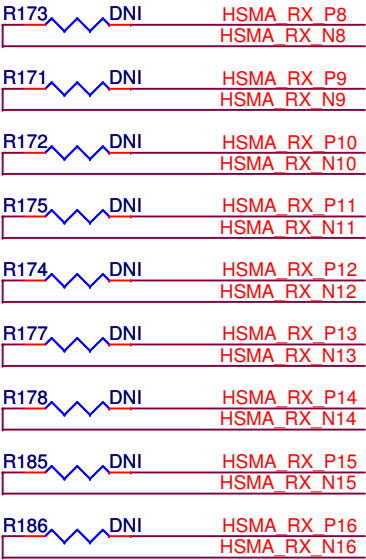
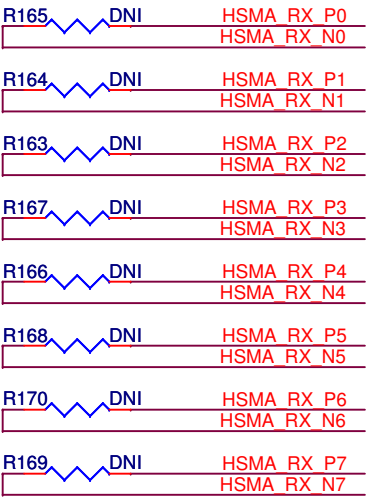


High Speed Mezzanine (HSM) Interface



High Speed Mezzanine (HSM) Termination

By default all of the data signal on the HSMC's are single ended. 100 Ohm resistors should be installed between the P/N pairs in order to use differential signals. Place near C3LS.

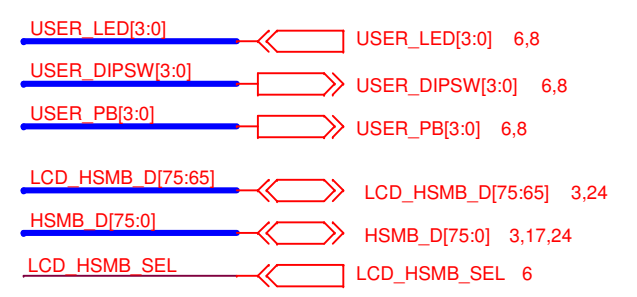
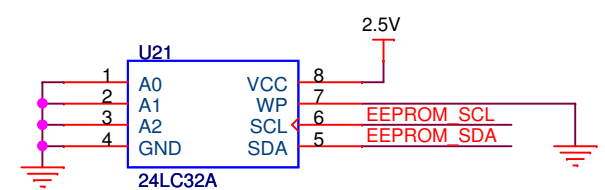
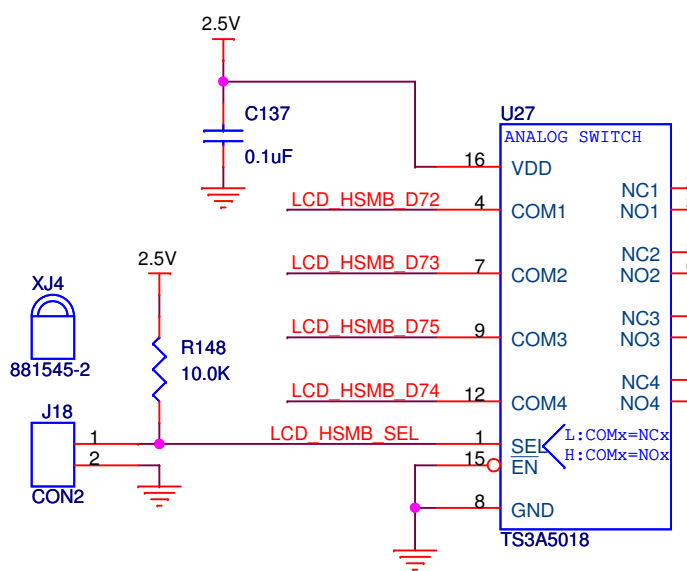
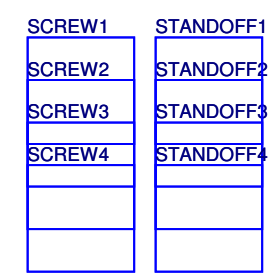
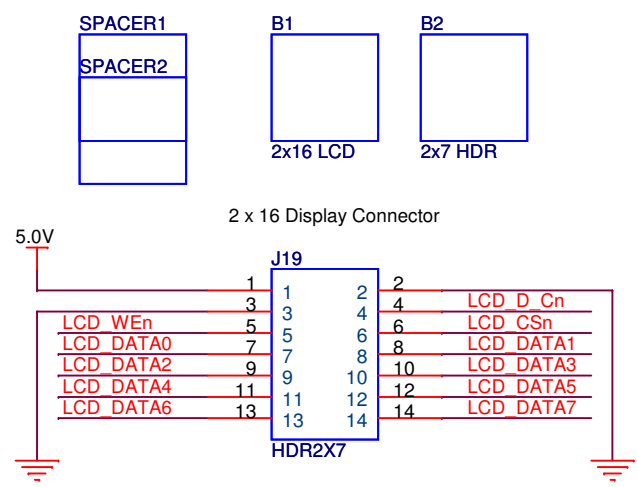
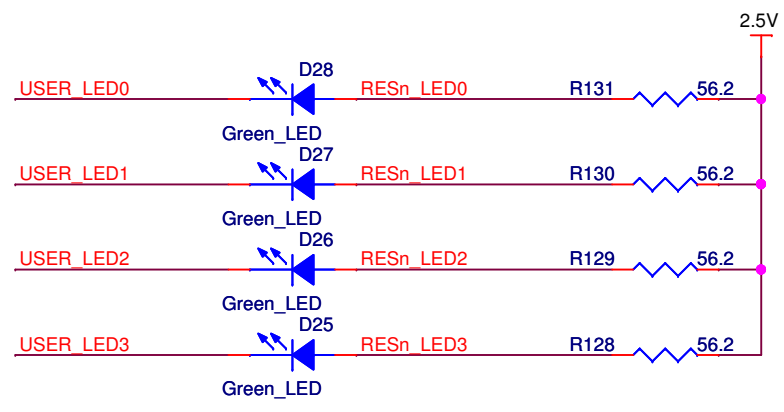


HSMC PORT A



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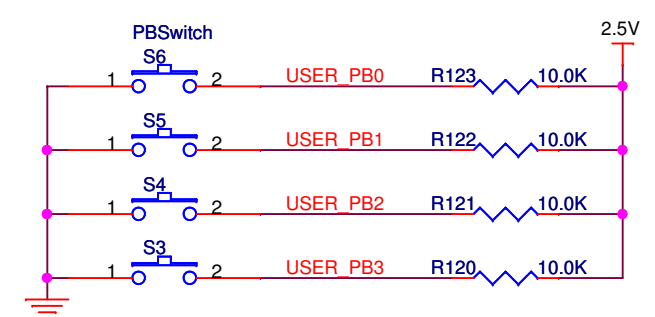
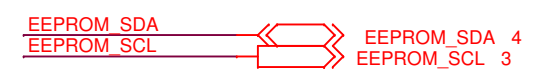
User IO Cyclone III LS



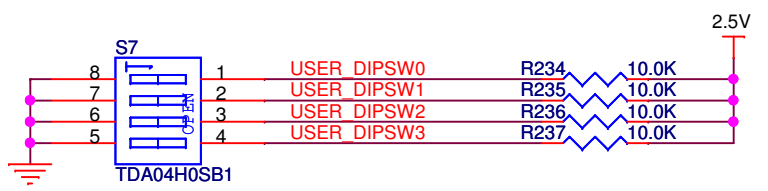
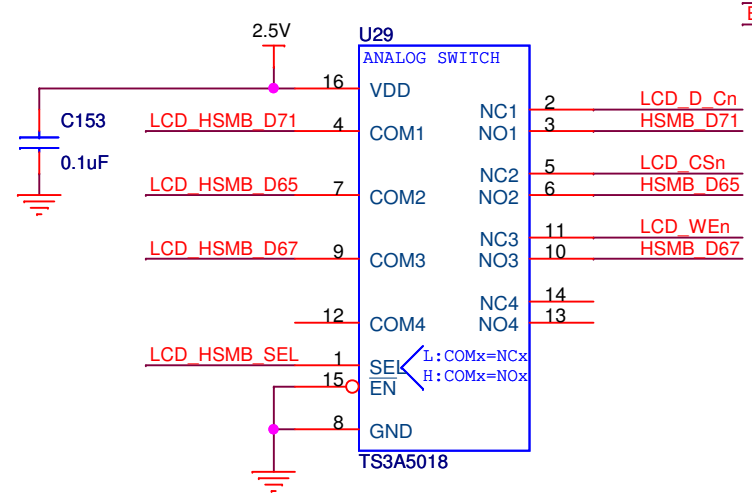
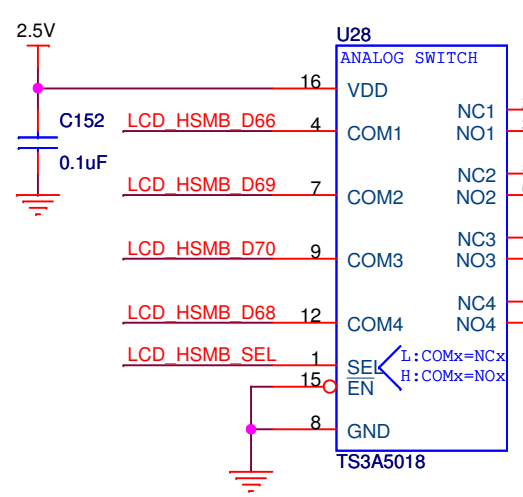
USER IO



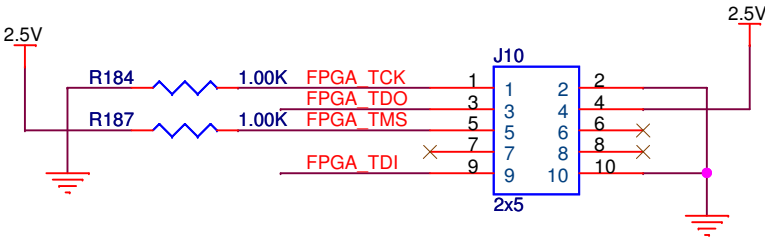
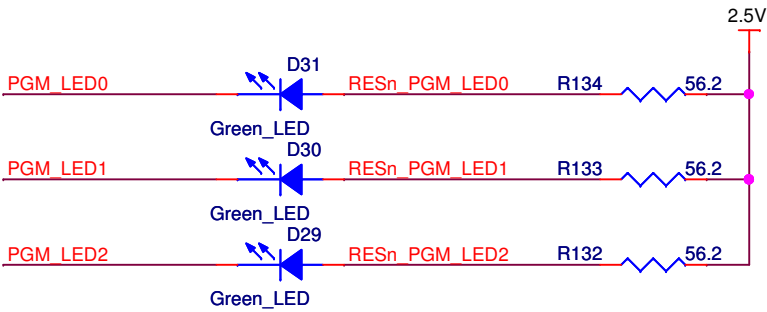
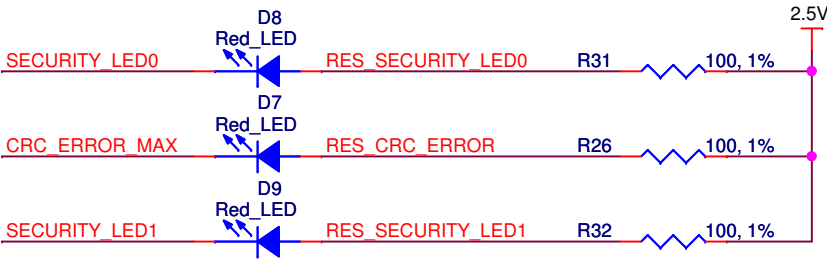
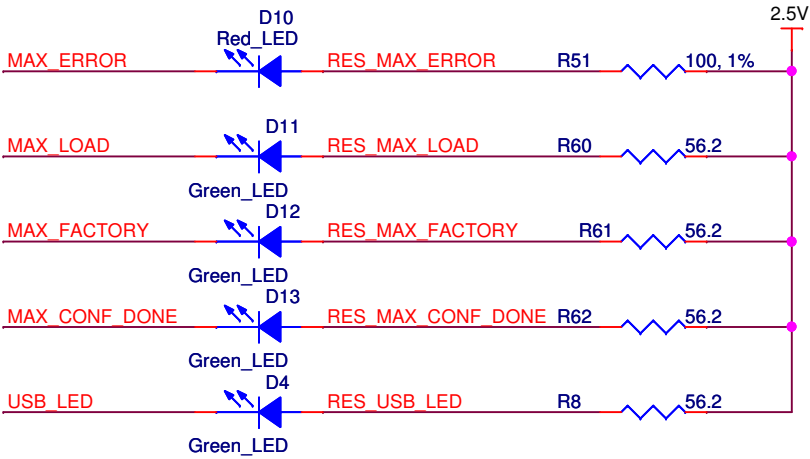
EEPROM SIGNALS



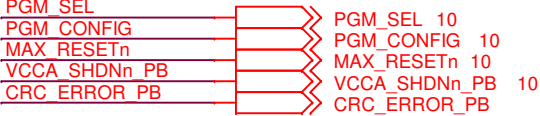
LCD_HSMB_SEL = '1' Jumper Off -> Select HSMB Data Signals.
LCD_HSMB_SEL = '0' Jumper On -> Select LCD Signals.



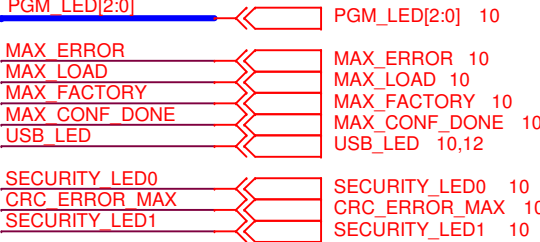
USER IO EPM2210



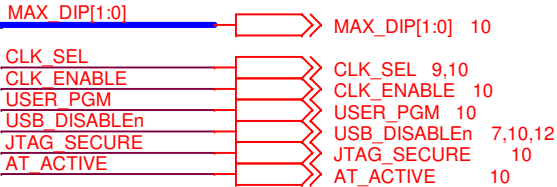
PUSH BUTTON INTERFACE



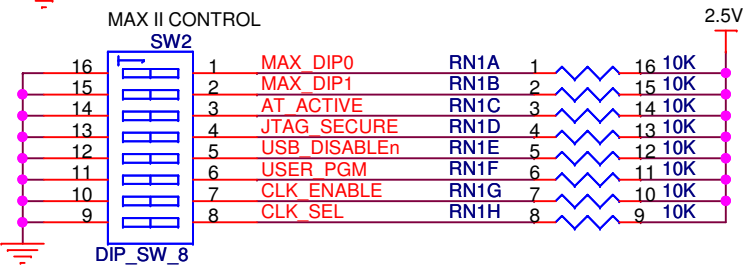
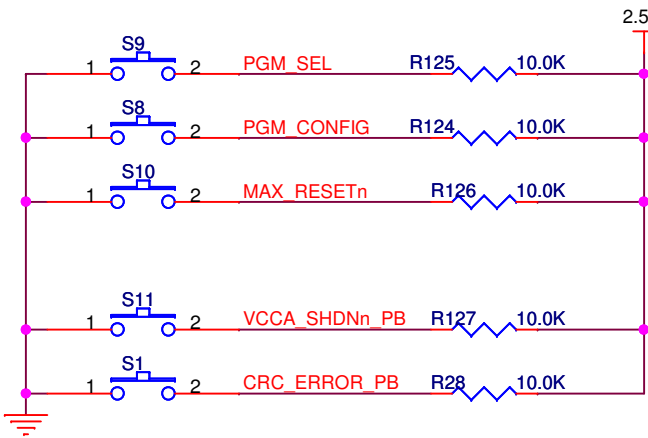
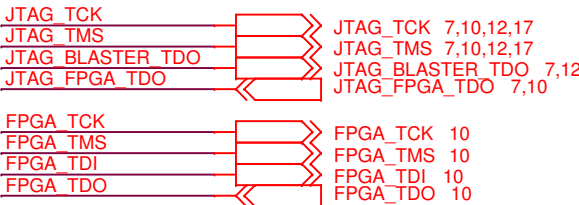
LED INTERFACE



DIP SWITCH INTERFACE

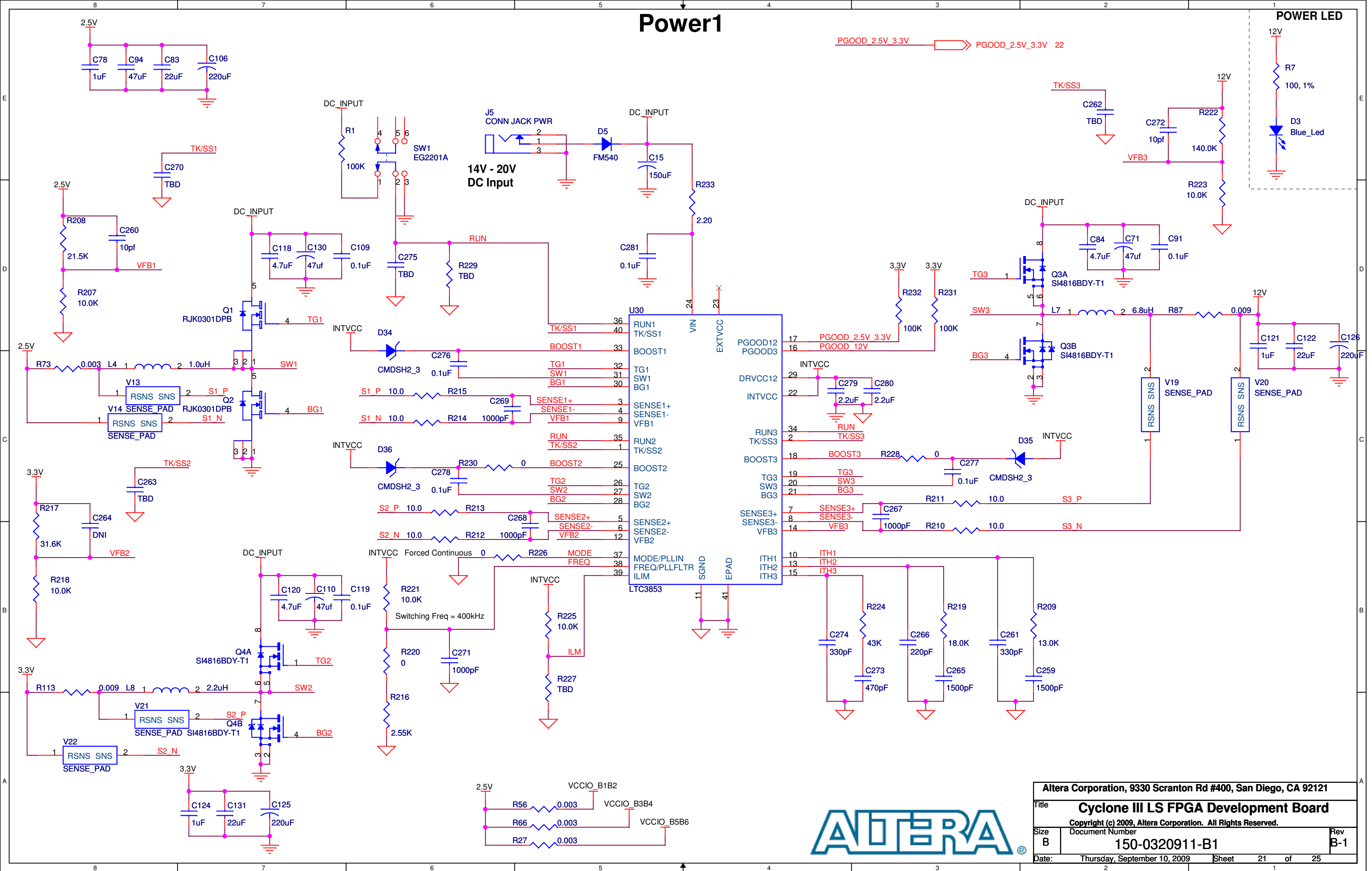


JTAG SIGNALS

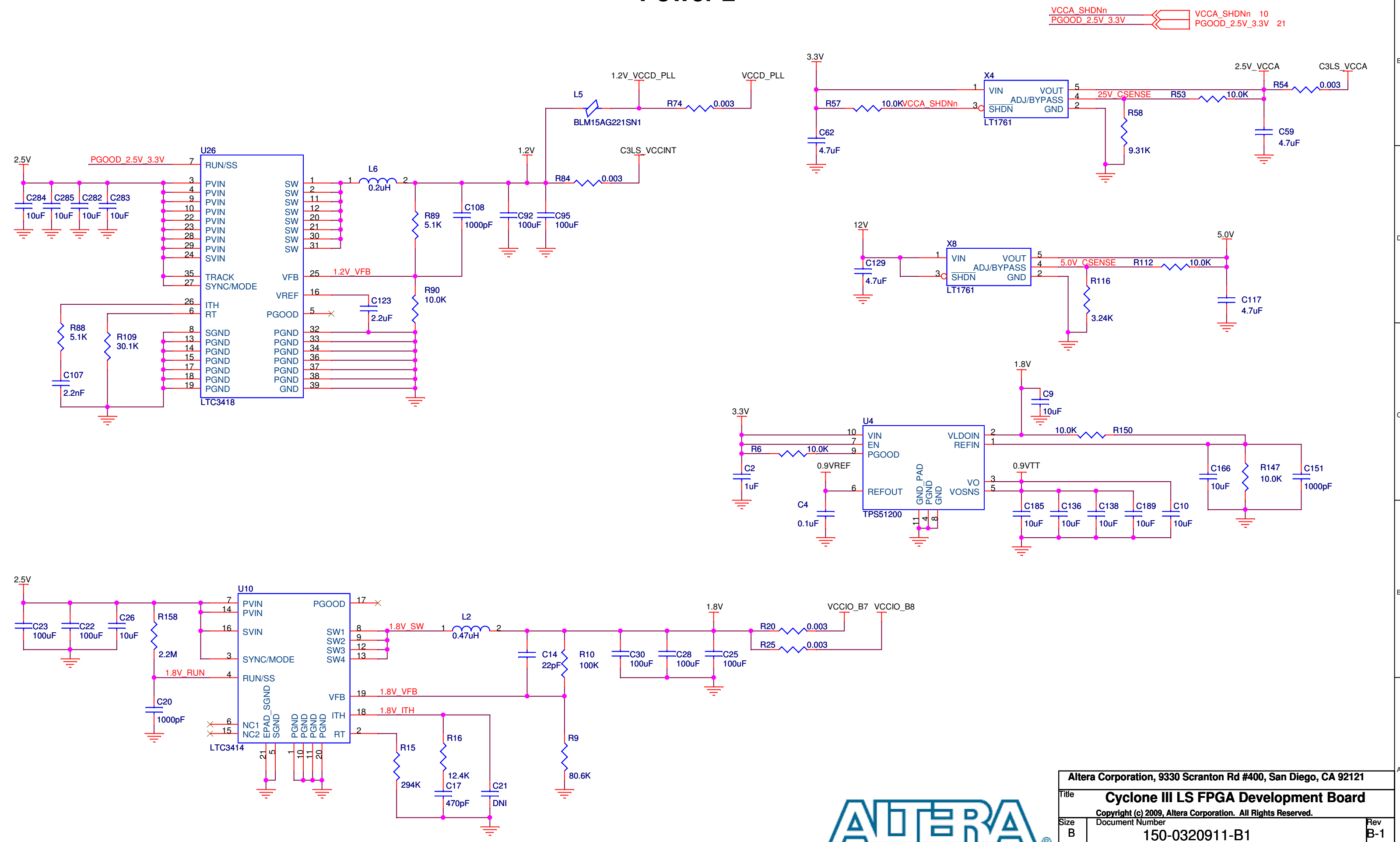


Power1

POWER LED

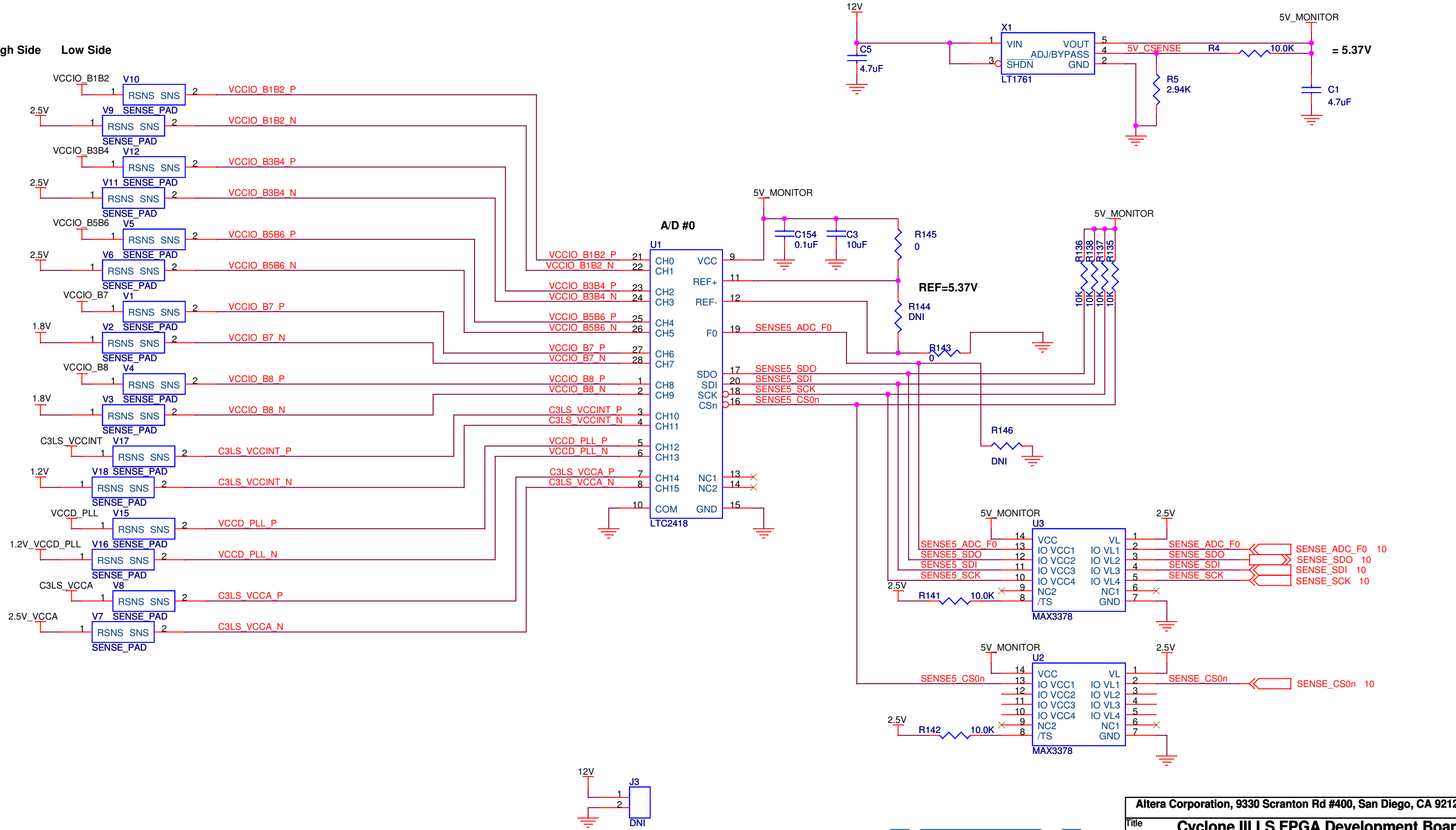


Power 2



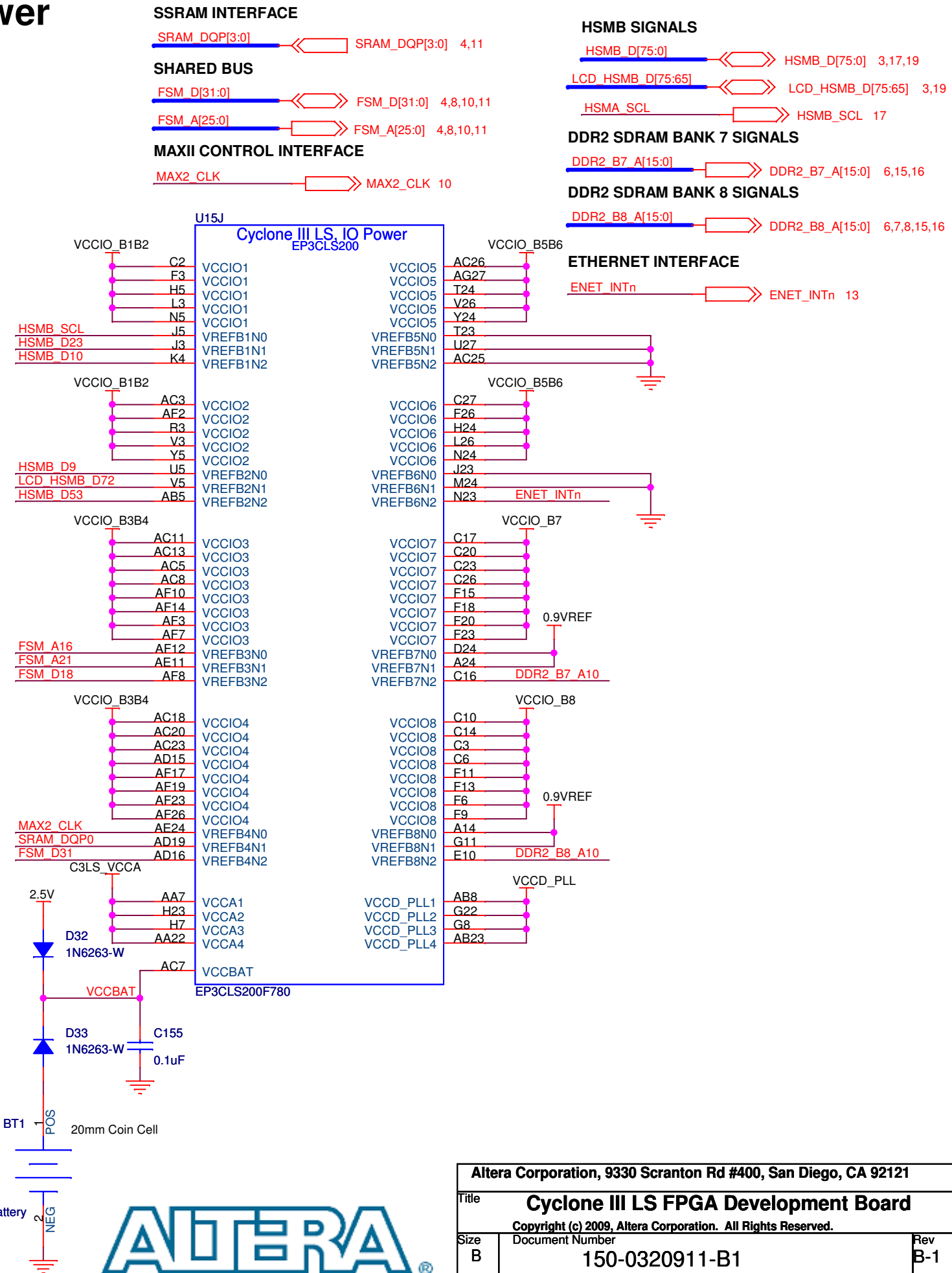
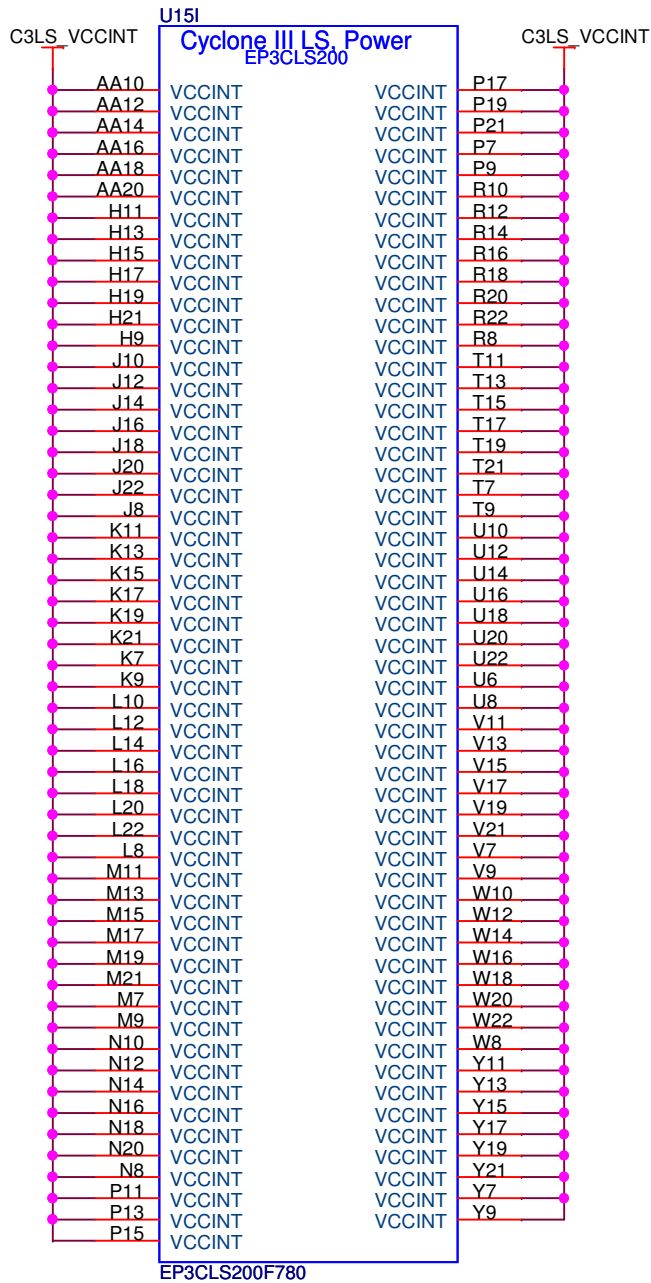
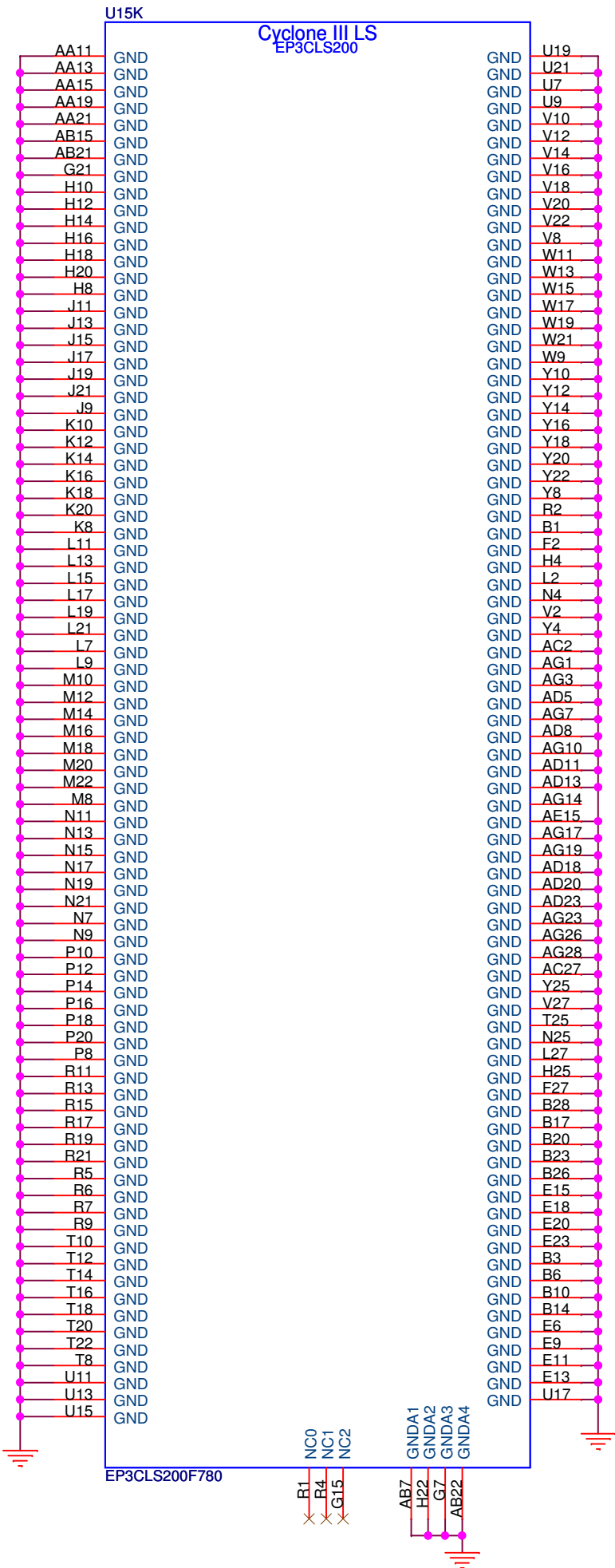
Power Monitor

High Side Low Side



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Cyclone III LS Power



Decoupling

