NOTES:

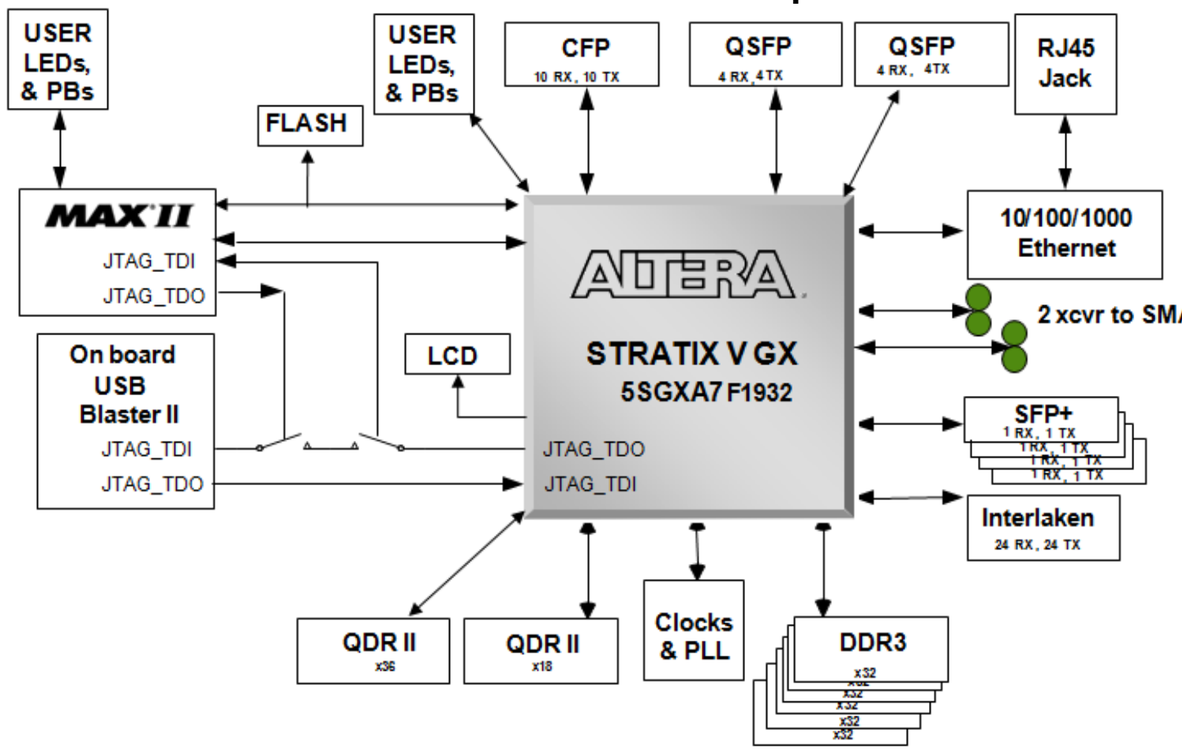
1. Project Drawing Numbers:

Raw PCB	100-0310914-01
Gerber Files	110-0310914-01
PCB Design Files	120-0310914-01
Assembly Drawing	130-0310914-01
Fab Drawing	140-0310914-01
Schematic Drawing	150-0310914-01
PCB Film	160-0310914-01
Bill of Materials	170-0310914-01
Schematic Design Files	180-0310914-01
Functional Specification	210-0310914-01
PCB Layout Guidelines	220-0310914-01
Assembly Rework	320-0310914-01

2. 1436 Parts, 71 Library Parts, 1694 Nets, 9264 Pins

REV	DATE	PAGES	DESCRIPTION
01	06/28/11	All	Initial Design
A	11/01/11	All	Revision A Release

Stratix V GX 100G Development Kit Board



PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	Title, Note, Block Diagram	31	DDR3 Ports C & D
2	Optical POWER	32	DDR3 Ports E & F
3	Power 1	33	QSFP INTERFACE
4	Power 2	34	XCVR Based SFP Connectors
5	Power 3	35	Transceiver Power & CFP
6	Power 4	36	10/100/1000 Ethernet
7	Power 5	37	INTERLAKEN INTERFACE
8	Power 6	38	User IO
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15	Flash		
16	PLL		
17	Clock Circuitry1		
18	Clock Circuitry2		
19	Stratix V GX Clocks		
20	Stratix V GX Config		
21	Stratix V GX Power		
22	Stratix V GX Bank 3		
23	Stratix V GX Bank 4		
24	Stratix V GX Bank 7		
25	Stratix V GX Bank 8		
26	Stratix V GX Left XCVRs		
27	Stratix V GX Right XCVRs		
28	QDRII Memory Ports A & B		
29	QDRII Memory Termination		
30	DDR3 Ports A & B		

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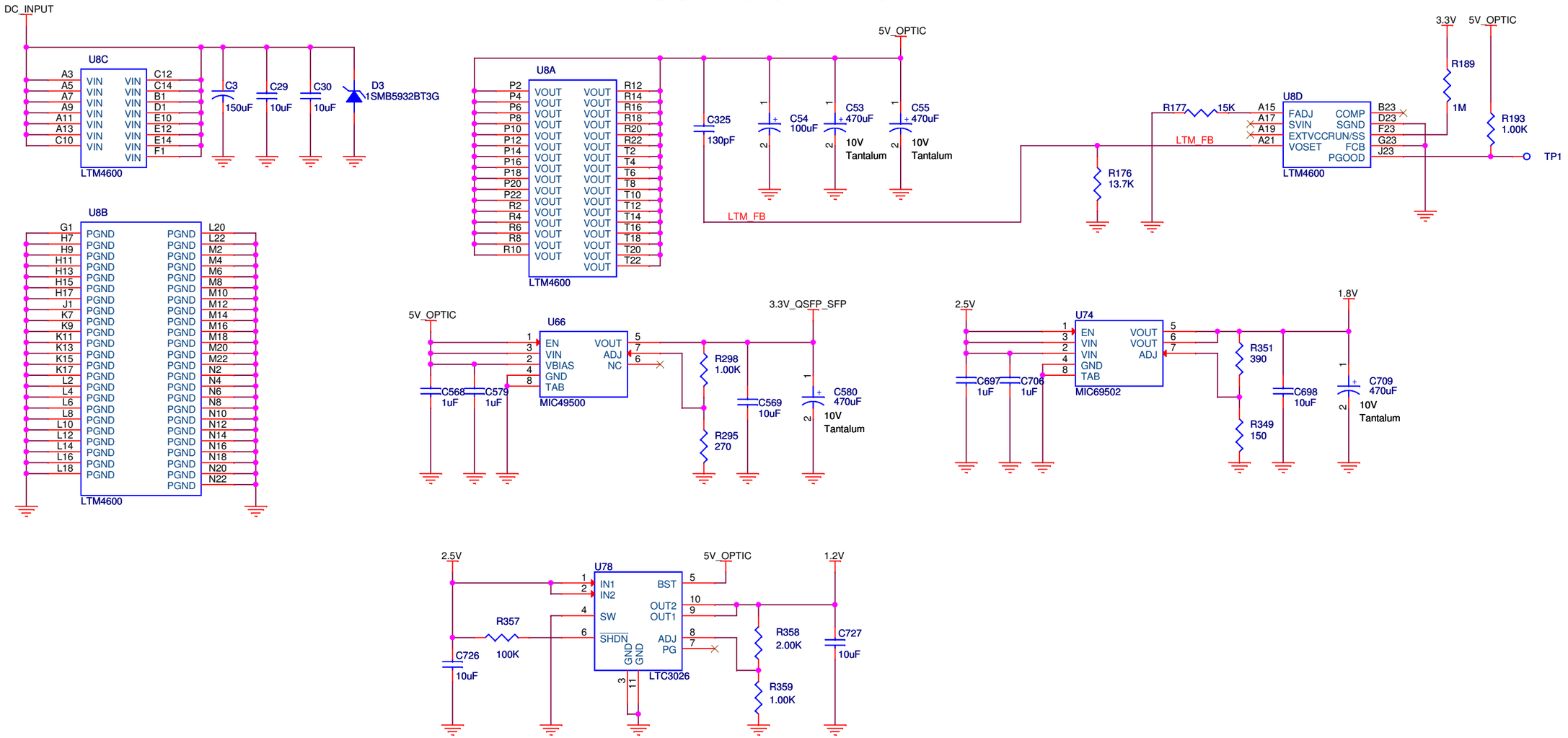
QSFP & SFP+ POWER



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Power 1

14V-20V DC INPUT

J2 — RAPC712X — R4 10.0K — D8 (A2, BaseCC, A1) 12CWQ03FN — PWR_CON — DC_INPUT

U7C — LTM4601 — C9 150uF (35V) — C12 10uF (25V) — C11 10uF (25V) — C13 0.1uF (25V) — D2 20V Zener

U7B — LTM4601

U7A — LTM4601 — C333 100pF — LTM_FB_3.3V — C33 0.1uF — C32 100uF — C31 100uF — C52 470uF 10V Tantalum — C49 10uF — 3.3V

CONTROL SIGNALS

PHASE240 PWR_CTL → PHASE240 PWR_CTL 13,7 13

PWR_ONn — SW1 EG2201A — DC_INPUT — R2 10.0K

U7D — LTM4601 — R179 2.2K — RUN_SW_MAIN — C314 0.01uF — PHASE240 — R178 787K — R197 100K — R194 13.3K — C329 1000pF — PWR_GOOD — LTM_FB_3.3V — R198 DNI — C313 DNI — FSET

POWER LED — R5 100 — D1 Blue_Led

12V power

DC_INPUT — R14 15K — R15 3.00K — 12V_SD — U19 LT1374 — C107 1nF — C101 10uF (25V) — R17 2.2K — C92 0.22uF — D12 MMSD914 — L2 2.2uH — R16 0 — R12 20.0K — R13 4.99K — D13 B530C-13 — C74 100uF — C73 10uF — 5V_MAIN — 12V

12V_ATX_V1 — R6 10.0K

U1 U3 U5 — FDS8870 — 12V_ATX_V1 — 12V_ATX_V2 — DC_INPUT — PWR_CON — 12V

U2 U4 U6 — LTC4357

J1 — 39-29-1047 — C1 47uf — C2 10uF — C10 0.1uF

12V_ATX_V2 — R7 10.0K

12V_SD — Q1 FDV305N — 12V_ATX_V1 — R1 4.99K — R3 3.00K

J3 — PWR_ONn — 5.0V_ATX — 12V_ATX_V1

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Power 2

DC_INPUT

U13C LTM4601 — A1–A5, B1–B3 VIN; B4–B6, C1–C6 VIN

35V C8 150uF | 25V C27 10uF | 25V C26 10uF | 25V C28 0.1uF

D6 20V Zener

VCCOUT_PWRGD → VCCOUT_PWRGD 5,7

3.3V — 100K R182 — VCCOUT_PWRGD — C316 47nF

U13D LTM4601

RUN, INTVCC, DRVCC, PLLIN, TRACK/SS, COMP, MPGM, MARG0, MARG1

PHASE120 — C317 0.01uF

MPGM_2.5V — R181 787K

PGOOD, VFB, DIFFVOUT, VOUT_LCL, VOSNS+, FSET, VOSNS-

2.5V_PWRGD — LTM_FB_2.5V

2.5VIO_PD_CLK_PGM — R180 DNI — FSET2.5V — C315 DNI

2.5VIO_PD_CLK_PGM — C326 100pF — R195 19.1K

PHASE120 → PHASE120 13,9

2.5V_PWRGD → 2.5V_PWRGD 8

U13B LTM4601 — D1–F7, F8–H12 PGND; SGND

U13A LTM4601 — J1–K11, L1–M11 VOUT

2.5V — C48 0.1uF | C47 100uF | C46 100uF

R10 0.003 — C63 470uF 10V Tantalum — C64 470uF 10V Tantalum

2.5VIO_PD_CLK_PGM

0.75V VTT (3A Sink/Src) BANKS 7, 8 DDR3

5V_MAIN — C364 1uF

U64 TPS51100DGQ — VIN, VLDOIN, VDDQSNS, S3, S5, VTTREF, VTT, VTTSNS, PGND, GND, GND

VREF_B7_B8 — R247 10K — R246 10K

1.5V — C365 10uF

VTT_DDR3 — R254 0 — R253 DNI — C366 DNI

C369 10uF | C368 10uF | C370 10uF | C371 10uF | C367 10uF

3.3V — R292 100K — VCCOUT_PWRGD — C540 10uF

U65 LTC3026 — IN1, IN2, SW, SHDN, BST, OUT2, OUT1, ADJ, PG, GND, GND

C552 1uF — R289 21K (1%) — R290 4.02K

L16 BLM15AG221SN1

2.5VP_AUX — R288 0.003 — 2.5V_AUX

C541 — C528 470uF — 10uF — 10V Tantalum — 5V_MAIN

C524 470uF 10V Tantalum

2.5VP_VCCA — R291 0.003 — 2.5V_VCCA_PLL

C542 10uF — C554 470uF 10V Tantalum

0.75V VTT (3A Sink/Src) BANK 3 QDRII

5V_MAIN — C787 1uF

U79 TPS51100DGQ — VIN, VLDOIN, VDDQSNS, S3, S5, VTTREF, VTT, VTTSNS, PGND, GND, GND

VREF_B3 — R397 10K — R396 10K

1.5V — C784 10uF

VTT_B3 — C736 10uF | C783 10uF

0.75V VTT (3A Sink/Src) BANK 4 QDRII

5V_MAIN — C788 1uF

U80 TPS51100DGQ — VIN, VLDOIN, VDDQSNS, S3, S5, VTTREF, VTT, VTTSNS, PGND, GND, GND

VREF_B4 — R399 10K — R398 10K

1.5V — C786 10uF

VTT_B4 — C742 10uF | C785 10uF

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Power 3

0.9V

5V_MAIN

U17C — LTM4627 — VIN

C57 150uF (35V) · C70 10uF (25V) · C69 10uF (25V) · C71 0.1uF (25V)

D10 20V Zener

5V_MAIN

U18C — LTM4627 — VIN

C72 0.1uF

VCC_OUT

U17A — LTM4627 — VOUT

U18A — LTM4627 — VOUT

R11 0.0005

VCC

C97 470uF 10V Tantalum

C85 0.1uF · C84 100uF · C83 100uF · C96 470uF 10V Tantalum

C98 470uF 10V Tantalum · C87 100uF · C86 100uF · C88 0.1uF

U17B — LTM4627 — PGND / SGND

U18B — LTM4627 — PGND / SGND

U17D — LTM4627 — RUN, INTVCC1, INTVCC2, EXTVCC, PLLIN, TRACK/SS, COMP, MTP1–MTP8

RUN_SW2 · C337 47nF · C338 0.01uF · C336 DNI

INT_VCC_C · EXT_VCC_C · PHASE_A · TRACK_C · COMP_C

PGOOD1 · PGOOD2 · VFB · DIFFVOUT · VOUT_LCL · VOSNS+ · FSET · VOSNS-

VCCOUT_PWRGD → VCCOUT_PWRGD 3,7

VCC

C350 220PF Place Near The Regulator Output

LTMC_VFB · VOUT_LCL · VCC_SP

DC_INPUT

30.1K R218

DNI R213 · DNI R212

C346 DNI · C345 1000pF

R227 0 · R226 DNI

Near The Regulator

V5 RSNS SNS SENSE_PAD

PHASE_A · PHASE_B

LTMC_VFB · TRACK_C · COMP_C · RUN_SW2 · VOUT_LCL · INT_VCC_C

6

Near The Regulator

VCC · R224 0 · R225 DNI · VCC_SP

V6 RSNS SNS SENSE_PAD

3.3V · 10K R201 · C335 1000pF · C334 DNI

U18D — LTM4627 — RUN, INTVCC1, INTVCC2, EXTVCC, PLLIN, TRACK/SS, COMP, MTP1–MTP8

RUN_SW2 · INT_VCC_D · EXT_VCC_D · PHASE_B · TRACK_C · COMP_C

PGOOD1 · PGOOD2 · VFB · DIFFVOUT · VOUT_LCL · VOSNS+ · FSET · VOSNS-

LTMC_VFB · VOUT_LCL · INT_VCC_D

DC_INPUT

C351 100pF

DNI R211 · DNI R210

C344 DNI

Installed for 4627 / Not installed for 4627

Installed for 4601 / Not installed for 4601

5V_MAIN · R205 · EXT_VCC_C · R204 · INT_VCC_C

5V_MAIN · R203 0 · EXT_VCC_D · R202 DNI · INT_VCC_D

0 · DNI

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Power 4

PHASE0 → PHASE0 13
PHASE180 → PHASE180 13,9

5V_MAIN

U15C — LTM4627
A1 VIN VIN B4
A2 VIN VIN B5
A3 VIN VIN B6
A4 VIN VIN C1
A5 VIN VIN C2
A6 VIN VIN C3
B1 VIN VIN C4
B2 VIN VIN C5
B3 VIN VIN C6

35V 25V 25V 25V

C56 150uF — C66 10uF — C65 10uF — C67 0.1uF

D9 20V Zener

5V_MAIN

U16C — LTM4627
A1 VIN VIN B4
A2 VIN VIN B5
A3 VIN VIN B6
A4 VIN VIN C1
A5 VIN VIN C2
A6 VIN VIN C3
B1 VIN VIN C4
B2 VIN VIN C5
B3 VIN VIN C6

C68 0.1uF

VCC_OUT

U15A — LTM4627
K1 VOUT VOUT L11
K2 VOUT VOUT M1
K3 VOUT VOUT M2
K4 VOUT VOUT M3
K5 VOUT VOUT M4
K6 VOUT VOUT M5
K7 VOUT VOUT M6
K8 VOUT VOUT M7
K9 VOUT VOUT M8
K10 VOUT VOUT M9
K11 VOUT VOUT M10
L1 VOUT VOUT M11
L2 VOUT VOUT J1
L3 VOUT VOUT J2
L4 VOUT VOUT J3
L5 VOUT VOUT J4
L6 VOUT VOUT J5
L7 VOUT VOUT J6
L8 VOUT VOUT J7
L9 VOUT VOUT J8
L10 VOUT VOUT J9
VOUT J10

U16A — LTM4627
K1 VOUT VOUT L11
K2 VOUT VOUT M1
K3 VOUT VOUT M2
K4 VOUT VOUT M3
K5 VOUT VOUT M4
K6 VOUT VOUT M5
K7 VOUT VOUT M6
K8 VOUT VOUT M7
K9 VOUT VOUT M8
K10 VOUT VOUT M9
K11 VOUT VOUT M10
L1 VOUT VOUT M11
L2 VOUT VOUT J1
L3 VOUT VOUT J2
L4 VOUT VOUT J3
L5 VOUT VOUT J4
L6 VOUT VOUT J5
L7 VOUT VOUT J6
L8 VOUT VOUT J7
L9 VOUT VOUT J8
L10 VOUT VOUT J9
VOUT J10

C94 470uF 2 10V Tantalum

C79 0.1uF — C78 100uF — C77 100uF 2 — C93 470uF 10V Tantalum

C95 470uF 10V 2 Tantalum — C81 100uF — C80 100uF — C82 0.1uF

U15B — LTM4627
D1 PGND PGND G4
D2 PGND PGND G5
D3 PGND PGND G6
D4 PGND PGND G7
D5 PGND PGND G8
D6 PGND PGND G9
E1 PGND PGND H1
E2 PGND PGND H2
E3 PGND PGND H3
E4 PGND PGND H4
E5 PGND PGND H5
E6 PGND PGND H6
E7 PGND PGND H7
F1 PGND PGND H8
F2 PGND PGND H9
F3 PGND PGND B7
F4 PGND PGND C7
F5 PGND PGND D8
F6 PGND PGND B9
F7 PGND PGND C9
F8 PGND PGND E9
F9 PGND
G1 PGND G11
G2 PGND SGND H11
G3 PGND SGND H12

U16B — LTM4627
D1 PGND PGND G4
D2 PGND PGND G5
D3 PGND PGND G6
D4 PGND PGND G7
D5 PGND PGND G8
D6 PGND PGND G9
E1 PGND PGND H1
E2 PGND PGND H2
E3 PGND PGND H3
E4 PGND PGND H4
E5 PGND PGND H5
E6 PGND PGND H6
E7 PGND PGND H7
F1 PGND PGND H8
F2 PGND PGND H9
F3 PGND PGND B7
F4 PGND PGND C7
F5 PGND PGND D8
F6 PGND PGND B9
F7 PGND PGND C9
F8 PGND PGND E9
F9 PGND
G1 PGND G11
G2 PGND SGND H11
G3 PGND SGND H12

U15D — LTM4627
RUN_SW2 → A10 RUN
INT_VCC_E → A7 INTVCC1
D9 INTVCC2
EXT_VCC_E → E12 EXTVCC
PHASE_C → A8 PLLIN
TRACK_C → A9 TRACK/SS
COMP_C → A11 COMP
A12 MTP1
B11 MTP2
C11 MTP3
C10 MTP4
C12 MTP5
D10 MTP6
D11 MTP7
D12 MTP8

PGOOD1 F11
PGOOD2 G12
VFB F12 → LTMC_VFB
DIFFVOUT K12
VOUT_LCL L12 → VOUT_LCL

VOSNS+ J12
FSET B12
VOSNS- M12 → INT_VCC_E

C342 47nF — C343 0.01uF — C341 DNI

C353 100pF

DNI R217 — DNI R216

DC_INPUT — C349 DNI — C348 1000pF

Place Near The Regulator Output

INT_VCC_C → INT_VCC_C 5

INT_VCC_C
C58 0.1uF
DNI R200
R8 100K

U14 — LTC6902
1 V+ SET 10
2 DIV MOD 9
3 PH GND 8
4 OUT1 OUT4 7
5 OUT2 OUT3 6

INT_VCC_C 3
PHASE_A 4 ← PHASE_A
PHASE_B 5 ← PHASE_B
PHASE_D 7
PHASE_C 6

LTMC_VFB → LTMC_VFB 5
TRACK_C → TRACK_C 5
COMP_C → COMP_C 5
RUN_SW2 → RUN_SW2 5
VOUT_LCL → VOUT_LCL 5

U16D — LTM4627
RUN_SW2 → A10 RUN
INT_VCC_F → A7 INTVCC1
D9 INTVCC2
EXT_VCC_F → E12 EXTVCC
PHASE_D → A8 PLLIN
TRACK_C → A9 TRACK/SS
COMP_C → A11 COMP
A12 MTP1
B11 MTP2
C11 MTP3
C10 MTP4
C12 MTP5
D10 MTP6
D11 MTP7
D12 MTP8

PGOOD1 F11
PGOOD2 G12
VFB F12 → LTMC_VFB
DIFFVOUT K12
VOUT_LCL L12 → VOUT_LCL

VOSNS+ J12
FSET B12
VOSNS- M12 → INT_VCC_F

C340 1000pF — C339 DNI

DNI R215 — DNI R214

DC_INPUT — C347 DNI — C352 100pF

Installed for 4627 Not installed for 4601
Installed for 4601 Not installed for 4627

5V_MAIN — R209 — EXT_VCC_E — R208 — INT_VCC_E
5V_MAIN — R207 0 — EXT_VCC_F — R206 DNI — INT_VCC_F
0 DNI

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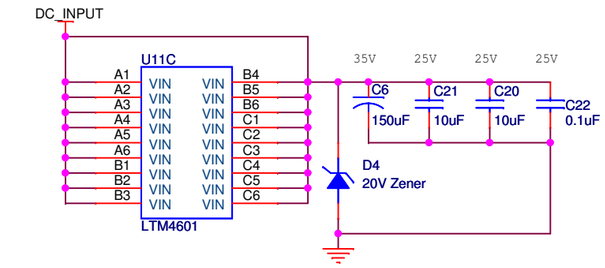
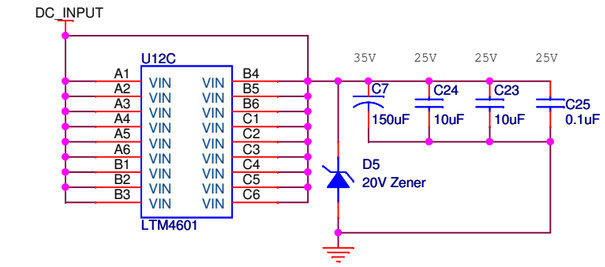
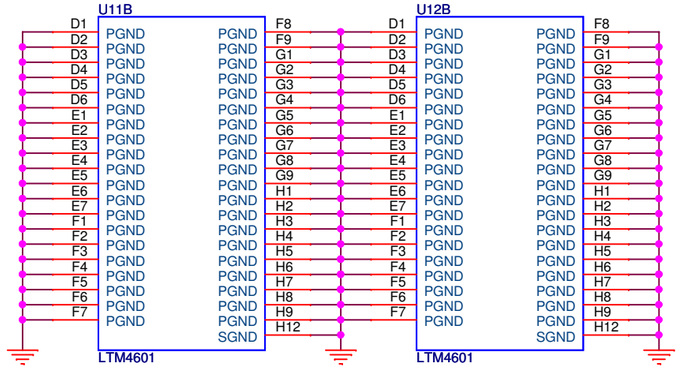
Power 4

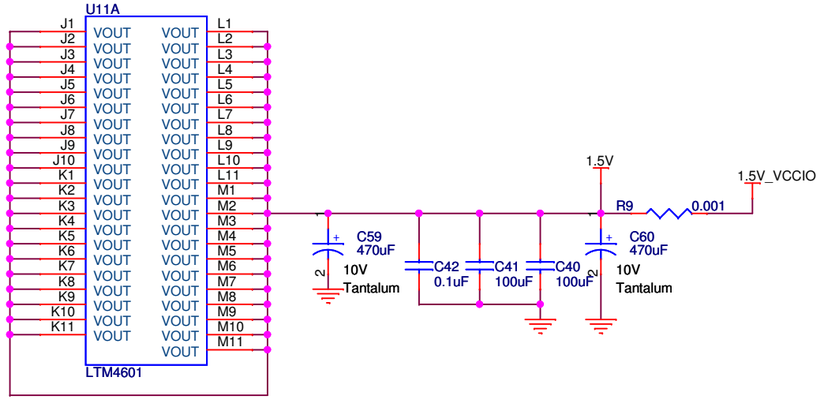
Regulator Sense Signals

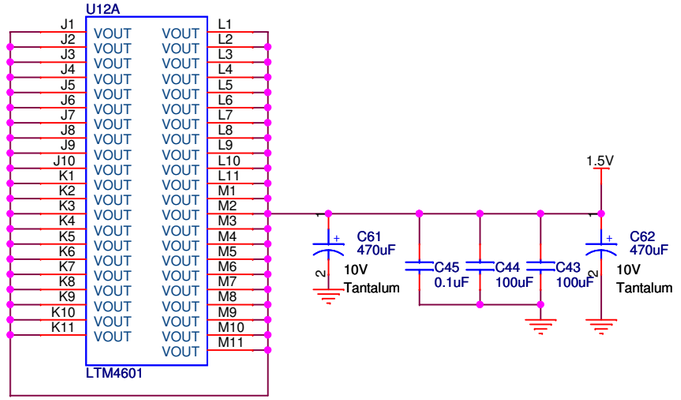
LT4601 SWITCHER

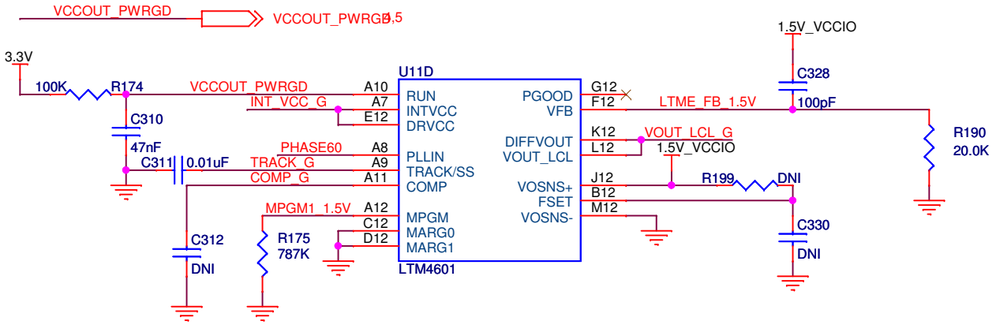


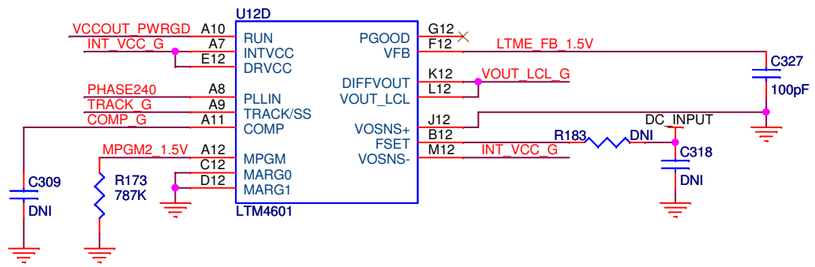












PHASE60 → PHASE60 13

PHASE240 → PHASE240 13.3

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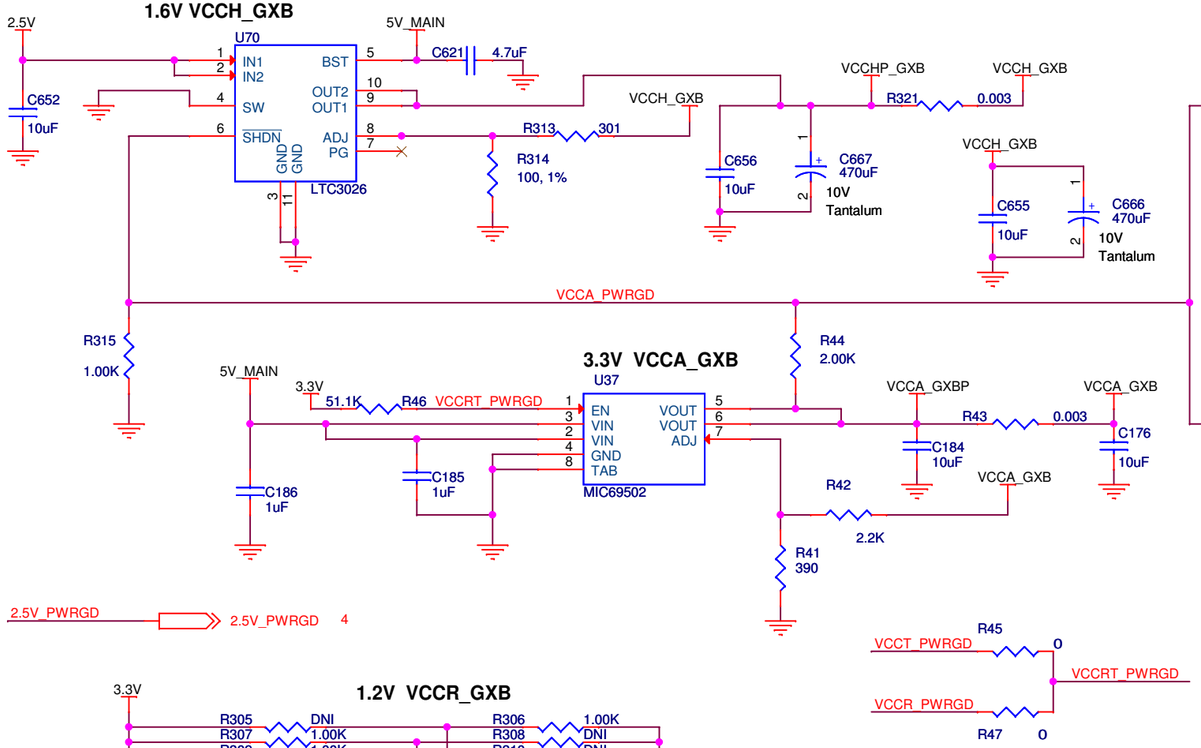
Power 5



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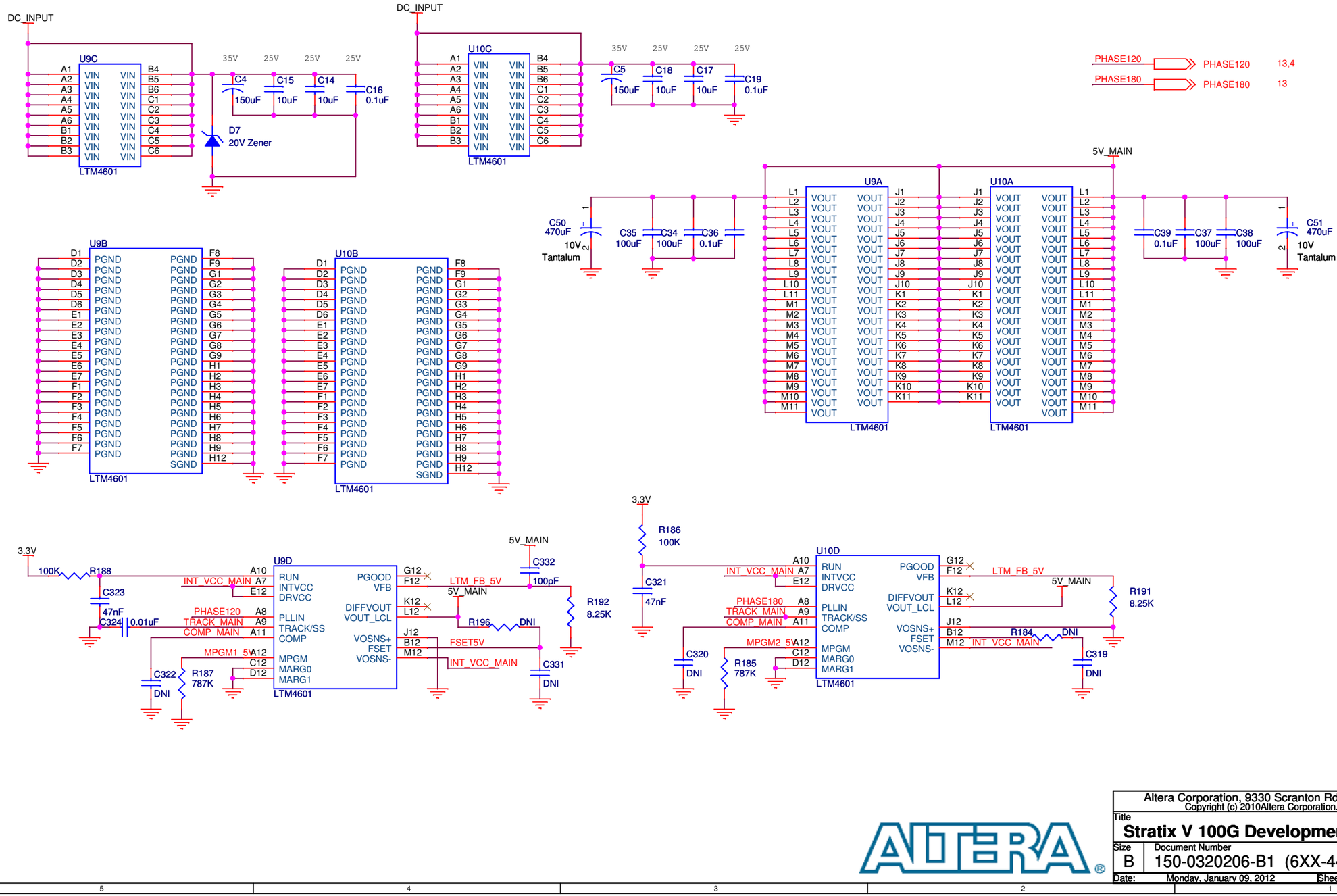
Power Bias, Power 6



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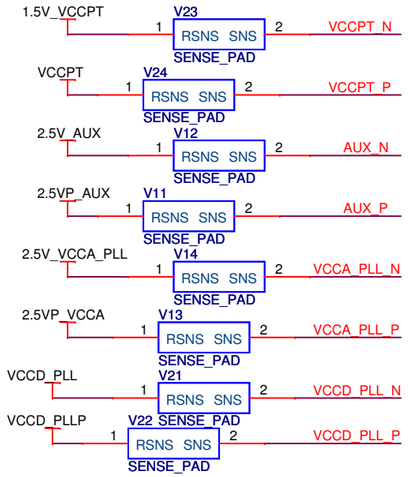
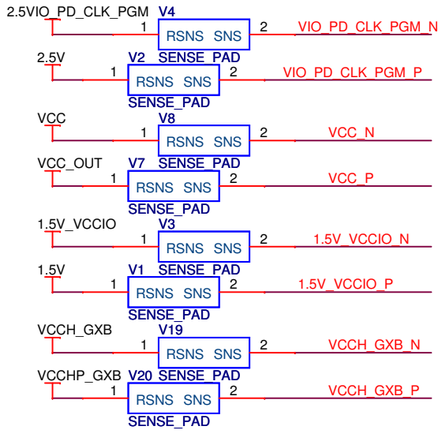
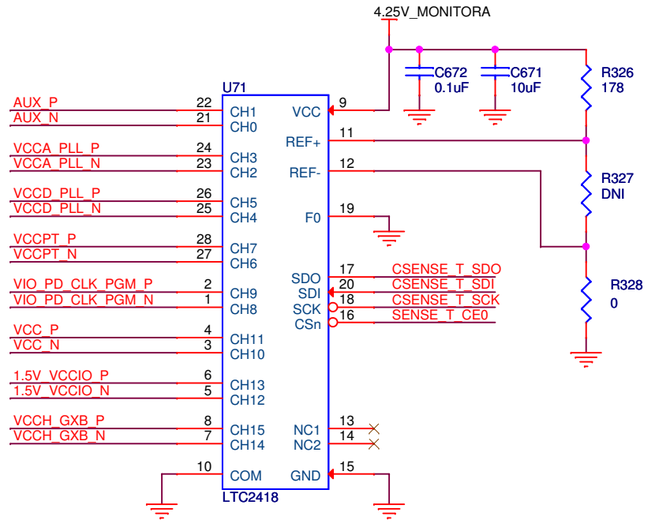
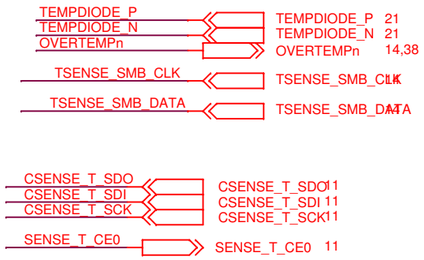
Power Monitor



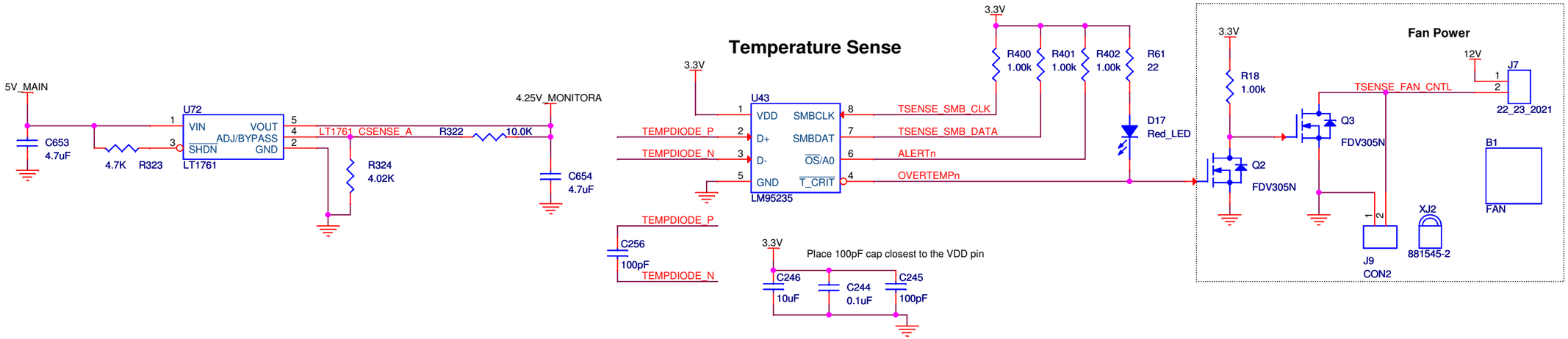




CURRENT & TEMP SENSE SIGNALS



Temperature Sense



Fan Power

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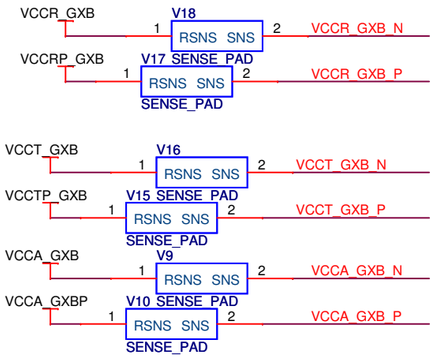
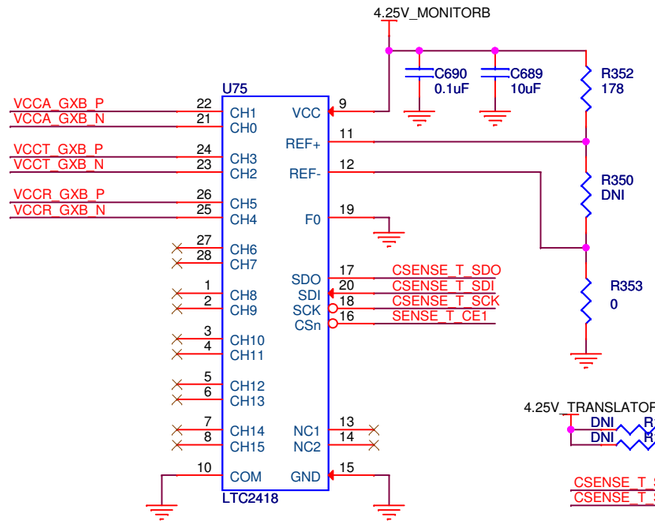
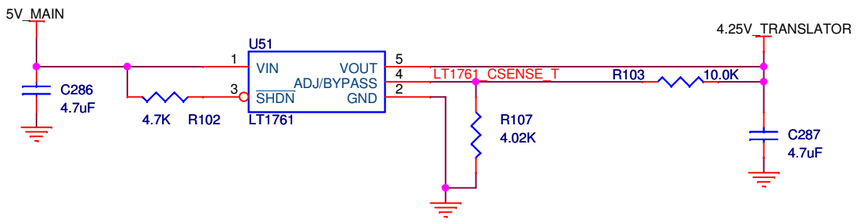
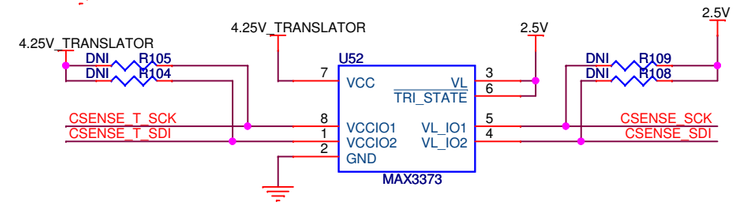
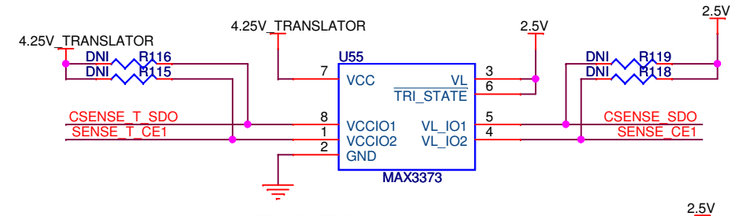
Power Monitor

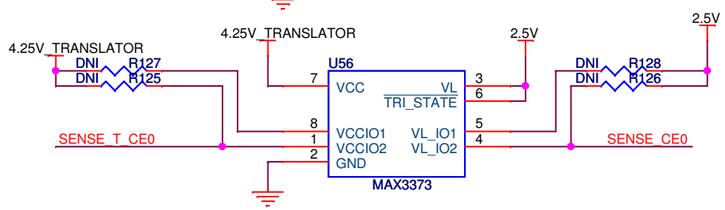


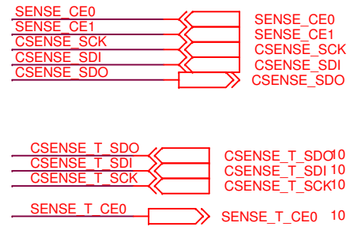


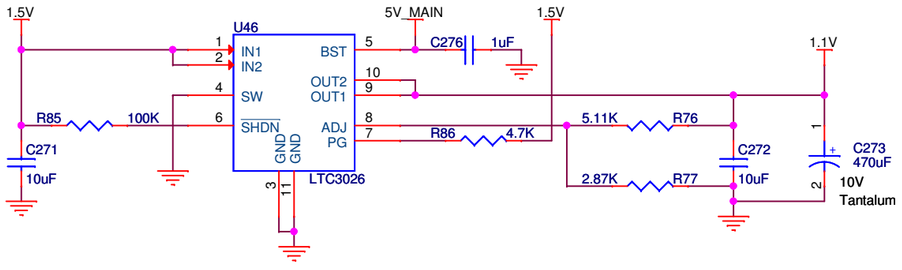


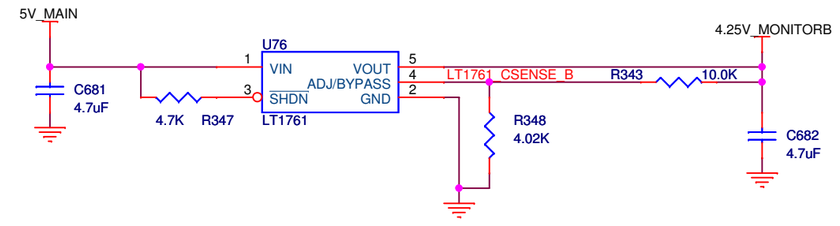












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On-Board USB Blaster II

STRATIX V USB INTERFACE

USB_DATA[7..0] — USB_DATA[7..0] 19,22,23
USB_ADDR[1..0] — USB_ADDR[1..0]22,23
USB_FULL — USB_FULL 22
USB_EMPTY — USB_EMPTY 23
USB_SCL — USB_SCL 22
USB_SDA — USB_SDA 23
USB_CLK — USB_CLK 19
USB_RESETn — USB_RESETn 23
USB_OEn — USB_OEn 22
USB_RDn — USB_RDn 23
USB_WRn — USB_WRn 22
USB_CFG[11..0] — USB_CFG[11..0] 19,22,23
EXTRA_SIG[2..0] — EXTRA_SIG[2..0]19,22,23
JTAG_FPGA_TDO_RETIMER — 20
USB_DISABLEn — USB_DISABLEn 20,38
M570_CLOCK — M570_CLOCK 14
FACTORY_STATUS — FACTORY_STATUS 14
FACTORY_REQUEST — FACTORY_REQUEST 14

MAXII USB INTERFACE

FPGA_JTAG_TCK — FPGA_JTAG_TCK 3,20
FPGA_JTAG_TMS — FPGA_JTAG_TMS 3,20
JTAG_BLASTER_TDI — JTAG_BLASTER_TDI 20
JTAG_BLASTER_TDO — JTAG_BLASTER_TDO 20

J65 USB CON: 1 VBUS_5V, 2 FX2_D_N, 3 FX2_D_P, 4 R134 DNI, 6, 5
U61: TPD2EUSB30 (D+, D-, GND)
1M R147, 4.7nF C307

FX2_SDA R439 0 MAX_SDA
U81: MAX811 (GND, VCC, RESET, MR)
C844 0.1uF
100K R436 FX2_RESETn

U63: CY7C68013A_SSOP56
AVCC, VCC, RESET, SCL, SDA, WAKEUP, CTL0, CTL1, CTL2, DMINUS, DPLUS, RDY0, RDY1, IFCLK, XTALIN, XTALOUT, CLKOUT, PA0–PA7, PB0–PB7, PD0–PD7, RESERVED, AGND, GND
FX2_RESETn, FX2_SCL, FX2_SDA, FX2_WAKEUP, FX2_FLAGA, FX2_FLAGB, FX2_FLAGC, FX2_SLRDn, FX2_SLWRn, FX2_PA0–FX2_PA7, FX2_PB0–FX2_PB7, FX2_PD0–FX2_PD7
R440 2.00K, R435 2.00K

Y4 24.00MHz
C843 12pF, C836 12pF
USB_CLK, 24M_XTALIN, 24M_XTALOUT

VBUS_5V R431 10.0K FX2_WAKEUP
R432 20.0K, C838 0.1uF

PLACE NEAR CY7C68013A
C835 C837 C834 C850 C848 C849 C851 C847 — 0.1uF

D35 Green_LED: JTAG_RX, RESn_JTAG_RX, R451 56.2
D36 Green_LED: JTAG_TX, RESn_JTAG_TX, R450 56.2
D37 Green_LED: SC_RX, RESn_SC_RX, R449 56.2
D38 Green_LED: SC_TX, RESn_SC_TX, R448 56.2

R423 1.00k USB_SCL
R424 1.00k USB_SDA
R425 1.00k USB_FULL
R422 1.00k USB_EMPTY
R430 1.00k FACTORY_REQUEST

J66 DNI
R415 1.00K C_USB_MAX_TCK
R416 1.00K C_USB_MAX_TDO, C_USB_MAX_TMS, C_USB_MAX_TDI

U62A: MAX II BANK1 — EPM570F100
FX2_PA2, FX2_PA7, FX2_FLAGC, FX2_PA4, FX2_PA3, FX2_FLAGA, FX2_PB4, FX2_PB2, FX2_FLAGB, FX2_PA6, FX2_PB5, FX2_PA1, FX2_PB0, FX2_PB1, FPGA_JTAG_TDO, JTAG_FPGA_TDO_RETIMER
FX2_SLWRn, FX2_SLRDn, FX2_PB6, FX2_PD7, FX2_PD5, FX2_PB3, FX2_PA5, FX2_SCL, USB_DISABLEn, C_JTAG_TMS, FX2_PD6, C_JTAG_TDI, FX2_PD4, C_JTAG_TCK, FX2_PB7, C_JTAG_TDO, USB_CLK, MAX_SDA, FX2_RESETn
FX2_PD0 0 R444 C_USB_MAX_TCK, FX2_PD2 0 R446 C_USB_MAX_TDI, FX2_PD1 0 R438 C_USB_MAX_TMS, FX2_PD3 0 R447 C_USB_MAX_TDO
JTAG_FPGA_TDO_RETIMER 0 R445 FPGA_JTAG_TDO — FPGA_JTAG_TDO 3,20

U62B: MAX II BANK2 — EPM570F100
JTAG_TX, USB_CFG8, JTAG_RX, USB_CFG9, FACTORY_REQUEST, USB_CFG10, USB_DATA0, USB_RESETn, USB_OEn, USB_DATA1, USB_DATA7, USB_RDn, USB_DATA2, USB_WRn, USB_DATA4, SC_RX, USB_CFG0–USB_CFG7
USB_DATA5, USB_DATA6, USB_EMPTY, USB_SCL, USB_SDA, EXTRA_SIG0, EXTRA_SIG1, EXTRA_SIG2, SC_TX, FACTORY_STATUS, USB_DATA3, USB_ADDR0, USB_ADDR1, USB_FULL, USB_CFG11, M570_CLOCK
C_JTAG_TCK 0 R437 FPGA_JTAG_TCK, C_JTAG_TMS 0 R441 FPGA_JTAG_TMS, C_JTAG_TDI 0 R442 JTAG_BLASTER_TDI, C_JTAG_TDO 0 R429 JTAG_BLASTER_TDO
R443 DNI JTAG_BLASTER_TDI

U62C: MAX II Power — EPM570F100
GNDINT, VCCINT, GNDIO, VCCIO1, VCCIO2
2.5V, 3.3V, 1.5V

PLACE NEAR MAX V (U14)
C846 C842 C841 C830 C832 C833 — 0.1uF

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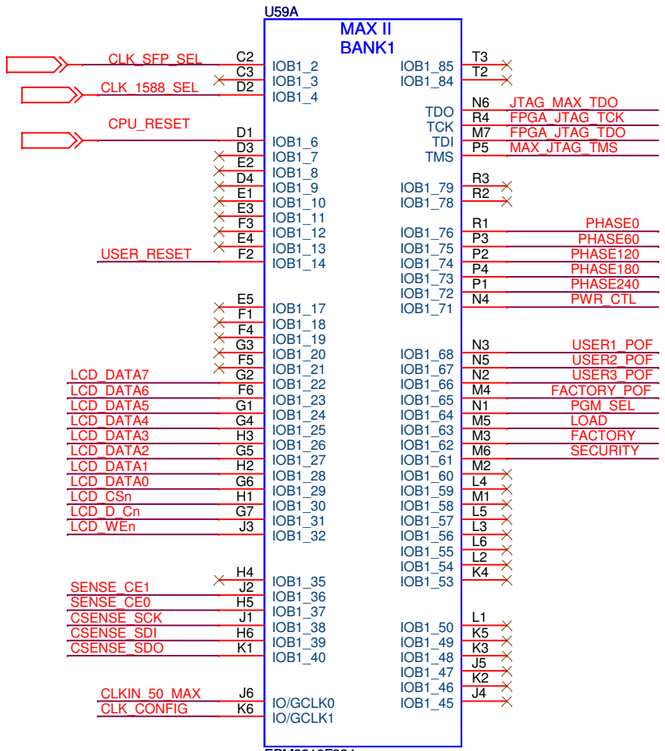
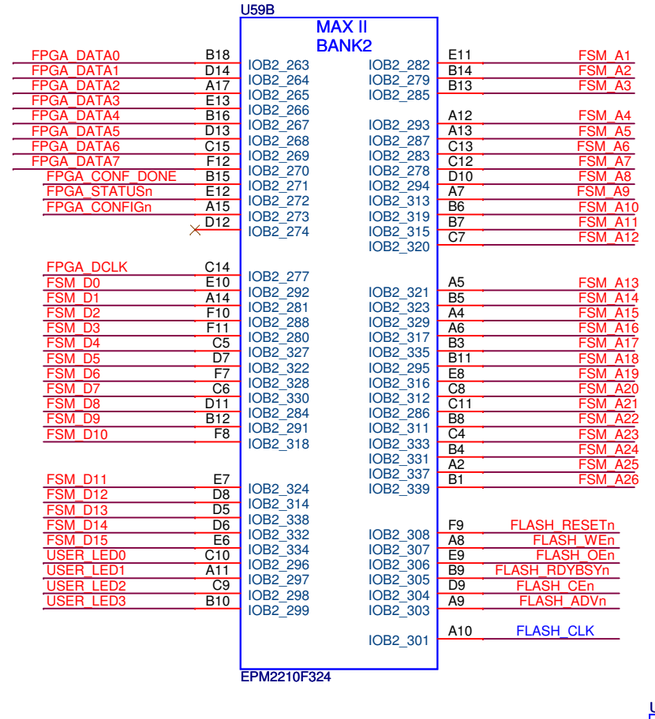
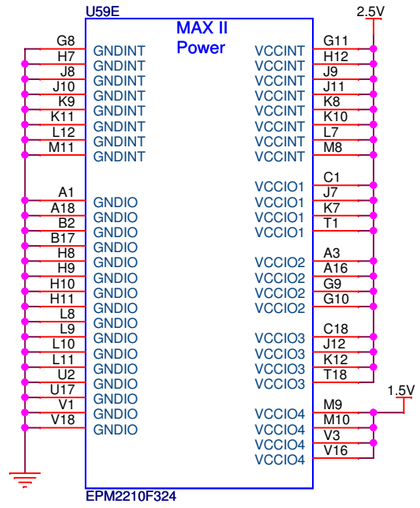
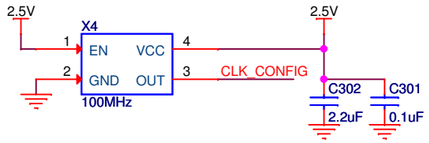
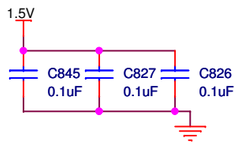
MAX II Banks 1, 2 and Power

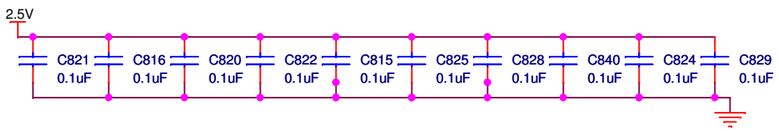












CURRENT SENSE INTERFACE

SENSE_CE1 → SENSE_CE1 11
SENSE_CE0 → SENSE_CE0 11
CSENSE_SCK → CSENSE_SCK 11
CSENSE_SDI → CSENSE_SDI 11
CSENSE_SDO → CSENSE_SDO 11

PHASE0 → PHASE0
PHASE60 → PHASE60 7
PHASE120 → PHASE120 4,9
PHASE180 → PHASE180 9
PHASE240 → PHASE240 3,7
PWR_CTL → PWR_CTL

USER1_POF → USER1_POF 38
USER2_POF → USER2_POF 38
USER3_POF → USER3_POF 38
FACTORY_POF → FACTORY_POF 38

PGM_SEL → PGM_SEL 38
LOAD → LOAD 38
FACTORY → FACTORY 38

USER_RESET → USER_RESET 22,38

FLASH INTERFACE

FSM_D[15..0] → FSM_D[15..0] 15,19,20,22,23
FSM_A[26..1] → FSM_A[26..1] 15,19,20,22,23
FLASH_RESETn → FLASH_RESETn 15,22
FLASH_WEn → FLASH_WEn 15,23
FLASH_OEn → FLASH_OEn 15,19
FLASH_RDYBSYn → FLASH_RDYBSYn 15,23
FLASH_CEn → FLASH_CEn 15,23
FLASH_ADVn → FLASH_ADVn 15,22
FLASH_CLK → FLASH_CLK 23

STRATIX V GX CONFIGURATION

FPGA_DATA[7..0] → FPGA_DATA[7..0] 20
FPGA_DCLK → FPGA_DCLK 20
FPGA_STATUSn → FPGA_STATUSn 20
FPGA_CONFIGn → FPGA_CONFIGn 20
FPGA_CONF_DONE → FPGA_CONF_DONE 20

FPGA_JTAG_TCK → FPGA_JTAG_TCK 12,20
MAX_JTAG_TMS → MAX_JTAG_TMS 20
FPGA_JTAG_TDO → FPGA_JTAG_TDO 12,20
JTAG_MAX_TDO → JTAG_MAX_TDO 20

LED INTERFACE

USER_LED[3..0] → USER_LED[3..0] 38
CLKIN_50_MAX → CLKIN_50_MAX 15
SECURITY → SECURITY 14,15

2x16 LED DISPLAY INTERFACE

LCD_DATA[7..0] → LCD_DATA[7..0] 20,22,23,38
LCD_CSn → LCD_CSn 23,38
LCD_D_Cn → LCD_D_Cn 23,38
LCD_WEn → LCD_WEn 22,38

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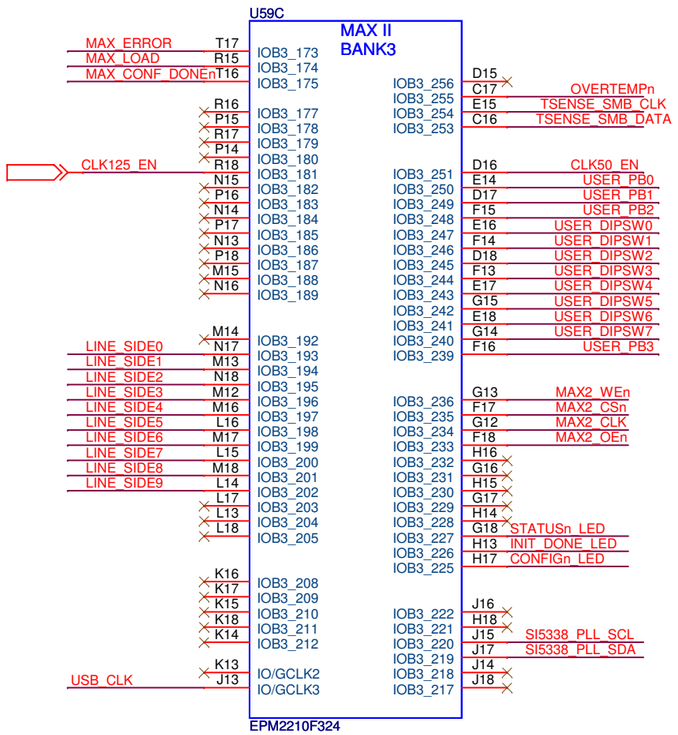
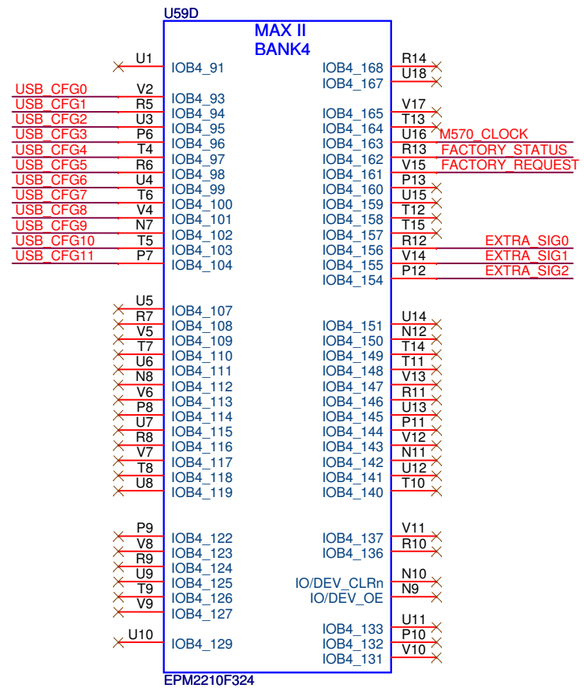
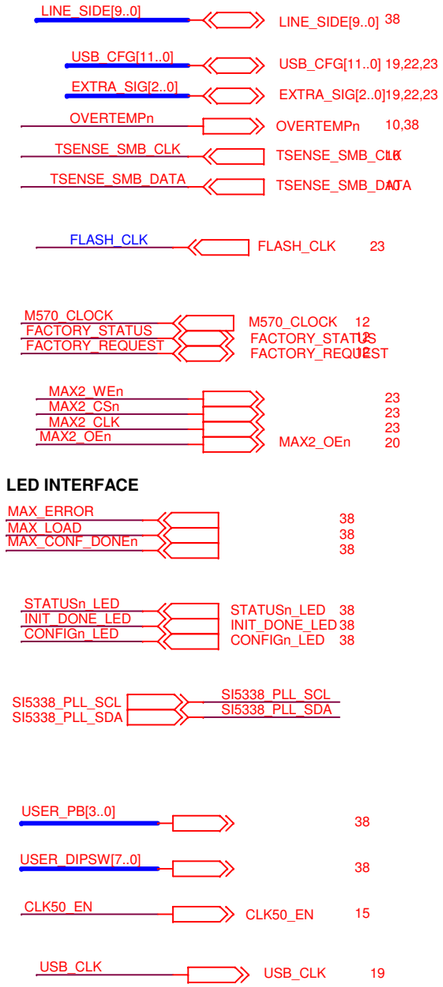
MAX II Banks 3 and 4







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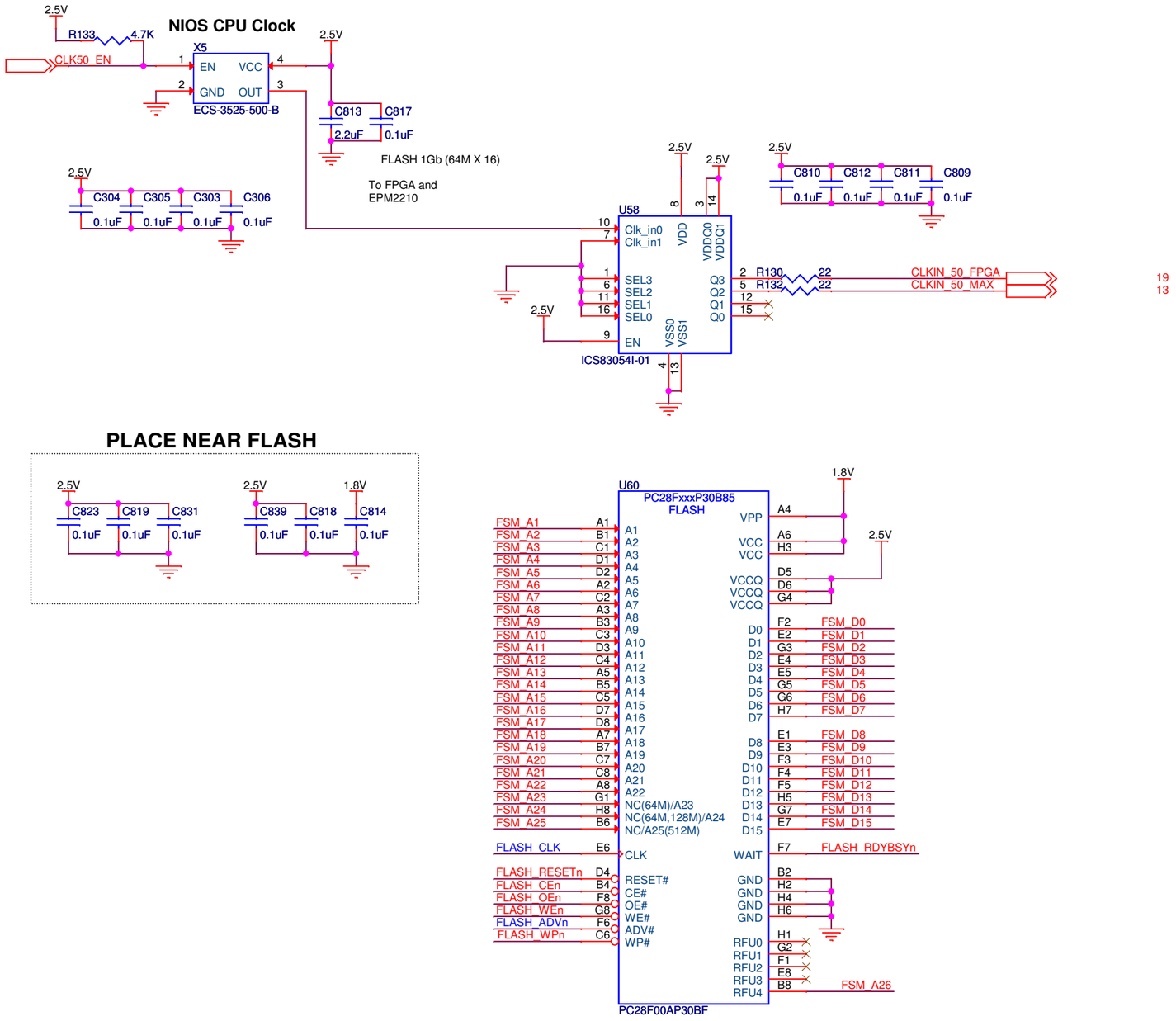
FLASH / SRAM



SHARED BUS

FSM_D[15..0] — FSM_D[15..0] 13,19,20,22,23

FSM_A[26..1] — FSM_A[26..1] 13,19,20,22,23

FLASH INTERFACE

FLASH_RESETn	FLASH_RESETn	13,22
FLASH_WEn	FLASH_WEn	13,23
FLASH_OEn	FLASH_OEn	13,19
FLASH_RDYBSYn	FLASH_RDYBSYn	13,23
FLASH_CEn	FLASH_CEn	13,23
FLASH_ADVn	FLASH_ADVn	13,22
FLASH_CLK	FLASH_CLK	23

2.5V

R434	10K	FLASH_WPn
R433	10K	FLASH_CEn
R426	10K	FLASH_OEn
R421	10K	FLASH_WEn
R428	10K	FLASH_RDYBSYn
R419	DNI	FLASH_CLK

R427	10K	FLASH_RESETn
R316	10K	FLASH_ADVn

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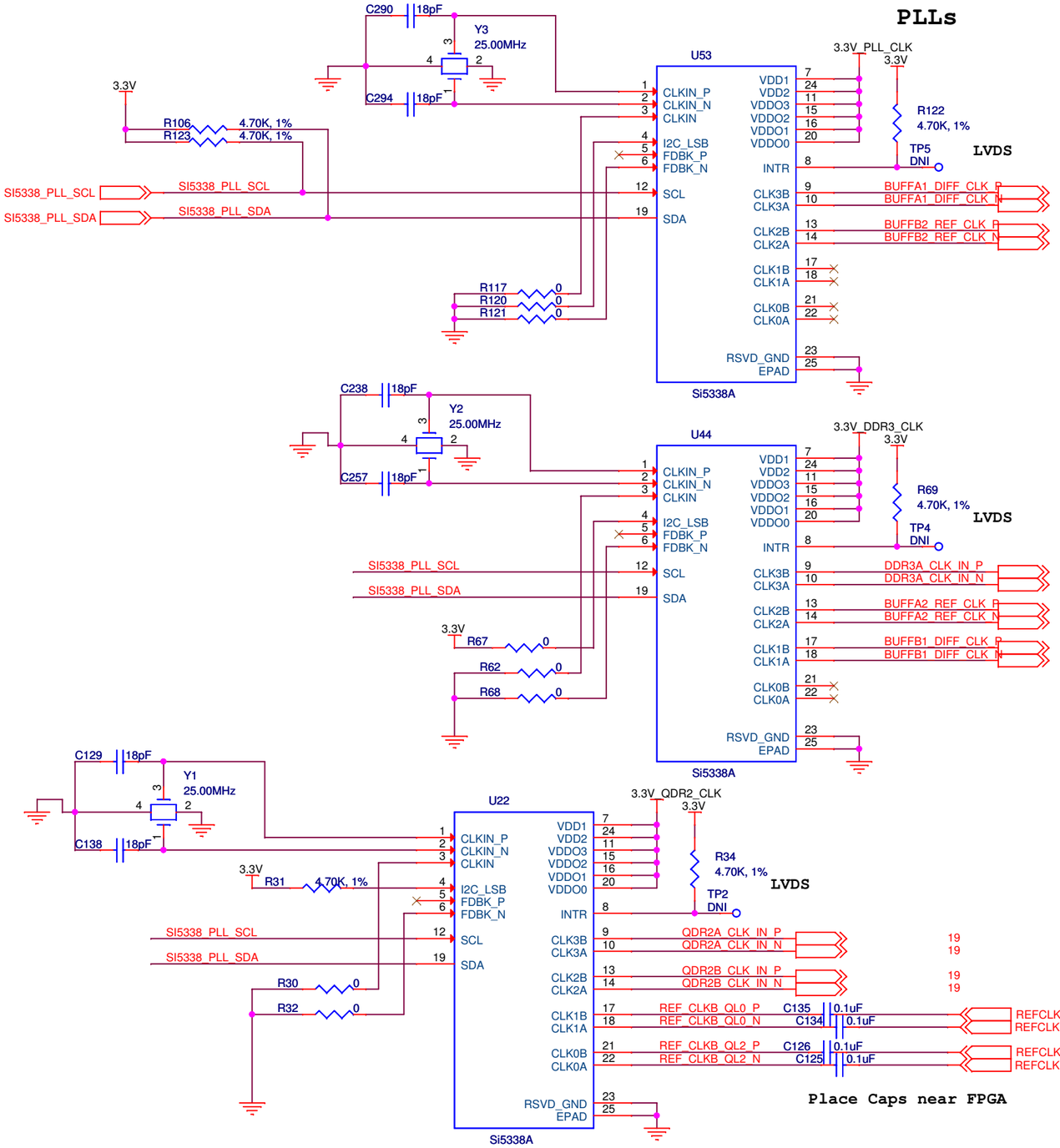
PLLs



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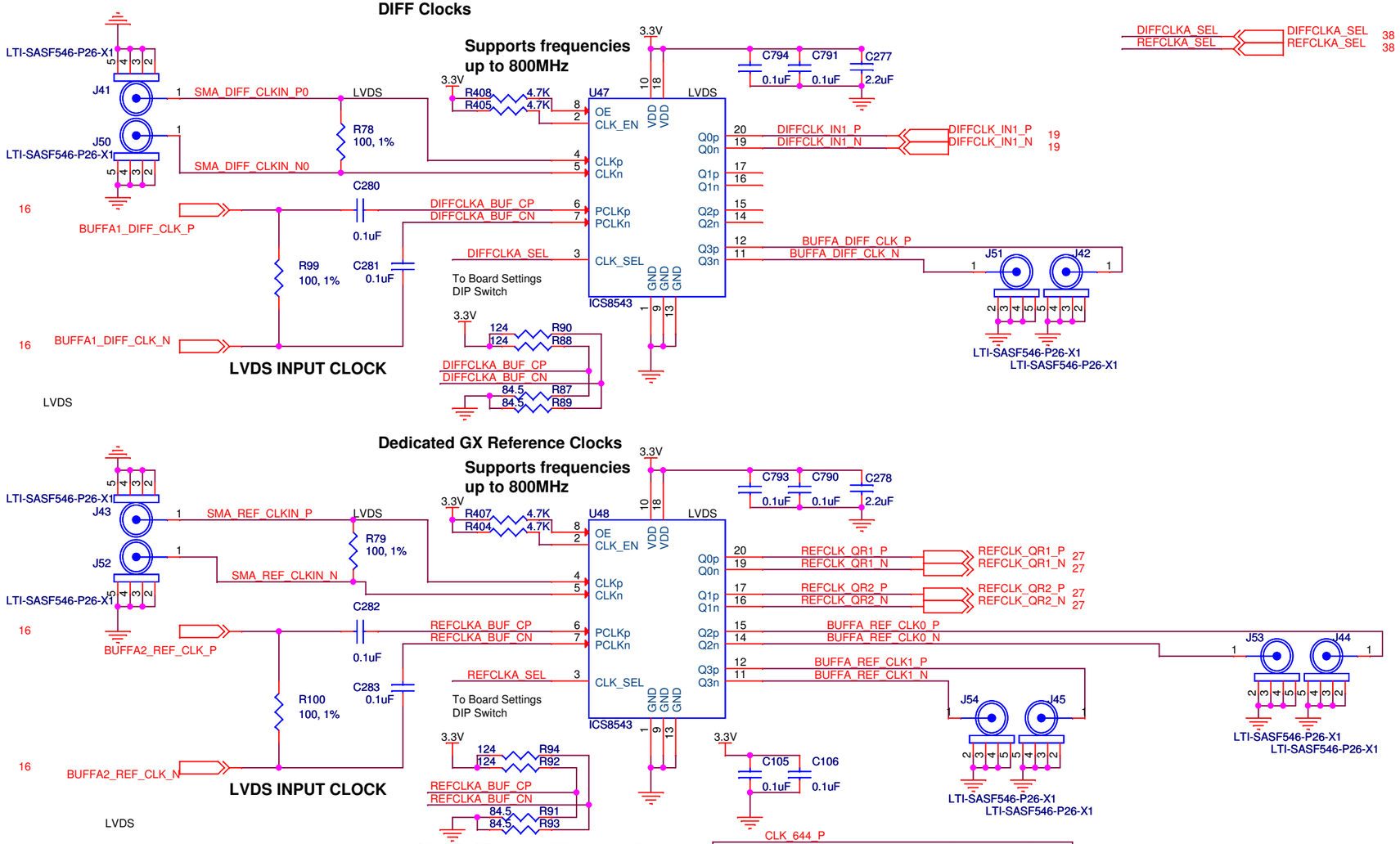
Clock A Circuitry

DIFF Clocks



Dedicated GX Reference Clocks

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Clock B Circuitry

Dedicated GX Reference Clocks

Supports frequencies up to 800MHz

LTI-SASF546-P26-X1 J46 — SMA_DIFF_CLKIN_P1
LTI-SASF546-P26-X1 J55 — SMA_DIFF_CLKIN_N1
LVDS
R80 100, 1%

3.3V
R406 4.7K
R403 4.7K

U49 ICS8543
OE, CLK_EN
CLKp, CLKn
PCLKp, PCLKn
CLK_SEL
VDD, GND

C792 0.1uF, C789 0.1uF, C279 2.2uF

To Buffer

Q0p/Q0n: REFCLK_QR0_P / REFCLK_QR0_N → REFCLK_QR0_P 27 / REFCLK_QR0_N 27
Q1p/Q1n: REFCLK_QR3_P / REFCLK_QR3_N → REFCLK_QR3_P 27 / REFCLK_QR3_N 27
Q2p/Q2n
Q3p/Q3n: BUFFB_CLK_P, BUFFB_CLK_N

C284 0.1uF
DIFFCLKB_BUF_CP
DIFFCLKB_BUF_CN
DIFFCLKB_SEL
To Board Settings DIP Switch
BUFFB1_DIFF_CLK_P
BUFFB1_DIFF_CLK_N
R101 100, 1%
C285 0.1uF

J56, J47 — LTI-SASF546-P26-X1

LVDS INPUT CLOCK

3.3V
124 R98
124 R96
84.5 R95
84.5 R97

LVDS

2.5V
C149 0.1uF, C151 0.1uF, C154 2.2uF

DIFF Clocks

Supports frequencies up to 1GHz

LTI-SASF546-P26-X1 J17 — BUFFB2_REF_CLK_P
LTI-SASF546-P26-X1 J21 — BUFFB2_REF_CLK_N
LVDS
R38 100, 1%
R39 100, 1%

2.5V
R40 4.7K
R37 4.7K
R36 4.7K

U30 IDT5T9306
VDD, GND, NC
Gn, GL, PDn
CLK1p/CLK1n: REFCLK_OSC_P / REFCLK_OSC_N
CLK2p/CLK2n: BUFFB2_REF_CLK_P / BUFFB2_REF_CLK_N
CLK_SEL: REFCLKB_SEL
To Board Settings DIP Switch

Q1p/Q1n: REFCLK_QL0_P / REFCLK_QL0_N → REFCLK_QL0_P 26 / REFCLK_QL0_N 26
Q2p/Q2n: REFCLK_QL3_P / REFCLK_QL3_N → REFCLK_QL3_P 26 / REFCLK_QL3_N 26
Q3p/Q3n: REFCLK_QL2_P / REFCLK_QL2_N → REFCLK_QL2_P 26 / REFCLK_QL2_N 26
Q4p/Q4n: REFCLK_QL1_P / REFCLK_QL1_N → REFCLK_QL1_P 26 / REFCLK_QL1_N 26
Q5p/Q5n: REFCLK_OPTIC_P / REFCLK_OPTIC_N
Q6p/Q6n: REFCLK_QL_P / REFCLK_QL_N

C110 0.1uF, C112 0.1uF, C111 2.2uF
C120 0.1uF, C121 0.1uF

U21 MC100ES6139
MR, CLK_EN
CLKp, CLKn
VBB
DIV_B1, DIV_B0
DIV_A
VCC, VEE

R248 1.00k
R240 1.00k
R249 1.00k
R243 1.00k
R25 1.00k

Q0p/Q0n: OPTIC_CLK_P / OPTIC_CLK_N
Q2p/Q2n: CFP_REFCLK_P / CFP_REFCLK_N → CFP_REFCLK_P 35 / CFP_REFCLK_N 35
Q3p/Q3n

R19 100, 1%
REFCLK_OPTIC_P — REFCLK_OPTIC_N

3.3V
124 R23
124 R22
84.5 R20
84.5 R21
OPTIC_CLK_P
OPTIC_CLK_N

LTI-SASF546-P26-X1 J12 — OPTIC_CLK_P
LTI-SASF546-P26-X1 J15 — OPTIC_CLK_N

3.3V
124 R26
124 R27
84.5 R29
84.5 R28
CFP_REFCLK_P
CFP_REFCLK_N

DIFFCLKB_SEL → DIFFCLKB_SEL 38
REFCLKB_SEL → REFCLKB_SEL 38

2.5V
C148 0.1uF, C150 0.1uF, C147 2.2uF

LTI-SASF546-P26-X1 J11 — REFCLK_QL_P
LTI-SASF546-P26-X1 J14 — REFCLK_QL_N

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Stratix V GX Clocks

23,28,29 — QDR2B_A[20..0]

X2: CLK125_EN (1) → EN; 2.5V (2) → NC; (6) → VCC; OUT (4) → CLKIN_125_P; OUTn (5) → CLKIN_125_N; GND (3); 125.0MHz
C222 0.1uF, C221 10uF

CLKIN_125_N — 100, 1% — R340 — CLKIN_125_P
QDR2A_CLK_IN_P — 100, 1% — R339 — QDR2A_CLK_IN_N
DDR3A_CLK_IN_P — 100, 1% — R296 — DDR3A_CLK_IN_N

From FPGA

VCXOB_UP — R63 4.99K — 1588_CLK_CTL
VCXOB_DN — R64 4.99K
R71 180K
C261 0.001uF
2.5V: C243 0.1uF, C242 0.1uF, C262 0.1uF

2.5V: R59 10.0K, R60 10.0K
U42 SI552_570: 1588_CLK_CTL (1) → VC; CLK_1588_SEL (2) → FS_OE; VCXOB_SDA (7) → NC_SDA; VCXOB_SCL (8) → NC_SCL; (3) GND; VCC (6) ← 2.5V; CLK- (5) → VCXOB_CLK_IN_N; CLK+ (4) → VCXOB_CLK_IN_P

U38E

Stratix V GX Clocks

ENET_RX_CLK	AW35	CLK0p,DIFFIO_RX_B22p,DQS4B/CQ4B	Bank 3B	FPLL_BL_FB/CLKOUTp,DIFFIO_RX_B26p,DQ5B/CQn5B	AR31	QSFP0_MOD_PRSn
SFP2_TXFAULT	AY36	CLK0n,DIFFIO_RX_B22n,DQSn4B/DQ4B		FPLL_BL_FB/CLKOUTn,DIFFIO_RX_B26n,DQ5B	AR32	INT_LSB_CON_TX_FC_SYNC
DIFFCLK_IN1_P	AY34	CLK1p,DIFFIO_RX_B24p,DQ4B		FPLL_BL_CLKOUTp,DIFFIO_TX_B25p,DQ5B	AV34	SFP0_MOD2_SDA
DIFFCLK_IN1_N	BA34	CLK1n,DIFFIO_RX_B24n,DQ4B		FPLL_BL_CLKOUTn,DIFFIO_TX_B25n,DQ5B	AW33	QSFP1_SCL
FSM_D2	AY33	CLK2p,DIFFIO_RX_B28p,DQS5B/CQ5B				
SFP1_MOD0_PRSNTn	BA33	CLK2n,DIFFIO_RX_B28n,DQSn5B/DQ5B				
VCXOB_CLK_IN_P	BB33	CLK3p,DIFFIO_RX_B30p,DQ5B				
VCXOB_CLK_IN_N	BC34	CLK3n,DIFFIO_RX_B30n,DQ5B				
QDR2A_Q18	BD28	CLK4n,DIFFIO_RX_B76n,DQSn13B/DQ13B	Bank 3D			
QDR2A_CQ_N	BC28	CLK4p,DIFFIO_RX_B76p,DQS13B/CQ13B				
QDR2A_CLK_IN_N	BB27	CLK5n,DIFFIO_RX_B78n,DQ13B				
QDR2A_CLK_IN_P	BA27	CLK5p,DIFFIO_RX_B78p,DQ13B				
CLKIN_125_P	AY18	CLK6p,DIFFIO_RX_B142p,DQS24B/CQ24B	Bank 4D	FPLL_BC_FB/CLKOUTp,DIFFIO_RX_B140p,DQ24B/CQn24B	BC19	
CLKIN_125_N	BA18	CLK6n,DIFFIO_RX_B142n,DQSn24B/DQ24B		FPLL_BC_FB/CLKOUTn,DIFFIO_RX_B140n,DQ24B	BD19	USB_DATA6
	BB18	CLK7p,DIFFIO_RX_B144p,DQ24B		FPLL_BC_CLKOUTp,DIFFIO_TX_B139p,DQ24B	AY19	FPGA_USER_LED7
	BB17	CLK7n,DIFFIO_RX_B144n,DQ24B		FPLL_BC_CLKOUTn,DIFFIO_TX_B139n,DQ24B	BA19	USB_DATA1
QDR2B_CLK_IN_P	BC8	CLK11p,DIFFIO_RX_B200p,DQ34B/CQn34B	Bank 4A	FPLL_BR_FB/CLKOUTn,DIFFIO_RX_B204n,DQ34B	AU8	QSFP0_SCL
QDR2B_CLK_IN_N	BD8	CLK11n,DIFFIO_RX_B200n,DQ34B		FPLL_BR_FB/CLKOUTp,DIFFIO_RX_B204p,DQ34B	AT9	SFP0_RATESEL
CLKIN_50_FPGA	AY9	CLK10p,DIFFIO_RX_B202p,DQS34B/CQ34B		FPLL_BR_CLKOUTn,DIFFIO_TX_B203n,DQ34B	AW9	FSM_A16
SFP0_TXFAULT	BA9	CLK10n,DIFFIO_RX_B202n,DQSn34B/DQ34B		FPLL_BR_CLKOUTp,DIFFIO_TX_B203p,DQ34B	AV8	FLASH_OEn
USB_CLK	AP10	CLK8p,DIFFIO_RX_B208p,DQS35B/CQ35B				
FSM_A1	AR10	CLK8n,DIFFIO_RX_B208n,DQSn35B/DQ35B				
FSM_A8	AR11	CLK9p,DIFFIO_RX_B206p,DQ35B/CQn35B				
FSM_A12	AT11	CLK9n,DIFFIO_RX_B206n,DQ35B				
DDR3A_RASn	B8	CLK15p,DIFFIO_RX_T11p,DQ2T/CQn2T	Bank 7A			
DDR3A_CASn	A8	CLK15n,DIFFIO_RX_T11n,DQ2T				
DDR3B_CK_P	E8	CLK14p,DIFFIO_RX_T9p,DQS2T/CQ2T		FPLL_TR_FB/CLKOUTp,DIFFIO_RX_T7p,DQ2T	G8	DDR3A_A1
DDR3B_CK_N	D9	CLK14n,DIFFIO_RX_T9n,DQSn2T/DQ2T		FPLL_TR_FB/CLKOUTn,DIFFIO_RX_T7n,DQ2T	F8	DDR3A_BA0
DDR3A_CSn	M9	CLK13p,DIFFIO_RX_T5p,DQ1T/CQn1T		FPLL_TR_CLKOUTp,DIFFIO_TX_T8p,DQ2T	F9	DDR3A_A3
DDR3A_BA1	L9	CLK13n,DIFFIO_RX_T5n,DQ1T		FPLL_TR_CLKOUTn,DIFFIO_TX_T8n,DQ2T	E9	DDR3A_BA2
DDR3A_CK_P	M8	CLK12p,DIFFIO_RX_T3p,DQS1T/CQ1T				
DDR3A_CK_N	L8	CLK12n,DIFFIO_RX_T3n,DQSn1T/DQ1T				
DDR3C_DQS_P1	J18	CLK18p,DIFFIO_RX_T69p,DQS12T/CQ12T	Bank 7D	FPLL_TC_FB/CLKOUTp,DIFFIO_RX_T71p,DQ12T/CQn12T	E17	DDR3C_DQ10
DDR3C_DQS_N1	H18	CLK18n,DIFFIO_RX_T69n,DQSn12T/DQ12T		FPLL_TC_FB/CLKOUTn,DIFFIO_RX_T71n,DQ12T	D17	DDR3C_DQ14
DDR3A_CLK_IN_P	G16	CLK19p,DIFFIO_RX_T67p,DQ12T		FPLL_TC_CLKOUTp,DIFFIO_TX_T72p,DQ12T	B16	DDR3C_DQ13
DDR3A_CLK_IN_N	F16	CLK19n,DIFFIO_RX_T67n,DQ12T		FPLL_TC_CLKOUTn,DIFFIO_TX_T72n,DQ12T	A16	DDR3C_DQ12
DDR3D_DQS_P2	R25	CLK16p,DIFFIO_RX_T135p,DQS23T/CQ23T	Bank 8D			
DDR3D_DQS_N2	P25	CLK16n,DIFFIO_RX_T135n,DQSn23T/DQ23T				
DDR3D_DQ20	N25	CLK17p,DIFFIO_RX_T133p,DQ23T				
DDR3D_DQ23	M25	CLK17n,DIFFIO_RX_T133n,DQ23T				
DDR3F_A4	R36	CLK20p,DIFFIO_RX_T201p,DQS34T/CQ34T	Bank 8A			
DDR3F_A9	P37	CLK20n,DIFFIO_RX_T201n,DQSn34T/DQ34T		FPLL_TL_FB/CLKOUTp,DIFFIO_RX_T197p,DQ33T/CQn33T	J37	DDR3F_CK_P
DDR3F_BA0	U36	CLK21p,DIFFIO_RX_T199p,DQ34T		FPLL_TL_FB/CLKOUTn,DIFFIO_RX_T197n,DQ33T	H37	DDR3F_CK_N
DDR3F_A13	T36	CLK21n,DIFFIO_RX_T199n,DQ34T				
DDR3F_A12	B39	CLK22p,DIFFIO_RX_T195p,DQS33T/CQ33T		FPLL_TL_CLKOUTp,DIFFIO_TX_T198p,DQ33T	G37	DDR3F_A6
DDR3F_CSn	A38	CLK22n,DIFFIO_RX_T195n,DQSn33T/DQ33T		FPLL_TL_CLKOUTn,DIFFIO_TX_T198n,DQ33T	F36	DDR3F_A0
DDR3F_ODT	B37	CLK23p,DIFFIO_RX_T193p,DQ33T				
DDR3F_A10	A37	CLK23n,DIFFIO_RX_T193n,DQ33T				

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QDR2A_Q18 ↔ QDR2A_Q18 28
QDR2A_CQ_N ↔ QDR2A_CQ_N 28
SFP0_RATESEL ↔ 34
QDR2A_CLK_IN_P, QDR2A_CLK_IN_N ↔ 16, 16
QDR2B_CLK_IN_P, QDR2B_CLK_IN_N ↔ 16, 16
SFP2_TXFAULT ↔ SFP2_TXFAULT 34
SFP1_MOD0_PRSNTn ↔ SFP1_MOD0_PRSNTn 34
SFP0_MOD2_SDA ↔ SFP0_MOD2_SDA 34
SFP0_TXFAULT ↔ SFP0_TXFAULT 34
QSFP1_SCL ↔ QSFP1_SCL 33
QSFP0_MOD_PRSn ↔ QSFP0_MOD_PRSn 33
INT_LSB_CON_TX_FC_SYNC ↔ INT_LSB_CON_TX_FC_SYNC 37
DIFFCLK_IN1_P, DIFFCLK_IN1_N ↔ 17, 17
CLKIN_50_FPGA ↔ CLKIN_50_FPGA 15
QSFP0_SCL ↔ QSFP0_SCL 33
ENET_RX_CLK ↔ ENET_RX_CLK 36
FSM_D2 ↔ FSM_D2 13,15
FLASH_OEn ↔ FLASH_OEn 13,15
FSM_A[26..1] ↔ FSM_A[26..1] 13,15,20,22,23
USB_DATA[7..0] ↔ USB_DATA[7..0] 12,22,23
USB_CLK ↔ USB_CLK 12
FPGA_USER_LED7 ↔ FPGA_USER_LED7 38
DDR3A_RASn ↔ DDR3A_RASn 30
DDR3A_CASn ↔ DDR3A_CASn 30
DDR3A_A[13..0] ↔ 24,30
DDR3F_A[13..0] ↔ 25,32
DDR3B_A[13..0] ↔ 24,30
DDR3A_BA[2..0] ↔ 24,30
DDR3F_CSN ↔ DDR3F_CSN 32
DDR3F_BA[2..0] ↔ 25,32
DDR3F_CK_P, DDR3F_CK_N ↔ 32, 32
DDR3B_CK_P, DDR3B_CK_N ↔ 30, 30
DDR3A_CK_P, DDR3A_CK_N ↔ 30, 30
DDR3C_DQS_P1, DDR3C_DQS_N1 ↔ 31, 31
DDR3D_DQ[31..0] ↔ 25,31
DDR3C_DQ[31..0] ↔ 24,31
DDR3A_CSn ↔ DDR3A_CSn 30
DDR3A_CLK_IN_P, DDR3A_CLK_IN_N ↔ 16, 16
DDR3D_DQS_P2, DDR3D_DQS_N2 ↔ 31, 31
DDR3F_ODT ↔ DDR3F_ODT 32

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Stratix V GX Configuration

U38P — Stratix V GX Power

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J17			V8
J20	GND513	GND565	W10
J23	GND514	GND566	W11
J26	GND515	GND567	W12
J29	GND516	GND568	W13
J32	GND517	GND569	W15
J35	GND518	GND570	W19
J38	GND519	GND571	W21
J7	GND520	GND572	W23
J8	GND521	GND573	W25
K38	GND522	GND574	W27
K7	GND523	GND575	W30
L10	GND524	GND576	W33
L13	GND525	GND577	W36
L16	GND526	GND578	W9
L19	GND527	GND579	Y10
L22	GND528	GND580	Y11
L25	GND529	GND581	Y12
L28	GND530	GND582	Y13
L31	GND531	GND583	Y14
L34	GND532	GND584	Y15
L37	GND533	GND585	Y18
L38	GND534	GND586	Y22
L7	GND535	GND587	Y26
M40	GND536	GND588	Y31
M5	GND537	GND589	Y33
M6	GND538	GND590	Y34
N12	GND539	GND591	Y35
N15	GND540	GND592	Y36
N18	GND541	GND593	Y9
N21	GND542	GND594	AD24
N24	GND543	GND595	V37
N27	GND544	GND596	U8
N30	GND545	GND597	U37
N33	GND546	GND598	U34
N36	GND547	GND599	U31
N39	GND548	GND600	U28
N40	GND549	GND601	U25
N5	GND550	GND602	U22
N6	GND551	GND603	U19
N9	GND552	GND604	U16
P40	GND553	GND605	U13
P5	GND554	GND606	U10
P9	GND555	GND607	T8
R11	GND556	GND608	T37
R14	GND557	GND609	R9
R17	GND558	GND610	R8
R20	GND559	GND611	R6
R23	GND560	GND612	R5
R26	GND561	GND613	R40
R29	GND562	GND614	R39
R32	GND563	GND615	R37
	GND564	GND616	R35
		GND617	

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AP38	GND385	GND449 BC4
AP40	GND386	GND450 BC40
AP5	GND387	GND451 BC41
AP7	GND388	GND452 BC5
AP8	GND389	GND453 BC6
AR38	GND390	GND454 BD12
AR7	GND391	GND455 BD15
AT10	GND392	GND456 BD18
AT13	GND393	GND457 BD21
AT16	GND394	GND458 BD24
AT19	GND395	GND459 BD27
AT22	GND396	GND460 BD30
AT25	GND397	GND461 BD33
AT28	GND398	GND462 BD36
AT31	GND399	GND463 BD39
AT34	GND400	GND464 BD40
AT37	GND401	GND465 BD5
AT38	GND402	GND466 BD6
AT7	GND403	GND467 BD9
AU38	GND404	GND468 C11
AU7	GND405	GND469 C14
AV12	GND406	GND470 C17
AV15	GND407	GND471 C20
AV18	GND408	GND472 C23
AV21	GND409	GND473 C26
AV24	GND410	GND474 C29
AV27	GND411	GND475 C32
AV30	GND412	GND476 C35
AV33	GND413	GND477 C38
AV36	GND414	GND478 C7
AV38	GND415	GND479 C8
AV7	GND416	GND480 D38
AV9	GND417	GND481 D7
AW38	GND418	GND482 D8
AW7	GND419	GND483 E10
AW8	GND420	GND484 E13
AY11	GND421	GND485 E16
AY14	GND422	GND486 E19
AY17	GND423	GND487 E22
AY20	GND424	GND488 E25
AY23	GND425	GND489 E28
AY26	GND426	GND490 E31
AY29	GND427	GND491 E34
AY32	GND428	GND492 E37
AY35	GND429	GND493 E38
AY38	GND430	GND494 E7
AY7	GND431	GND495 F38
AY8	GND432	GND496 F7
B6	GND433	GND497 G12
BA38	GND434	GND498 G15
BA7	GND435	GND499 G18
BA8	GND436	GND500 G21
BB10	GND437	GND501 G24
BB13	GND438	GND502 G27
BB16	GND439	GND503 G30
BB19	GND440	GND504 G33
BB22	GND441	GND505 G36
BB25	GND442	GND506 G38
BB28	GND443	GND507 G7
BB31	GND444	GND508 G9
BB34	GND445	GND509 H38
BB37	GND446	GND510 H7
BB6	GND447	GND511 J11
BB7	GND448	GND512 J14

TP19 FPGA_DATA0
TP18 FPGA_DATA1
TP17 FPGA_DATA2
TP16 FPGA_DATA3
TP15 FPGA_DATA4
TP14 FPGA_DATA5
TP13 FPGA_DATA6
TP12 FPGA_DATA7
TP8 FPGA_STATUSn
TP9 FPGA_CONFIGn
TP10 FPGA_CONF_DONE
TP11 FPGA_DCLK

2.5V — 10.0K — R56

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FPGA_JTAG_TMS	AL37	TMS
FPGA_JTAG_TCK	AL34	TCK
JTAG_BLASTER_TDI	AM37	TDI
FPGA_JTAG_TDO	AL36	TDO
FPGA_JTAG_TRST	AG37	TRST
FPGA_DATA0	BB38	DATA0,DIFFIO_RX_B4p,DQS1B/CQ1B
FPGA_DATA1	BD38	DATA1,DIFFIO_TX_B5n,DQ1B
FPGA_DATA2	BC39	DATA2,DIFFIO_TX_B5p,DQ1B
FPGA_DATA3	BD37	DATA3,DIFFIO_RX_B6n,DQ1B
FPGA_DATA4	BC38	DATA4,DIFFIO_RX_B6p,DQ1B
FPGA_DATA5	AR37	DATA5,DIFFIO_TX_B7n,DQ2B
FPGA_DATA6	AP37	DATA6,DIFFIO_TX_B7p,DQ2B
FPGA_DATA7	AN39	DATA7,DIFFIO_RX_B8n,DQ2B
ENET_MDC	AP39	DATA8,DIFFIO_RX_B8p,DQ2B/CQn2B
FSM_D12	AN38	DATA9,DIFFIO_TX_B9n,DQ2B
FSM_A4	AN37	DATA10,DIFFIO_TX_B9p,DQ2B
ENET_MDIO	AR36	DATA11,DIFFIO_RX_B10n,DQSn2B/DQ2B
SFP1_RATESEL	AR35	DATA12,DIFFIO_RX_B10p,DQS2B/CQ2B
FSM_A17	AT36	DATA13,DIFFIO_TX_B11n,DQ2B
SMA_IN	AT35	DATA14,DIFFIO_TX_B11p,DQ2B
SMA_OUT	AU37	DATA15,DIFFIO_RX_B12n,DQ2B
SFP1_TXDISABLE	AU36	DATA16,DIFFIO_RX_B12p,DQ2B
SFP0_RS1	AP34	DATA17,DIFFIO_TX_B13n,DQ3B
ENET_RX_DV	AN34	DATA18,DIFFIO_TX_B13p,DQ3B
ENET_TX_EN	AP36	DATA19,DIFFIO_RX_B14n,DQ3B
FSM_A15	AN36	DATA20,DIFFIO_RX_B14p,DQ3B/CQn3B
INT_LSB_CON_RX_FC_DATA	AL35	DATA21,DIFFIO_TX_B15n,DQ3B
QSFP0_SDA	AK35	DATA22,DIFFIO_TX_B15p,DQ3B
CFP_PRG_ALRM1	AG34	DATA23,DIFFIO_RX_B16n,DQSn3B/DQ3B
FPGA_USER_DIPSW7	AF35	DATA24,DIFFIO_RX_B16p,DQS3B/CQ3B
FSM_A7	AJ34	DATA25,DIFFIO_TX_B17n,DQ3B
CFP_MOD_RST	AH34	DATA26,DIFFIO_TX_B17p,DQ3B
INT_MSB_CON_TX_FC_DATA	AE36	DATA27,DIFFIO_RX_B18n,DQ3B
	AE35	DATA28,DIFFIO_RX_B18p,DQ3B
SFP1_MOD2_SDA	AR33	DATA29,DIFFIO_TX_B19n,DQ4B
INT_LSB_CON_TX_FC_DATA	AR34	DATA30,DIFFIO_TX_B19p,DQ4B
INT_MSB_CON_RX_FC_CK	AU35	DATA31,DIFFIO_RX_B20n,DQ4B
FSM_D15	BB36	INIT_DONE,DIFFIO_TX_B3p,DQ1B
FPGA_CONFIGn	AM38	nCONFIG
FPGA_CONF_DONE	AH9	CONF_DONE
FPGA_DCLK	AG36	DCLK
FPGA_STATUSn	AL8	nSTATUS
FPGA_CEn	AP6	nCE

Bank 3A

CRC_ERROR,DIFFIO_TX_B1p,DQ1B	AV37	FSM_D4
CLKUSR,DIFFIO_TX_B1n,DQ1B	AW37	CFP_MOD_LOPWR
	AH36	
AS_DATA0,ASDO	AJ36	
AS_DATA1	AJ35	
AS_DATA2	AK36	
AS_DATA3		
nCSO	AG35	

Bank 3B

CvPCIe_CONFDONE,DIFFIO_TX_B23p,DQ4B	BB35	SFP0_MOD1_SCL
PR_DONE,DIFFIO_RX_B20p,DQ4B/CQn4B	AU34	
PR_REQUEST,DIFFIO_TX_B21n,DQ4B	AW36	FSM_A25
PR_READY,DIFFIO_TX_B21p,DQ4B	AV35	FSM_D5
PR_ERROR,DIFFIO_TX_B23n,DQ4B	BC35	QSFP0_RST
nPERSTL0,DIFFIO_TX_B27n,DQ5B	AU33	VCXOB_SCL
nPERSTL1,DIFFIO_TX_B27p,DQ5B	AT33	FSM_D10
nPERSTR0,DIFFIO_TX_B29p,DQ5B	BD34	FSM_A9
nPERSTR1,DIFFIO_TX_B29n,DQ5B	BD35	FSM_D3

Bank 4A

MSEL0	AM5	FPGA_MSEL0
MSEL1	AM8	FPGA_MSEL1
MSEL2	AM7	FPGA_MSEL2
MSEL3	AJ9	FPGA_MSEL3
MSEL4	AN8	FPGA_MSEL4
nIO_PULLUP	AN7	FPGA_NIO_PULLUP

Bank 3B

DEV_CLRn,DIFFIO_TX_B3n,DQ1B	BC37	SFP2_RS1
DEV_OE,DIFFIO_RX_B2p,DQ1B/CQn1B	AY37	MAX2_OEn

Bank 3A

nCEO,DIFFIO_RX_B4n,DQSn1B/DQ1B	BB39	LCD_DATA0

2.5V — R54 0 — R53 DNI

FPGA_STATUSn — FPGA_CEn — R325 10.0K — TP3

USB Blaster Programming Header
(uses JTAG mode only)

2.5V — USB_DISABLEn — J59 — 70247-1051

2	4	1	FPGA_JTAG_TCK
4	6	3	JTAG_BLASTER_TDI
6	8	5	FPGA_JTAG_TMS
8	10	7	JTAG_BLASTER_TDO
10		9	

J26 — LTI-SASF546-P26-X1 — 1 SMA_OUT
J24 — LTI-SASF546-P26-X1 — 1 SMA_IN

Logic 0 = pin 6 <--> pin 7 (5M2210 Bypass)
Logic 1 = pin 6 <--> pin 4 (5M2210 Enable)

2.5V — FPGA_JTAG_TMS — 10.0K — R129
JTAG_BLASTER_TDO — 10.0K — R57

FPGA_JTAG_TCK — R148 DNI — C308 DNI
R146 1.00k

U57 — TS5A23157

MAX_JTAG_EN	1	IN1	COM1 10 JTAG_BLASTER_TDI
13,20 JTAG_MAX_TDO	2	NO1	NC1 9 JTAG_FPGA_TDO_RETIMER
	3	GND	V+ 8 2.5V — C808 0.1uF
FPGA_JTAG_TMS	4	NO2	NC2 7 R420 1.00K — 2.5V
MAX_JTAG_EN	5	IN2	COM2 6 MAX_JTAG_TMS 13

J62 CON2 — MAX_JTAG_EN — R131 — 1.00k — 2.5V

2.5V
10.0K R418 FPGA_STATUSn
10.0K R417 FPGA_CONFIGn
10.0K R55 FPGA_CONF_DONE

FSM_A[26..1] — FSM_A[26..1] 13,15,19,22,23
FSM_D[15..0] — FSM_D[15..0] 13,15,19,22,23

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FPGA_DCLK — FPGA_DCLK 13
FPGA_STATUSn — FPGA_STATUSn 13
FPGA_CONFIGn — FPGA_CONFIGn 13
FPGA_CONF_DONE — FPGA_CONF_DONE 13

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8 bit FPP Mode

SW2 — TDA06H0SB1 — OPEN

1	12	FPGA_MSEL0	R380 10.0K — 2.5V
2	11	FPGA_MSEL1	R379 10.0K
3	10	FPGA_MSEL2	R378 10.0K
4	9	FPGA_MSEL3	R377 10.0K
5	8	FPGA_MSEL4	R376 10.0K
6	7		

FPGA_JTAG_TDO — FPGA_JTAG_TDO 12,13,20
JTAG_FPGA_TDO_RETIMER — 12

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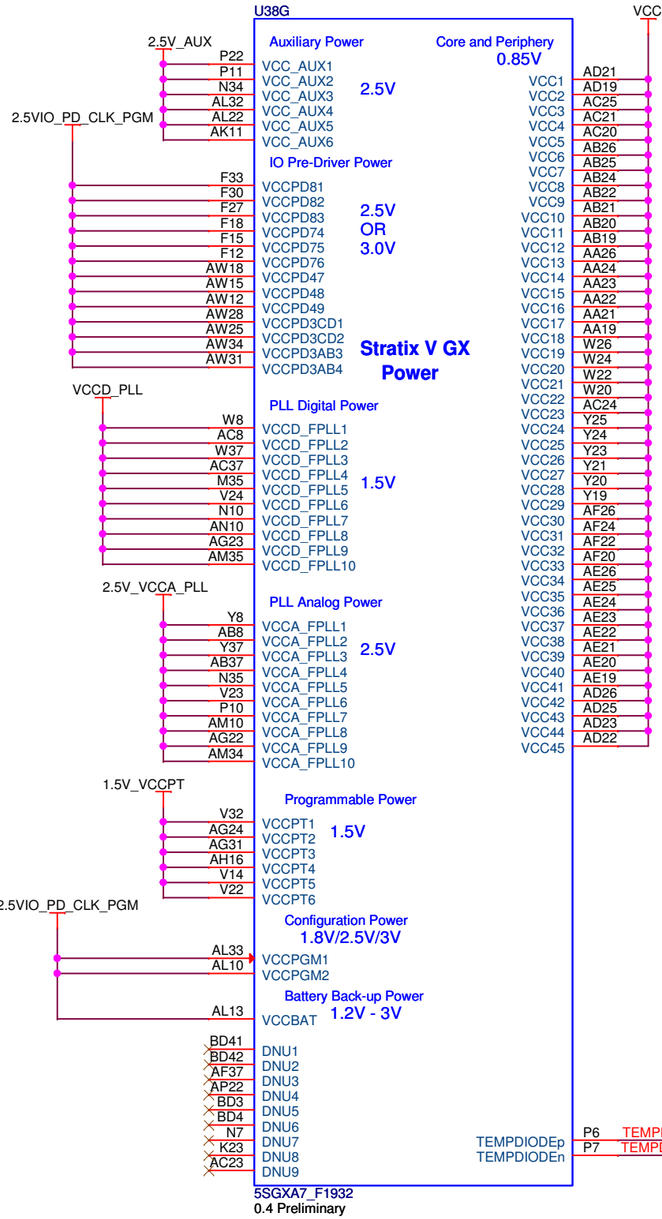

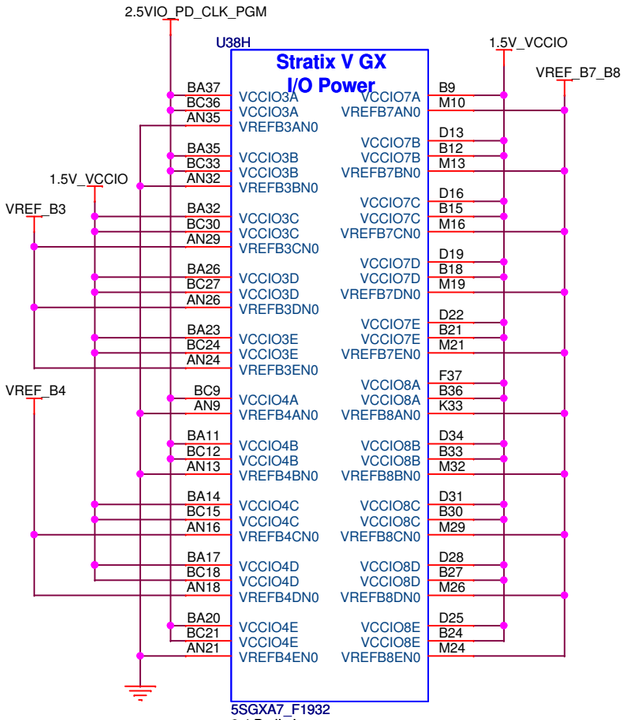

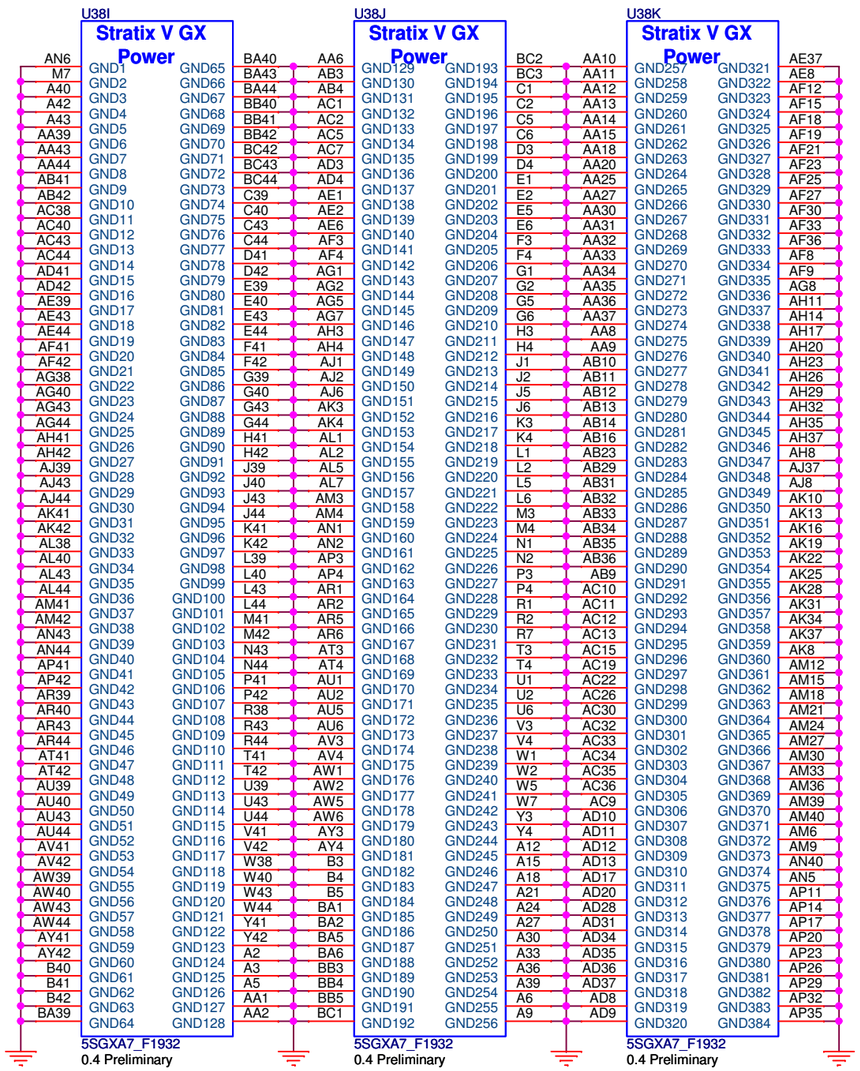

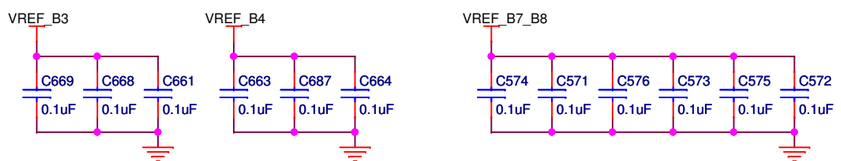

TEMP SENSE SIGNALS

TEMPDIODE_P → TEMPDIODE_P 10
TEMPDIODE_N → TEMPDIODE_N 10

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THESE OFF-PAGE CONNECTORS NEED TO CHANGE

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Stratix V GX Bank 3

Bank 3A

RZQ_0,DIFFIO_RX_B2n,DQ1B

Bank 3B

DIFFIO_TX_B31p,DQ6B
DIFFIO_TX_B31n,DQ6B
DIFFIO_RX_B32p,DQ6B/CQn6B
DIFFIO_RX_B32n,DQ6B
DIFFIO_TX_B33p,DQ6B
DIFFIO_TX_B33n,DQ6B
DIFFIO_RX_B34p,DQS6B/CQ6B
DIFFIO_RX_B34n,DQSn6B/DQ6B
DIFFIO_TX_B35p,DQ6B
DIFFIO_TX_B35n,DQ6B
DIFFIO_RX_B36p,DQ6B
DIFFIO_RX_B36n,DQ6B
DIFFIO_TX_B37p,DQ7B
DIFFIO_TX_B37n,DQ7B

Bank 3C

1.5V

DIFFIO_RX_B54p,DQ9B
DIFFIO_RX_B54n,DQ9B
DIFFIO_TX_B55p,DQ10B
DIFFIO_TX_B55n,DQ10B
DIFFIO_RX_B56p,DQ10B/CQn10B
DIFFIO_RX_B56n,DQ10B
DIFFIO_TX_B57p,DQ10B
DIFFIO_TX_B57n,DQ10B
DIFFIO_RX_B58p,DQS10B/CQ10B
DIFFIO_RX_B58n,DQSn10B/DQ10B
DIFFIO_TX_B59p,DQ10B
DIFFIO_TX_B59n,DQ10B
DIFFIO_RX_B60p,DQ10B
DIFFIO_RX_B60n,DQ10B
DIFFIO_TX_B61p,DQ11B
DIFFIO_TX_B61n,DQ11B
DIFFIO_RX_B62p,DQ11B/CQn11B
DIFFIO_RX_B62n,DQ11B
DIFFIO_TX_B63p,DQ11B
DIFFIO_TX_B63n,DQ11B
DIFFIO_RX_B64p,DQS11B/CQ11B
DIFFIO_RX_B64n,DQSn11B/DQ11B
DIFFIO_TX_B65p,DQ11B
DIFFIO_TX_B65n,DQ11B
DIFFIO_RX_B66p,DQ11B
DIFFIO_RX_B66n,DQ11B

DIFFIO_TX_B53p,DQ9B
DIFFIO_TX_B53n,DQ9B
DIFFIO_RX_B52p,DQS9B/CQ9B
DIFFIO_RX_B52n,DQSn9B/DQ9B
DIFFIO_TX_B51p,DQ9B
DIFFIO_TX_B51n,DQ9B
DIFFIO_RX_B50p,DQ9B/CQn9B
DIFFIO_RX_B50n,DQ9B
DIFFIO_TX_B49p,DQ9B
DIFFIO_TX_B49n,DQ9B
DIFFIO_RX_B48p,DQ8B
DIFFIO_RX_B48n,DQ8B
DIFFIO_TX_B47p,DQ8B
DIFFIO_TX_B47n,DQ8B
DIFFIO_RX_B46p,DQS8B/CQ8B
DIFFIO_RX_B46n,DQSn8B/DQ8B
DIFFIO_TX_B45p,DQ8B
DIFFIO_TX_B45n,DQ8B
DIFFIO_RX_B44p,DQ8B/CQn8B
DIFFIO_RX_B44n,DQ8B
DIFFIO_TX_B43p,DQ8B
DIFFIO_TX_B43n,DQ8B

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Stratix V GX Bank 3

Bank 3D

1.5V

DIFFIO_TX_B67p,DQ12B
DIFFIO_TX_B67n,DQ12B
DIFFIO_RX_B68p,DQ12B/CQn12B
DIFFIO_RX_B68n,DQ12B
DIFFIO_TX_B69p,DQ12B
DIFFIO_TX_B69n,DQ12B
DIFFIO_TX_B89p,DQ15B
DIFFIO_TX_B89n,DQ15B
DIFFIO_RX_B88p,DQS15B/CQ15B
DIFFIO_RX_B88n,DQSn15B/DQ15B
DIFFIO_TX_B87p,DQ15B
DIFFIO_TX_B87n,DQ15B
DIFFIO_RX_B86p,DQ15B/CQn15B
DIFFIO_RX_B86n,DQ15B
DIFFIO_TX_B85p,DQ15B
DIFFIO_TX_B85n,DQ15B
DIFFIO_TX_B84p,DQ14B
DIFFIO_RX_B84n,DQ14B
DIFFIO_TX_B83p,DQ14B
DIFFIO_TX_B83n,DQ14B
DIFFIO_RX_B82p,DQS14B/CQ14B
DIFFIO_RX_B82n,DQSn14B/DQ14B

DIFFIO_RX_B90p,DQ15B
DIFFIO_RX_B90n,DQ15B
DIFFIO_RX_B70p,DQS12B/CQ12B
DIFFIO_RX_B70n,DQSn12B/DQ12B
DIFFIO_TX_B71p,DQ12B
DIFFIO_TX_B71n,DQ12B
DIFFIO_RX_B72p,DQ12B
DIFFIO_RX_B72n,DQ12B
DIFFIO_TX_B73p,DQ13B
DIFFIO_TX_B73n,DQ13B
DIFFIO_RX_B74p,DQ13B/CQn13B
DIFFIO_RX_B74n,DQ13B
DIFFIO_TX_B75p,DQ13B
DIFFIO_TX_B75n,DQ13B
DIFFIO_TX_B77p,DQ13B
DIFFIO_TX_B77n,DQ13B
DIFFIO_TX_B79p,DQ14B
DIFFIO_TX_B79n,DQ14B
DIFFIO_RX_B80p,DQ14B/CQn14B
DIFFIO_TX_B81p,DQ14B
DIFFIO_TX_B81n,DQ14B

Bank 3E

1.5V

DIFFIO_RX_B108p,DQ18B
DIFFIO_RX_B108n,DQ18B
DIFFIO_TX_B107p,DQ18B
DIFFIO_TX_B107n,DQ18B
DIFFIO_RX_B106p,DQS18B/CQ18B
DIFFIO_RX_B106n,DQSn18B/DQ18B
DIFFIO_TX_B105p,DQ18B
DIFFIO_TX_B105n,DQ18B
DIFFIO_RX_B104p,DQ18B/CQn18B
DIFFIO_RX_B104n,DQ18B
DIFFIO_TX_B103p,DQ18B
DIFFIO_TX_B103n,DQ18B
DIFFIO_RX_B102p,DQ17B
DIFFIO_RX_B102n,DQ17B
DIFFIO_TX_B101p,DQ17B
DIFFIO_TX_B101n,DQ17B
DIFFIO_RX_B100p,DQS17B/CQ17B
DIFFIO_RX_B100n,DQSn17B/DQ17B

DIFFIO_TX_B91p,DQ16B
DIFFIO_TX_B91n,DQ16B
DIFFIO_RX_B92p,DQ16B/CQn16B
DIFFIO_RX_B92n,DQ16B
DIFFIO_TX_B93p,DQ16B
DIFFIO_TX_B93n,DQ16B
DIFFIO_RX_B94p,DQS16B/CQ16B
DIFFIO_RX_B94n,DQSn16B/DQ16B
DIFFIO_TX_B95p,DQ16B
DIFFIO_TX_B95n,DQ16B
DIFFIO_RX_B96p,DQ16B
DIFFIO_RX_B96n,DQ16B
DIFFIO_TX_B97p,DQ17B
DIFFIO_TX_B97n,DQ17B
DIFFIO_RX_B98p,DQ17B/CQn17B
DIFFIO_RX_B98n,DQ17B
DIFFIO_TX_B99p,DQ17B
DIFFIO_TX_B99n,DQ17B

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0.4 Preliminary

ENET_GTX_CLK BA36

CFP_PRG_ALRM2 AP33
SFP2_MOD1_SCL AN33
INT_MSB_CON_TX_FC_CK AK33
FSM_A24 AJ33
FSM_A22 AH33
SFP3_RS1 AG33
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LCD_WEn AM32
FSM_D9 AJ32
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QDR2A_D8 AG30
QDR2A_BWSn0 AJ29
QDR2A_D26 AK29
QDR2A_BWSn2 AF28
QDR2A_BWSn1 AF29
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QDR2A_BWSn3 AE28
AG25
USB_OEn AG26
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AE31 SFP3_RATESEL
AF31 LCD_DATA3
AE29 FSM_A13
AE30 SFP2_MOD2_SDA
AD32 SFP3_MOD0_PRSNTn
AE32 FLASH_RESETn
AD33 FSM_A20
AE33 QSFP1_MOD_SELn
AF32 INT_MSB_CON_RX_FC_SYNC
AG32 CFP_PRG_CNTL2

AM29 QDR2A_D32
AN28 QDR2A_D23
AK30
AL29 QDR2A_D25
AV32 QDR2A_D3
AW32 QDR2A_D12
AT29 QDR2A_D28
AU30 QDR2A_D11
AU31 QDR2A_D10
AV31 QDR2A_D4
AH30 QDR2A_D17
AJ30 QDR2A_D35
AH31 QDR2A_D16
AJ31 QDR2A_D34
AL30 QDR2A_D33
AL31 QDR2A_D24
AR30 QDR2A_D0
AT30 QDR2A_D9
AT32 QDR2A_D1
AU32 QDR2A_D2
AN30 QDR2A_D31
AP30 QDR2A_D22

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QDR2A_Q11 AM28
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QDR2A_Q30 AP27
QDR2A_Q10 AK27
QDR2A_Q1 AL27
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FPGA_USER_LED0 AU27
USB_DATA3 AT26
QDR2A_Q19 AU26
QDR2A_Q24 AL25
QDR2A_Q23 AM25
QDR2A_Q21 AP25
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FPGA_USER_LED4 AV23
FPGA_USER_PB3 AM23
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QDR2A_A2 AR23
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AW26
AR27 QDR2A_Q20
AR28 QDR2A_Q12
AU28 QDR2A_Q13
AV28 QDR2A_Q6
AU29 QDR2A_Q4
AV29 QDR2A_Q5
AY28 QDR2A_Q15
AW29 QDR2A_Q14
BC29 QDR2A_Q8
BD29 QDR2A_Q17
BA28 QDR2A_Q16
BB29 QDR2A_Q7
AW27 QDR2A_Q28
AY27 QDR2A_Q27
AH28 QDR2A_Q9
AJ28 QDR2A_Q0
AH27 QDR2A_CQ_P
AJ27 CPU_RESET
AK26 QDR2A_Q33
AL26 QDR2A_Q32

AU24 QDR2A_A11
AU25 FPGA_USER_PB0
AP24 QDR2A_A0
AR25 QDR2A_A12
AV25 QDR2A_A17
AW24 QDR2A_A6
BA25 QDR2A_A7
BB26 QDR2A_A3
BC26 QDR2A_A5
BD26 QDR2A_A19
AY25 QDR2A_A8
BA24 QDR2A_A4
AJ23 QDR2A_A10
AK23 QDR2A_A16
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AK21 QDR2A_A14
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Bank 4A

ENET_RESETn	AR8	RZQ_1,DIFFIO_RX_B210p,DQ35B		BC7	FPGA_USER_DIPSW1
SFP0_TXDISABLE	AT8	DIFFIO_RX_B210n,DQ35B	DIFFIO_TX_B199p,DQ34B	BD7	FSM_A5
FSM_D8	AP9	DIFFIO_TX_B209p,DQ35B	DIFFIO_TX_B199n,DQ34B	BB8	QSFP1_SDA
CFP_GLB_ALRM	AR9	DIFFIO_TX_B209n,DQ35B	DIFFIO_TX_B201p,DQ34B	BB9	SFP0_MOD0_PRSNTn
SFP3_MOD2_SDA	AM11	DIFFIO_TX_B207p,DQ35B	DIFFIO_TX_B201n,DQ34B	AK9	FSM_D11
VCXOB_UP	AN11	DIFFIO_TX_B207n,DQ35B	DIFFIO_TX_B205p,DQ35B	AL9	FSM_D6
			DIFFIO_TX_B205n,DQ35B		

Bank 4B

ENET_RXD2	AT12	DIFFIO_RX_B198p,DQ33B	DIFFIO_TX_B175p,DQ30B	AE11	ENET_TXD0
LCD_DATA7	AU11	DIFFIO_RX_B198n,DQ33B	DIFFIO_TX_B175n,DQ30B	AE12	LCD_DATA4
FPGA_USER_DIPSW5	AU9	DIFFIO_RX_B197p,DQ33B	DIFFIO_RX_B176p,DQ30B/CQn30B	AD14	FLASH_CEn
ENET_TXD2	AV10	DIFFIO_RX_B197n,DQ33B	DIFFIO_RX_B176n,DQ30B	AE14	ENET_RXD0
	AU10	DIFFIO_RX_B196p,DQS33B/CQ33B	DIFFIO_TX_B177p,DQ30B	AE13	FPGA_USER_DIPSW2
LCD_DATA2	AV11	DIFFIO_RX_B196n,DQSn33B/DQ33B	DIFFIO_TX_B177n,DQ30B	AF14	FLASH_CLK
LCD_D_Cn	AR12	DIFFIO_TX_B195p,DQ33B	DIFFIO_RX_B178p,DQS30B/CQ30B	AF13	FSM_D7
	AR13	DIFFIO_TX_B195n,DQ33B	DIFFIO_RX_B178n,DQSn30B/DQ30B	AG13	SFP1_LOS
ENET_RXD1	AP12	DIFFIO_RX_B194p,DQ33B/CQn33B	DIFFIO_TX_B179p,DQ30B	AE9	VCXOA_DN
ENET_RXD3	AP13	DIFFIO_RX_B194n,DQ33B	DIFFIO_TX_B179n,DQ30B	AE10	QSFP1_LP_MODE
INT_LSB_CON_TX_FC_CK	AM13	DIFFIO_TX_B193p,DQ33B	DIFFIO_RX_B180p,DQ30B	AF10	SFP3_LOS
MAX2_WEn	AN12	DIFFIO_TX_B193n,DQ33B	DIFFIO_RX_B180n,DQ30B	AF11	SFP2_LOS
FSM_A19	AJ12	DIFFIO_RX_B192p,DQ32B	DIFFIO_TX_B181p,DQ31B	BA12	ENET_INTn
ENET_TXD1	AK12	DIFFIO_RX_B192n,DQ32B	DIFFIO_TX_B181n,DQ31B	BB12	SFP3_MOD1_SCL
ENET_TXD3	AL11	DIFFIO_TX_B191p,DQ32B	DIFFIO_RX_B182p,DQ31B/CQn31B	BC11	CFP_TX_DIS
FSM_A6	AL12	DIFFIO_TX_B191n,DQ32B	DIFFIO_RX_B182n,DQ31B	BD11	INT_LSB_CON_RX_FC_SYNC
FPGA_USER_DIPSW0	AG12	DIFFIO_RX_B190p,DQS32B/CQ32B	DIFFIO_TX_B183p,DQ31B	AW11	FSM_A11
CFP_MDIO	AH12	DIFFIO_RX_B190n,DQSn32B/DQ32B	DIFFIO_TX_B183n,DQ31B	AY12	SFP1_RS1
FSM_D0	AG9	DIFFIO_TX_B189p,DQ32B	DIFFIO_RX_B184p,DQS31B/CQ31B	BC10	FSM_D14
SFP3_TXDISABLE	AH10	DIFFIO_TX_B189n,DQ32B	DIFFIO_RX_B184n,DQSn31B/DQ31B	BD10	SFP2_RATESEL
MAX2_CSn	AG10	DIFFIO_RX_B188p,DQ32B/CQn32B	DIFFIO_TX_B185p,DQ31B	AW10	MAX2_CLK
FSM_D1	AG11	DIFFIO_RX_B188n,DQ32B	DIFFIO_TX_B185n,DQ31B	AY10	SFP0_LOS
FSM_A2	AJ10	DIFFIO_TX_B187p,DQ32B	DIFFIO_RX_B186p,DQ31B	BA10	VCXOB_SDA
FLASH_WEn	AJ11	DIFFIO_TX_B187n,DQ32B	DIFFIO_RX_B186n,DQ31B	BB11	VCXOA_SDA

Bank 4C

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QDR2B_D17	AE15	DIFFIO_TX_B151p,DQ26B	DIFFIO_TX_B163p,DQ28B	AU14	QDR2B_Q4
QDR2B_D16	AE16	DIFFIO_TX_B151n,DQ26B	DIFFIO_TX_B163n,DQ28B	AV14	
QDR2B_D7	AE17	DIFFIO_RX_B152p,DQ26B/CQn26B	DIFFIO_RX_B164p,DQ28B/CQn28B	AT15	QDR2B_Q2
QDR2B_D6	AE18	DIFFIO_RX_B152n,DQ26B	DIFFIO_RX_B164n,DQ28B	AU15	QDR2B_Q3
QDR2B_D15	AF16	DIFFIO_TX_B153p,DQ26B	DIFFIO_TX_B165p,DQ28B	AW13	QDR2B_Q7
QDR2B_D13	AG15	DIFFIO_TX_B153n,DQ26B	DIFFIO_TX_B165n,DQ28B	AW14	QDR2B_Q5
QDR2B_D12	AG16	DIFFIO_RX_B154p,DQS26B/CQ26B	DIFFIO_RX_B166p,DQS28B/CQ28B	AP15	QDR2B_CQ_N
QDR2B_D8	AF17	DIFFIO_RX_B154n,DQSn26B/DQ26B	DIFFIO_RX_B166n,DQSn28B/DQ28B	AR16	QDR2B_Q0
QDR2B_D10	AJ14	DIFFIO_TX_B155p,DQ26B	DIFFIO_TX_B167p,DQ28B	AN15	QDR2B_Q11
QDR2B_D9	AK15	DIFFIO_TX_B155n,DQ26B	DIFFIO_TX_B167n,DQ28B	AM16	QDR2B_Q12
QDR2B_D14	AG14	DIFFIO_RX_B156p,DQ26B	DIFFIO_RX_B168p,DQ28B	AL15	QDR2B_Q14
QDR2B_D11	AH15	DIFFIO_RX_B156n,DQ26B	DIFFIO_RX_B168n,DQ28B	AL16	QDR2B_Q13
QDR2B_D0	BC16	DIFFIO_TX_B157p,DQ27B	DIFFIO_TX_B169p,DQ29B	AR15	QDR2B_Q1
QDR2B_D1	BD16	DIFFIO_TX_B157n,DQ27B	DIFFIO_TX_B169n,DQ29B	AR14	QDR2B_Q10
QDR2B_K_P	AY15	DIFFIO_RX_B158p,DQ27B/CQn27B	DIFFIO_RX_B170p,DQ29B/CQn29B	AU12	QDR2B_CQ_P
QDR2B_K_N	BA15	DIFFIO_RX_B158n,DQ27B	DIFFIO_RX_B170n,DQ29B	AV13	QDR2B_Q8
QDR2B_D3	BB14	DIFFIO_TX_B159p,DQ27B	DIFFIO_TX_B171p,DQ29B	AT14	QDR2B_Q9
QDR2B_D2	BB15	DIFFIO_TX_B159n,DQ27B	DIFFIO_TX_B171n,DQ29B	AU13	QDR2B_Q6
QDR2B_D4	BC14	DIFFIO_RX_B160p,DQS27B/CQ27B	DIFFIO_RX_B172p,DQS29B/CQ29B	AH13	QDR2B_Q17
QDR2B_D5	BD14	DIFFIO_RX_B160n,DQSn27B/DQ27B	DIFFIO_RX_B172n,DQSn29B/DQ29B	AJ13	QDR2B_Q16
QDR2B_BWSn1	AY13	DIFFIO_TX_B161p,DQ27B	DIFFIO_TX_B173p,DQ29B	AK14	
QDR2B_BWSn0	BA13	DIFFIO_TX_B161n,DQ27B	DIFFIO_TX_B173n,DQ29B	AL14	QDR2B_Q15
	BC13	DIFFIO_RX_B162p,DQ27B	DIFFIO_RX_B174p,DQ29B	AM14	
	BD13	DIFFIO_RX_B162n,DQ27B	DIFFIO_RX_B174n,DQ29B	AN14	FPGA_USER_LED2

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Bank 4D

1.5V

QDR2B_A15	AL18	DIFFIO_TX_B127p,DQ22B	DIFFIO_RX_B150p,DQ25B	AR18	
QDR2B_A11	AL19	DIFFIO_TX_B127n,DQ22B	DIFFIO_RX_B150n,DQ25B	AT18	USB_EMPTY
QDR2B_A12	AM19	DIFFIO_RX_B128p,DQ22B/CQn22B	DIFFIO_TX_B149p,DQ25B	AR17	
QDR2B_A8	AN20	DIFFIO_RX_B128n,DQ22B	DIFFIO_TX_B149n,DQ25B	AT17	USB_DATA5
QDR2B_A13	AN19	DIFFIO_TX_B129p,DQ22B	DIFFIO_RX_B148p,DQS25B/CQ25B	AN17	FPGA_USER_LED5
QDR2B_A7	AP19	DIFFIO_TX_B129n,DQ22B	DIFFIO_RX_B148n,DQSn25B/DQ25B	AP16	
QDR2B_A9	AP18	DIFFIO_RX_B130p,DQS22B/CQ22B	DIFFIO_TX_B147p,DQ25B	AU16	USB_RDn
QDR2B_A6	AR19	DIFFIO_RX_B130n,DQSn22B/DQ22B	DIFFIO_TX_B147n,DQ25B	AV16	
QDR2B_A1	AV19	DIFFIO_TX_B131p,DQ22B	DIFFIO_RX_B146p,DQ25B/CQn25B	AW16	
QDR2B_A16	AW19	DIFFIO_TX_B131n,DQ22B	DIFFIO_RX_B146n,DQ25B	AW17	USB_RESETn
QDR2B_A0	AU18	DIFFIO_RX_B132p,DQ22B	DIFFIO_TX_B145p,DQ25B	AU17	USB_ADDR1
QDR2B_A10	AU19	DIFFIO_RX_B132n,DQ22B	DIFFIO_TX_B145n,DQ25B	AV17	QDR2B_RPSn
QDR2B_A18	AG17	DIFFIO_TX_B133p,DQ23B	DIFFIO_TX_B143p,DQ24B	AY16	
QDR2B_A2	AG18	DIFFIO_TX_B133n,DQ23B	DIFFIO_TX_B143n,DQ24B	BA16	
QDR2B_A5	AJ15	DIFFIO_RX_B134p,DQ23B/CQn23B	DIFFIO_TX_B141p,DQ24B	BC17	USB_DATA0
QDR2B_A3	AJ16	DIFFIO_RX_B134n,DQ23B	DIFFIO_TX_B141n,DQ24B	BD17	USB_SDA
QDR2B_A17	AJ17	DIFFIO_TX_B135p,DQ23B	DIFFIO_RX_B138p,DQ23B	AJ18	QDR2B_WPSn
QDR2B_A19	AK17	DIFFIO_TX_B135n,DQ23B	DIFFIO_RX_B138n,DQ23B	AK18	FPGA_USER_LED3
QDR2B_A4	AH18	DIFFIO_RX_B136p,DQS23B/CQ23B	DIFFIO_TX_B137p,DQ23B	AL17	
QDR2B_A20	AH19	DIFFIO_RX_B136n,DQSn23B/DQ23B	DIFFIO_TX_B137n,DQ23B	AM17	QDR2B_A14

Bank 4E

QSFP1_MOD_PRSn	AV22	DIFFIO_RX_B118p,DQS20B/CQ20B	DIFFIO_TX_B117p,DQ20B	AU22	SFP3_TXFAULT
FSM_A14	AW22	DIFFIO_RX_B118n,DQSn20B/DQ20B	DIFFIO_TX_B117p,DQ20B	AU21	CFP_PRG_CNTL1
VCXOB_DN	AY21	DIFFIO_TX_B119p,DQ20B	DIFFIO_RX_B116n,DQ20B	AT21	SI5338_PLL_SCL
FSM_A18	BA21	DIFFIO_TX_B119n,DQ20B	DIFFIO_RX_B116p,DQ20B/CQn20B	AR22	QSFP1_RST
FPGA_USER_DIPSW4	AY22	DIFFIO_RX_B120p,DQ20B	DIFFIO_TX_B115n,DQ20B	AR21	LCD_DATA1
LCD_CSn	BA22	DIFFIO_RX_B120n,DQ20B	DIFFIO_TX_B115p,DQ20B	AP21	SFP2_MOD0_PRSNTn
FLASH_RDYBSYn	AU20	DIFFIO_TX_B121p,DQ21B	DIFFIO_RX_B114n,DQ19B	AG20	VCXOA_SCL
FSM_A3	AV20	DIFFIO_RX_B121n,DQ21B	DIFFIO_RX_B114p,DQ19B	AG19	FSM_A10
CFP_MOD_ABS	AR20	DIFFIO_RX_B122p,DQ21B/CQn21B	DIFFIO_TX_B113n,DQ19B	AJ20	INT_LSB_CON_RX_FC_CK
FSM_A23	AT20	DIFFIO_RX_B122n,DQ21B	DIFFIO_TX_B113p,DQ19B	AJ19	SI5338_PLL_SDA
INT_MSB_CON_RX_FC_DATA	AW20	DIFFIO_TX_B123p,DQ21B	DIFFIO_RX_B112n,DQSn19B/DQ19B	AH21	INT_MSB_CON_TX_FC_SYNC
CFP_PRG_CNTL3	AW21	DIFFIO_TX_B123n,DQ21B	DIFFIO_RX_B112p,DQS19B/CQ19B	AG21	FPGA_USER_DIPSW3
QSFP0_LP_MODE	BC22	DIFFIO_RX_B124p,DQS21B/CQ21B	DIFFIO_TX_B111n,DQ19B	AM20	VCXOA_UP
QSFP1_INTERRUPTn	BD22	DIFFIO_RX_B124n,DQSn21B/DQ21B	DIFFIO_TX_B111p,DQ19B	AL20	SFP1_MOD1_SCL
FSM_A26	BC20	DIFFIO_TX_B125p,DQ21B	DIFFIO_RX_B110n,DQ19B	AJ21	FSM_D13
LCD_DATA5	BD20	DIFFIO_TX_B125n,DQ21B	DIFFIO_RX_B110p,DQ19B/CQn19B	AK20	QSFP0_MOD_SELn
CFP_RX_LOS	BB20	DIFFIO_RX_B126p,DQ21B	DIFFIO_TX_B109n,DQ19B	AN22	SFP2_TXDISABLE
SFP1_TXFAULT	BB21	DIFFIO_RX_B126n,DQ21B	DIFFIO_TX_B109p,DQ19B	AM22	QSFP0_INTERRUPTn

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QDR2B_D[17..0] 28,29

QDR2B_A[20..0] 28,29

QDR2B_RPSn	QDR2B_RPSn	28,29
QDR2B_WPSn	QDR2B_WPSn	28,29
QDR2B_CQ_N	QDR2B_CQ_N	28
QDR2B_CQ_P	QDR2B_CQ_P	28
QDR2B_BWSn1	QDR2B_BWSn1	28,29
QDR2B_BWSn0	QDR2B_BWSn0	28,29
QDR2B_K_P	QDR2B_K_P	28
QDR2B_K_N	QDR2B_K_N	28

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QSFP1_SDA		33
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VCXOB_UP		19
VCXOB_DN		19
VCXOA_DN		26
VCXOB_SDA		19
VCXOA_SCL		26
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MAX2_CSn		14
MAX2_CLK		14
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SFP2_TXDISABLE		34
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SFP2_LOS		34
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SFP0_MOD0_PRSNTn		34
SFP0_TXDISABLE		34
SFP0_LOS		34
SFP2_MOD0_PRSNTn		34
SFP1_MOD1_SCL		34
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DDR3_RZQIN — 100, 1% — R297

DDR3A_WEn, DDR3A_ODT → DDR3A_WEn, DDR3A_ODT (30, 30)

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DDR3_RZQIN	H9	RZQ_4,DIFFIO_RX_T1p,DQ1T		B7	DDR3A_A8
DDR3A_A5	H8	DIFFIO_RX_T1n,DQ1T	Bank 7A	A7	DDR3A_RSTn
DDR3A_ODT	K8	DIFFIO_TX_T2p,DQ1T		D10	DDR3A_A0
DDR3A_A6	J9	DIFFIO_TX_T2n,DQ1T		C9	DDR3A_WEn
DDR3A_A11	K10	DIFFIO_TX_T4p,DQ1T		P8	DDR3A_A7
DDR3A_A12	K9	DIFFIO_TX_T4n,DQ1T		N8	DDR3A_A10
DDR3A_DQ3	V10	DIFFIO_RX_T13p,DQ3T		B10	DDR3B_A10
DDR3A_DQ0	V9	DIFFIO_RX_T13n,DQ3T	Bank 7B	A10	DDR3A_DQ27
DDR3A_DQ2	T10	DIFFIO_TX_T14p,DQ3T		B11	DDR3A_DQ26
DDR3A_DQ6	R10	DIFFIO_TX_T14n,DQ3T		A11	DDR3A_DQ25
DDR3A_DQS_P0	U9	DIFFIO_RX_T15p,DQS3T/CQ3T		D11	DDR3B_CSn
DDR3A_DQS_N0	T9	DIFFIO_RX_T15n,DQSn3T/DQ3T		C10	DDR3A_DQ30
DDR3A_A9	P12	DIFFIO_TX_T16p,DQ3T		D12	DDR3A_DQS_P3
DDR3A_DQ4	R12	DIFFIO_TX_T16n,DQ3T		C12	DDR3A_DQS_N3
DDR3A_DQ5	T12	DIFFIO_RX_T17p,DQ3T/CQn3T		E12	DDR3A_DQ24
DDR3A_DQ1	T11	DIFFIO_RX_T17n,DQ3T		E11	DDR3A_DQ31
DDR3A_A2	M12	DIFFIO_TX_T18p,DQ3T		G11	DDR3A_DQ28
DDR3A_DQ7	L12	DIFFIO_TX_T18n,DQ3T		F11	DDR3A_DQ29
DDR3A_DQ15	J10	DIFFIO_RX_T19p,DQ4T		U12	DDR3B_ODT
DDR3A_DQ14	H10	DIFFIO_RX_T19n,DQ4T		U11	DDR3A_DQ18
DDR3A_DQ12	N11	DIFFIO_TX_T20p,DQ4T		V12	DDR3A_DQ19
DDR3A_DQ13	M11	DIFFIO_TX_T20n,DQ4T		V11	DDR3A_DQ16
DDR3A_DQS_P1	K11	DIFFIO_RX_T21p,DQS4T/CQ4T		U14	DDR3A_A13
DDR3A_DQS_N1	L11	DIFFIO_RX_T21n,DQSn4T/DQ4T		T14	DDR3A_DQ23
DDR3A_CKE	H12	DIFFIO_TX_T22p,DQ4T		P14	DDR3A_DQS_P2
DDR3A_DQ9	H11	DIFFIO_TX_T22n,DQ4T		N14	DDR3A_DQS_N2
DDR3A_DQ10	G10	DIFFIO_RX_T23p,DQ4T/CQn4T		T13	DDR3A_DQ22
DDR3A_DQ11	F10	DIFFIO_RX_T23n,DQ4T		R13	DDR3A_DQ17
DDR3A_A4	K12	DIFFIO_TX_T24p,DQ4T		P13	DDR3A_DQ21
DDR3A_DQ8	J12	DIFFIO_TX_T24n,DQ4T		N13	DDR3A_DQ20
DDR3B_DQ5	H14	DIFFIO_RX_T37p,DQ7T		K15	DDR3B_DQ19
DDR3B_DQ1	H13	DIFFIO_RX_T37n,DQ7T	Bank 7C	J15	DDR3B_DQ22
DDR3B_DQ3	K13	DIFFIO_TX_T38p,DQ7T		M14	DDR3B_A1
DDR3B_DQ0	J13	DIFFIO_TX_T38n,DQ7T		L14	DDR3B_DQ16
DDR3B_DQS_P0	L15	DIFFIO_RX_T39p,DQS7T/CQ7T		F14	DDR3B_DQ26
DDR3B_DQS_N0	K14	DIFFIO_RX_T39n,DQSn7T/DQ7T		E14	DDR3B_DQ27
DDR3B_BA1	G13	DIFFIO_TX_T40p,DQ7T		D14	DDR3B_DQ31
DDR3B_DQ2	F13	DIFFIO_TX_T40n,DQ7T		C13	DDR3B_DQ28
DDR3B_DQ4	H15	DIFFIO_RX_T41p,DQ7T/CQn7T		E15	DDR3B_DQS_P3
DDR3B_DQ6	G14	DIFFIO_RX_T41n,DQ7T		D15	DDR3B_DQS_N3
DDR3B_A8	K16	DIFFIO_TX_T42p,DQ7T		B13	DDR3B_A12
DDR3B_DQ7	J16	DIFFIO_TX_T42n,DQ7T		A13	DDR3B_DQ29
DDR3B_DQ9	Y17	DIFFIO_RX_T43p,DQ8T		C16	DDR3B_DQ24
DDR3B_DQ8	W17	DIFFIO_RX_T43n,DQ8T		C15	DDR3B_DQ25
DDR3B_DQ13	W14	DIFFIO_TX_T44p,DQ8T		B14	DDR3B_A5
DDR3B_DQ12	V13	DIFFIO_TX_T44n,DQ8T		A14	DDR3B_DQ30
DDR3B_DQS_P1	Y16	DIFFIO_RX_T45p,DQS8T/CQ8T		N16	DDR3B_A11
DDR3B_DQS_N1	W16	DIFFIO_RX_T45n,DQSn8T/DQ8T		M15	DDR3B_DQ18
DDR3B_A6	U15	DIFFIO_TX_T46p,DQ8T		V17	DDR3B_DQS_P2
DDR3B_DQ14	T15	DIFFIO_TX_T46n,DQ8T		U17	DDR3B_DQS_N2
DDR3B_DQ10	R15	DIFFIO_RX_T47p,DQ8T/CQn8T		T17	DDR3B_DQ23
DDR3B_DQ11	P15	DIFFIO_RX_T47n,DQ8T		T16	DDR3B_DQ17
DDR3B_RSTn	V16	DIFFIO_TX_T48p,DQ8T		R16	DDR3B_DQ21
DDR3B_DQ15	V15	DIFFIO_TX_T48n,DQ8T		P16	DDR3B_DQ20

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DDR3C_DQ27	K19	DIFFIO_TX_T84n,DQ14T		N17	DDR3C_DQ0
DDR3B_BA2	L20	DIFFIO_TX_T84p,DQ14T	Bank 7D	P17	DDR3C_DQ3
DDR3C_DQ25	M20	DIFFIO_RX_T83n,DQ14T		R19	DDR3C_DQ7
DDR3C_DQ26	N19	DIFFIO_RX_T83p,DQ14T/CQn14T		R18	DDR3C_DQ4
DDR3C_DQ24	N20	DIFFIO_TX_T82n,DQ14T		P19	DDR3C_DQS_P0
DDR3B_CKE	P20	DIFFIO_TX_T82p,DQ14T		P18	DDR3C_DQS_N0
DDR3C_DQS_N3	T19	DIFFIO_RX_T81n,DQSn14T/DQ14T		M18	DDR3B_CASn
DDR3C_DQS_P3	T20	DIFFIO_RX_T81p,DQS14T/CQ14T		M17	DDR3C_DQ5
DDR3C_DQ30	V18	DIFFIO_TX_T80n,DQ14T		L18	DDR3C_DQ6
DDR3C_DQ28	W18	DIFFIO_TX_T80p,DQ14T		L17	DDR3C_DQ1
DDR3C_DQ31	T18	DIFFIO_RX_T79n,DQ14T		K18	DDR3B_WEn
DDR3C_DQ29	U18	DIFFIO_RX_T79p,DQ14T		K17	DDR3C_DQ2
DDR3C_DQ17	A19	DIFFIO_TX_T78n,DQ13T		H17	DDR3C_DQ8
DDR3B_BA0	B19	DIFFIO_TX_T78p,DQ13T		H16	DDR3C_DQ15
DDR3C_DQ18	C18	DIFFIO_RX_T77n,DQ13T		G17	DDR3C_DQ9
DDR3C_DQ21	C19	DIFFIO_RX_T77p,DQ13T/CQn13T		F17	DDR3C_DQ11
DDR3C_DQ16	A17	DIFFIO_TX_T76n,DQ13T		J19	DDR3C_DQ23
DDR3B_RASn	B17	DIFFIO_TX_T76p,DQ13T		H19	DDR3C_DQ20
DDR3C_DQS_P2	G19	DIFFIO_RX_T75p,DQS13T/CQ13T		E18	DDR3C_DQ22
DDR3C_DQS_N2	F19	DIFFIO_RX_T75n,DQSn13T/DQ13T		D18	DDR3C_DQ19
DDR3C_A4	H21	DIFFIO_RX_T93p,DQS16T/CQ16T		G20	DDR3C_A11
DDR3C_A8	H20	DIFFIO_RX_T93n,DQSn16T/DQ16T		F20	DDR3C_CASn
DDR3C_A1	L21	DIFFIO_TX_T92p,DQ16T		H22	DDR3C_RSTn
DDR3C_A6	K20	DIFFIO_TX_T92n,DQ16T		G22	DDR3C_A3
DDR3C_A9	K21	DIFFIO_RX_T91p,DQ16T	Bank 7E	K22	DDR3C_A13
DDR3C_A7	J21	DIFFIO_RX_T91n,DQ16T		J22	DDR3C_A2
DDR3C_A10	T22	DIFFIO_TX_T90p,DQ15T		F22	DDR3C_CKE
DDR3C_ODT	R22	DIFFIO_TX_T90n,DQ15T		F21	DDR3C_RASn
DDR3C_A12	N22	DIFFIO_RX_T89p,DQ15T/CQn15T		E21	DDR3C_BA0
DDR3C_A5	M22	DIFFIO_RX_T89n,DQ15T		E20	DDR3C_WEn
DDR3C_CSn	R21	DIFFIO_TX_T88p,DQ15T		D21	DDR3C_A0
DDR3C_BA1	P21	DIFFIO_TX_T88n,DQ15T		D20	DDR3C_BA2
DDR3C_CK_P	V21	DIFFIO_RX_T87p,DQS15T/CQ15T		B20	DDR3B_A0
DDR3C_CK_N	V20	DIFFIO_RX_T87n,DQSn15T/DQ15T		A20	DDR3B_A3
DDR3B_A9	U21	DIFFIO_TX_T86p,DQ15T		C22	DDR3B_A2
DDR3B_A7	T21	DIFFIO_TX_T86n,DQ15T		C21	
DDR3B_A13	V19	DIFFIO_RX_T85p,DQ15T		B22	
DDR3B_A4	U20	DIFFIO_RX_T85n,DQ15T		A22	

		DIFFIO_RX_T63p,DQS11T/CQ11T		N17	DDR3C_DQ0
		DIFFIO_RX_T63n,DQSn11T/DQ11T		P17	DDR3C_DQ3
		DIFFIO_TX_T64p,DQ11T		R19	DDR3C_DQ7
		DIFFIO_TX_T64n,DQ11T		R18	DDR3C_DQ4
		DIFFIO_RX_T65p,DQ11T/CQn11T		P19	DDR3C_DQS_P0
		DIFFIO_RX_T65n,DQ11T		P18	DDR3C_DQS_N0
		DIFFIO_TX_T66p,DQ11T		M18	DDR3B_CASn
		DIFFIO_TX_T66n,DQ11T		M17	DDR3C_DQ5
		DIFFIO_TX_T68p,DQ12T		L18	DDR3C_DQ6
		DIFFIO_TX_T68n,DQ12T		L17	DDR3C_DQ1
		DIFFIO_TX_T70p,DQ12T		K18	DDR3B_WEn
		DIFFIO_TX_T70n,DQ12T		K17	DDR3C_DQ2
		DIFFIO_RX_T73p,DQ13T		H17	DDR3C_DQ8
		DIFFIO_RX_T73n,DQ13T		H16	DDR3C_DQ15
		DIFFIO_TX_T74p,DQ13T		G17	DDR3C_DQ9
		DIFFIO_TX_T74n,DQ13T		F17	DDR3C_DQ11
		DIFFIO_TX_T94p,DQ16T		J19	DDR3C_DQ23
		DIFFIO_TX_T94n,DQ16T		H19	DDR3C_DQ20
		DIFFIO_RX_T95p,DQ16T/CQn16T		E18	DDR3C_DQ22
		DIFFIO_RX_T95n,DQ16T		D18	DDR3C_DQ19
		DIFFIO_TX_T96p,DQ16T		G20	DDR3C_A11
		DIFFIO_TX_T96n,DQ16T		F20	DDR3C_CASn
		DIFFIO_TX_T97p,DQ17T		H22	DDR3C_RSTn
		DIFFIO_TX_T97n,DQ17T		G22	DDR3C_A3
		DIFFIO_TX_T98p,DQ17T		K22	DDR3C_A13
		DIFFIO_TX_T98n,DQ17T		J22	DDR3C_A2
		DIFFIO_RX_T99p,DQS17T/CQ17T		F22	DDR3C_CKE
		DIFFIO_RX_T99n,DQSn17T/DQ17T		F21	DDR3C_RASn
		DIFFIO_TX_T100p,DQ17T		E21	DDR3C_BA0
		DIFFIO_TX_T100n,DQ17T		E20	DDR3C_WEn
		DIFFIO_RX_T101p,DQ17T/CQn17T		D21	DDR3C_A0
		DIFFIO_RX_T101n,DQ17T		D20	DDR3C_BA2
		DIFFIO_TX_T102p,DQ17T		B20	DDR3B_A0
		DIFFIO_TX_T102n,DQ17T		A20	DDR3B_A3
				C22	DDR3B_A2
				C21	
				B22	
				A22	

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DDR3A_DQ[31..0] → DDR3A_DQ[31..0] 30

DDR3A_A[13..0] → DDR3A_A[13..0] 19,30

DDR3A_BA[2..0] → DDR3A_BA[2..0] 30

DDR3A_CKE → DDR3A_CKE 30

DDR3A_DQS_N[3..0] → DDR3A_DQS_N[3..0] 30

DDR3A_DQS_P[3..0] → DDR3A_DQS_P[3..0] 30

DDR3A_RSTn → DDR3A_RSTn 30

DDR3B_A[13..0] → DDR3B_A[13..0] 30

DDR3B_BA[2..0] → DDR3B_BA[2..0] 19,30

DDR3B_CASn → DDR3B_CASn 30

DDR3B_CKE → DDR3B_CKE 30

DDR3B_CSn → DDR3B_CSn 30

DDR3B_DQ[31..0] → DDR3B_DQ[31..0] 30

DDR3B_DQS_N[3..0] → DDR3B_DQS_N[3..0] 30

DDR3B_DQS_P[3..0] → DDR3B_DQS_P[3..0] 30

DDR3B_ODT → DDR3B_ODT 30

DDR3B_RASn → DDR3B_RASn 30

DDR3B_WEn → DDR3B_WEn 30

DDR3C_A[13..0] → DDR3C_A[13..0] 31

DDR3C_BA[2..0] → DDR3C_BA[2..0] 31

DDR3C_CASn → DDR3C_CASn 31

DDR3C_CKE → DDR3C_CKE 31

DDR3C_CK_N → DDR3C_CK_N 31

DDR3C_CK_P → DDR3C_CK_P 31

DDR3C_CSn → DDR3C_CSn 31

DDR3C_DQ[31..0] → DDR3C_DQ[31..0] 19,31

DDR3C_DQS_N[3..0] → DDR3C_DQS_N[3..0] 19,31

DDR3C_DQS_P[3..0] → DDR3C_DQS_P[3..0] 19,31

DDR3C_ODT → DDR3C_ODT 31

DDR3C_RASn → DDR3C_RASn 31

DDR3C_RSTn → DDR3C_RSTn 31

DDR3C_WEn → DDR3C_WEn 31

DDR3D_A[13..0] → DDR3D_A[13..0] 31

DDR3B_RSTn → DDR3B_RSTn 30

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	M38	DIFFIO_TX_T210n,DQ35T	Bank 8A	DIFFIO_TX_T194p,DQ33T	C37 DDR3F_A5
	M39	DIFFIO_TX_T210p,DQ35T		DIFFIO_TX_T194n,DQ33T	B38 DDR3F_BA1
	L35	DIFFIO_RX_T209n,DQ35T		DIFFIO_TX_T196p,DQ33T	E36 DDR3F_BA2
	L36	DIFFIO_RX_T209p,DQ35T/CQn35T		DIFFIO_TX_T196n,DQ33T	D37 DDR3F_A1
	M36	DIFFIO_TX_T208n,DQ35T		DIFFIO_TX_T200p,DQ34T	W35 DDR3F_CASn
	M37	DIFFIO_TX_T208p,DQ35T		DIFFIO_TX_T200n,DQ34T	V36 DDR3F_WEn
	K36	DIFFIO_RX_T207n,DQSn35T/DQ35T		DIFFIO_TX_T202p,DQ34T	P39 DDR3F_A2
	K37	DIFFIO_RX_T207p,DQS35T/CQ35T		DIFFIO_TX_T202n,DQ34T	P38 DDR3F_A7
DDR3F_RASn	K34	DIFFIO_TX_T206n,DQ35T		DIFFIO_RX_T203p,DQ34T/CQn34T	P36 DDR3F_CKE
	K35	DIFFIO_TX_T206p,DQ35T		RZQ_5,DIFFIO_RX_T203n,DQ34T	P35 QDR2_RZQIN
DDR3F_A3	H36	DIFFIO_RX_T205n,DQ35T		DIFFIO_TX_T204p,DQ34T	N38 DDR3F_RSTn
DDR3F_A11	J36	DIFFIO_RX_T205p,DQ35T		DIFFIO_TX_T204n,DQ34T	N37 DDR3F_A8
DDR3F_DQ31	L33	DIFFIO_TX_T192n,DQ32T	Bank 8B		
	M34	DIFFIO_TX_T192p,DQ32T			
DDR3F_DQ28	K32	DIFFIO_RX_T191n,DQ32T		DIFFIO_RX_T169p,DQ29T	A35 DDR3F_DQ6
DDR3F_DQ29	L32	DIFFIO_RX_T191p,DQ32T/CQn32T		DIFFIO_RX_T169n,DQ29T	A34 DDR3F_DQ1
DDR3F_DQ30	P34	DIFFIO_TX_T190n,DQ32T		DIFFIO_TX_T170p,DQ29T	C33 DDR3F_DQ0
	R33	DIFFIO_TX_T190p,DQ32T		DIFFIO_TX_T170n,DQ29T	B32 DDR3F_DQ3
DDR3F_DQS_N3	T35	DIFFIO_RX_T189n,DQSn32T/DQ32T		DIFFIO_RX_T171p,DQS29T/CQ29T	C34 DDR3F_DQS_P0
DDR3F_DQS_P3	U35	DIFFIO_RX_T189p,DQS32T/CQ32T		DIFFIO_RX_T171n,DQSn29T/DQ29T	B34 DDR3F_DQS_N0
DDR3F_DQ27	R34	DIFFIO_TX_T188n,DQ32T		DIFFIO_TX_T172p,DQ29T	E33
DDR3F_DQ26	T34	DIFFIO_TX_T188p,DQ32T		DIFFIO_TX_T172n,DQ29T	D33 DDR3F_DQ2
DDR3F_DQ24	V35	DIFFIO_RX_T187n,DQ32T		DIFFIO_RX_T173p,DQ29T/CQn29T	C36 DDR3F_DQ7
DDR3F_DQ25	W34	DIFFIO_RX_T187p,DQ32T		DIFFIO_RX_T173n,DQ29T	B35 DDR3F_DQ5
DDR3F_DQ20	J33	DIFFIO_TX_T186n,DQ31T		DIFFIO_TX_T174p,DQ29T	D36 FPGA_USER_LED6
	J34	DIFFIO_TX_T186p,DQ31T		DIFFIO_TX_T174n,DQ29T	D35 DDR3F_DQ4
DDR3F_DQ16	H33	DIFFIO_RX_T185n,DQ31T		DIFFIO_RX_T175p,DQ30T	U33 DDR3F_DQ11
DDR3F_DQ22	H34	DIFFIO_RX_T185p,DQ31T/CQn31T		DIFFIO_RX_T175n,DQ30T	U32 DDR3F_DQ10
DDR3F_DQ23	J31	DIFFIO_TX_T184n,DQ31T		DIFFIO_TX_T176p,DQ30T	V34 DDR3F_DQ8
	K31	DIFFIO_TX_T184p,DQ31T		DIFFIO_TX_T176n,DQ30T	V33 DDR3F_DQ9
DDR3F_DQS_N2	G35	DIFFIO_RX_T183n,DQSn31T/DQ31T		DIFFIO_RX_T177p,DQS30T/CQ30T	T33 DDR3F_DQS_P1
DDR3F_DQS_P2	H35	DIFFIO_RX_T183p,DQS31T/CQ31T		DIFFIO_RX_T177n,DQSn30T/DQ30T	T32 DDR3F_DQS_N1
DDR3F_DQ18	F34	DIFFIO_TX_T182n,DQ31T		DIFFIO_TX_T178p,DQ30T	N31
DDR3F_DQ19	G34	DIFFIO_TX_T182p,DQ31T		DIFFIO_TX_T178n,DQ30T	M31 DDR3F_DQ12
DDR3F_DQ17	E35	DIFFIO_RX_T181n,DQ31T		DIFFIO_RX_T179p,DQ30T/CQn30T	N32 DDR3F_DQ13
DDR3F_DQ21	F35	DIFFIO_RX_T181p,DQ31T		DIFFIO_RX_T179n,DQ30T	M33 DDR3F_DQ15
DDR3F_DQ14	P32	DIFFIO_TX_T180n,DQ30T			
	P33	DIFFIO_TX_T180p,DQ30T			
DDR3E_DQ7	Y28	DIFFIO_RX_T145p,DQ25T	Bank 8C		
DDR3E_DQ5	Y27	DIFFIO_RX_T145n,DQ25T		DIFFIO_RX_T155p,DQ26T/CQn26T	E32 DDR3E_DQ8
DDR3E_DQ1	W28	DIFFIO_TX_T146p,DQ25T		DIFFIO_RX_T155n,DQ26T	D32 DDR3E_DQ9
DDR3E_DQ2	V28	DIFFIO_TX_T146n,DQ25T		DIFFIO_TX_T156p,DQ26T	G31 DDR3E_RASn
DDR3E_DQS_P0	Y30	DIFFIO_RX_T147p,DQS25T/CQ25T		DIFFIO_TX_T156n,DQ26T	F31 DDR3E_DQ10
DDR3E_DQS_N0	Y29	DIFFIO_RX_T147n,DQSn25T/DQ25T		DIFFIO_RX_T157p,DQ27T	G32 DDR3E_DQ20
DDR3E_RSTn	W29	DIFFIO_TX_T148p,DQ25T		DIFFIO_RX_T157n,DQ27T	F32 DDR3E_DQ21
DDR3E_DQ4	V30	DIFFIO_TX_T148n,DQ25T		DIFFIO_TX_T158p,DQ27T	H32 DDR3E_DQ23
DDR3E_DQ3	T28	DIFFIO_RX_T149p,DQ25T/CQn25T		DIFFIO_TX_T158n,DQ27T	H31 DDR3E_DQ17
DDR3E_DQ0	R28	DIFFIO_RX_T149n,DQ25T		DIFFIO_RX_T159p,DQS27T/CQ27T	J30 DDR3E_DQS_P2
DDR3E_A9	V29	DIFFIO_TX_T150p,DQ25T		DIFFIO_RX_T159n,DQSn27T/DQ27T	H30 DDR3E_DQS_N2
DDR3E_DQ6	U29	DIFFIO_TX_T150n,DQ25T		DIFFIO_TX_T160p,DQ27T	L30 DDR3E_BA0
				DIFFIO_TX_T160n,DQ27T	L29 DDR3E_DQ18
DDR3E_DQ11	A32				K30 DDR3E_DQ19
DDR3E_DQ13	A31	DIFFIO_RX_T151p,DQ26T		DIFFIO_RX_T161p,DQ27T/CQn27T	K29 DDR3E_DQ16
DDR3E_DQ14	C30	DIFFIO_RX_T151n,DQ26T		DIFFIO_RX_T161n,DQ27T	N29 DDR3E_BA2
DDR3E_DQ12	B29	DIFFIO_TX_T152p,DQ26T		DIFFIO_TX_T162p,DQ27T	M30 DDR3E_DQ22
DDR3E_DQS_P1	C31	DIFFIO_TX_T152n,DQ26T		DIFFIO_TX_T162n,DQ27T	U30 DDR3E_DQ29
DDR3E_DQS_N1	B31	DIFFIO_RX_T153p,DQS26T/CQ26T		DIFFIO_RX_T163p,DQ28T	T29 DDR3E_DQ28
DDR3E_CKE	E30	DIFFIO_RX_T153n,DQSn26T/DQ26T		DIFFIO_RX_T163n,DQ28T	P31 DDR3E_DQ30
DDR3E_DQ15	D30	DIFFIO_TX_T154p,DQ26T		DIFFIO_RX_T164p,DQ28T	P30 DDR3E_DQ31
DDR3E_A7	T31	DIFFIO_TX_T154n,DQ26T		DIFFIO_RX_T164n,DQ28T	T30 DDR3E_DQS_P3
DDR3E_DQ27	R31	DIFFIO_TX_T168p,DQ28T		DIFFIO_RX_T165p,DQS28T/CQ28T	R30 DDR3E_DQS_N3
DDR3E_DQ24	W32	DIFFIO_TX_T168n,DQ28T		DIFFIO_RX_T165n,DQSn28T/DQ28T	Y32 DDR3E_A13
DDR3E_DQ26	V31	DIFFIO_RX_T167p,DQ28T/CQn28T		DIFFIO_TX_T166p,DQ28T	W31 DDR3E_DQ25
		DIFFIO_RX_T167n,DQ28T		DIFFIO_TX_T166n,DQ28T	

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DDR3D_DQ6	D27	DIFFIO_RX_T121p,DQ21T	Bank 8D	DIFFIO_TX_T144p,DQ24T	P28 DDR3E_A0
DDR3D_DQ5	C27	DIFFIO_RX_T121n,DQ21T		DIFFIO_TX_T144n,DQ24T	P29 DDR3D_DQ31
DDR3D_DQ2	B26	DIFFIO_TX_T122p,DQ21T		DIFFIO_RX_T143p,DQ24T/CQn24T	P26 DDR3D_DQ28
DDR3D_DQ1	A26	DIFFIO_TX_T122n,DQ21T		DIFFIO_RX_T143n,DQ24T	N26 DDR3D_DQ30
DDR3D_DQS_P0	F26	DIFFIO_RX_T123p,DQS21T/CQ21T		DIFFIO_TX_T142p,DQ24T	R27 DDR3E_A3
DDR3D_DQS_N0	E27	DIFFIO_RX_T123n,DQSn21T/DQ21T		DIFFIO_TX_T142n,DQ24T	P27 DDR3D_DQ29
DDR3E_A1	A29	DIFFIO_TX_T124p,DQ21T		DIFFIO_RX_T141p,DQS24T/CQ24T	L27 DDR3D_DQS_P3
DDR3D_DQ7	A28	DIFFIO_TX_T124n,DQ21T		DIFFIO_RX_T141n,DQSn24T/DQ24T	K27 DDR3D_DQS_N3
DDR3D_DQ3	E29	DIFFIO_RX_T125p,DQ21T/CQn21T		DIFFIO_TX_T140p,DQ24T	N28 DDR3D_DQ27
DDR3D_DQ0	D29	DIFFIO_RX_T125n,DQ21T		DIFFIO_TX_T140n,DQ24T	M28 DDR3D_DQ25
DDR3E_A5	C28	DIFFIO_TX_T126p,DQ21T		DIFFIO_RX_T139p,DQ24T	M27 DDR3D_DQ26
DDR3D_DQ4	B28	DIFFIO_TX_T126n,DQ21T		DIFFIO_RX_T139n,DQ24T	L26 DDR3D_DQ24
DDR3D_DQ9	G29	DIFFIO_TX_T127p,DQ22T		DIFFIO_TX_T138p,DQ23T	T27 DDR3E_A4
DDR3D_DQ10	G28	DIFFIO_TX_T127n,DQ22T		DIFFIO_TX_T138n,DQ23T	U27 DDR3D_DQ21
DDR3D_DQ8	F29	DIFFIO_TX_T128p,DQ22T		DIFFIO_RX_T137p,DQ23T/CQn23T	V25 DDR3D_DQ16
DDR3D_DQ11	F28	DIFFIO_TX_T128n,DQ22T		DIFFIO_RX_T137n,DQ23T	U26 DDR3D_DQ22
DDR3D_DQS_P1	H27	DIFFIO_RX_T129p,DQS22T/CQ22T		DIFFIO_TX_T136p,DQ23T	V27 DDR3E_A2
DDR3D_DQS_N1	G26	DIFFIO_RX_T129n,DQSn22T/DQ22T		DIFFIO_TX_T136n,DQ23T	V26 DDR3D_DQ18
DDR3E_CASn	H29	DIFFIO_TX_T130p,DQ22T		DIFFIO_TX_T134p,DQ23T	T26 DDR3D_DQ17
DDR3D_DQ14	H28	DIFFIO_TX_T130n,DQ22T		DIFFIO_TX_T134n,DQ23T	T25 DDR3D_DQ19
DDR3D_DQ12	J27	DIFFIO_RX_T131p,DQ22T/CQn22T		DIFFIO_TX_T132p,DQ22T	K28 DDR3E_WEn
DDR3D_DQ13	H26	DIFFIO_RX_T131n,DQ22T		DIFFIO_TX_T132n,DQ22T	J28 DDR3D_DQ15
DDR3E_A8	P23	DIFFIO_TX_T112p,DQ19T	Bank 8E	DIFFIO_RX_T111p,DQS19T/CQ19T	R24 DDR3D_A7
DDR3E_A11	N23	DIFFIO_TX_T112n,DQ19T		DIFFIO_RX_T111n,DQSn19T/DQ19T	P24 DDR3D_A4
DDR3D_CK_P	L23	DIFFIO_RX_T113p,DQ19T/CQn19T		DIFFIO_TX_T110p,DQ19T	U23 DDR3D_A13
DDR3D_CK_N	K24	DIFFIO_RX_T113n,DQ19T		DIFFIO_TX_T110n,DQ19T	T23 DDR3D_A2
DDR3E_A6	M23	DIFFIO_RX_T114p,DQ19T		DIFFIO_RX_T109p,DQ19T	U24 DDR3D_CKE
DDR3E_A12	L24	DIFFIO_RX_T114n,DQ19T		DIFFIO_RX_T109n,DQ19T	T24 DDR3D_A9
DDR3E_CSn	H24	DIFFIO_RX_T115p,DQ20T		DIFFIO_TX_T108p,DQ18T	E24 DDR3D_WEn
DDR3E_A10	H23	DIFFIO_RX_T115n,DQ20T		DIFFIO_TX_T108n,DQ18T	D24 DDR3D_A8
DDR3E_BA1	J25	DIFFIO_TX_T116p,DQ20T		DIFFIO_RX_T107p,DQ18T/CQn18T	G23 DDR3D_A10
DDR3E_ODT	J24	DIFFIO_TX_T116n,DQ20T		DIFFIO_RX_T107n,DQ18T	F23 DDR3D_CSn
DDR3E_CK_P	K26	DIFFIO_RX_T117p,DQS20T/CQ20T		DIFFIO_TX_T106p,DQ18T	E23 DDR3D_RASn
DDR3E_CK_N	K25	DIFFIO_RX_T117n,DQSn20T/DQ20T		DIFFIO_TX_T106n,DQ18T	D23 DDR3D_A11
DDR3D_A0	F25	DIFFIO_TX_T118p,DQ20T		DIFFIO_RX_T105p,DQS18T/CQ18T	C25 DDR3D_A6
DDR3D_CASn	F24	DIFFIO_TX_T118n,DQ20T		DIFFIO_RX_T105n,DQSn18T/DQ18T	C24 DDR3D_A12
DDR3D_BA0	H25	DIFFIO_RX_T119p,DQ20T/CQn20T		DIFFIO_TX_T104p,DQ18T	B23 DDR3D_BA1
DDR3D_BA2	G25	DIFFIO_RX_T119n,DQ20T		DIFFIO_TX_T104n,DQ18T	A23 DDR3D_ODT
DDR3D_A3	E26	DIFFIO_TX_T120p,DQ20T		DIFFIO_RX_T103n,DQ18T	A25 DDR3D_A5
DDR3D_RSTn	D26	DIFFIO_TX_T120n,DQ20T		DIFFIO_RX_T103p,DQ18T	B25 DDR3D_A1

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DDR3B_A5	DDR3B_A5	24,30
DDR3D_A[13..0]	DDR3D_A[13..0]	24,31
DDR3D_BA[2..0]	DDR3D_BA[2..0]	31
DDR3D_CASn	DDR3D_CASn	31
DDR3D_CKE	DDR3D_CKE	31
DDR3D_CK_N	DDR3D_CK_N	31
DDR3D_CK_P	DDR3D_CK_P	31
DDR3D_CSn	DDR3D_CSn	31
DDR3D_DQ[31..0]	DDR3D_DQ[31..0]	19,31
DDR3D_DQS_N[3..0]	DDR3D_DQS_N[3..0]	19,31
DDR3D_DQS_P[3..0]	DDR3D_DQS_P[3..0]	19,31
DDR3D_ODT	DDR3D_ODT	31
DDR3D_RASn	DDR3D_RASn	31
DDR3D_RSTn	DDR3D_RSTn	31
DDR3D_WEn	DDR3D_WEn	31
DDR3E_A[13..0]	DDR3E_A[13..0]	32
DDR3E_BA[2..0]	DDR3E_BA[2..0]	32
DDR3E_CASn	DDR3E_CASn	32
DDR3E_CKE	DDR3E_CKE	32
DDR3E_CK_N	DDR3E_CK_N	32
DDR3E_CK_P	DDR3E_CK_P	32
DDR3E_CSn	DDR3E_CSn	32
DDR3E_DQ[31..0]	DDR3E_DQ[31..0]	32
DDR3E_DQS_N[3..0]	DDR3E_DQS_N[3..0]	32
DDR3E_DQS_P[3..0]	DDR3E_DQS_P[3..0]	32
DDR3E_ODT	DDR3E_ODT	32
DDR3E_RASn	DDR3E_RASn	32
DDR3E_RSTn	DDR3E_RSTn	32
DDR3E_WEn	DDR3E_WEn	32
DDR3F_A[13..0]	DDR3F_A[13..0]	19,32
DDR3F_CASN	DDR3F_CASN	32
DDR3F_CKE	DDR3F_CKE	32
DDR3F_DQ[31..0]	DDR3F_DQ[31..0]	32
DDR3F_DQS_N[3..0]	DDR3F_DQS_N[3..0]	32
DDR3F_DQS_P[3..0]	DDR3F_DQS_P[3..0]	32
DDR3F_RASN	DDR3F_RASN	32
DDR3F_RSTn	DDR3F_RSTn	32
DDR3F_WEN	DDR3F_WEN	32
DDR3F_BA[2..0]		25,32

QDR2_RZQIN — 100, 1% — R302

FPGA_USER_LED6 — FPGA_USER_LED6 38

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U38N

Stratix V GX Transceivers

5SGXA7_F1932
0.4 Preliminary

Bank QR0

SMA_RX_P0	BB2	GXB_RX_R0p,GXB_REFCLK_R0p	GXB_TX_R0p	AY6	SMA_TX_P0
SMA_RX_N0	BB1	GXB_RX_R0n,GXB_REFCLK_R0n	GXB_TX_R0n	AY5	SMA_TX_N0
SMA_RX_P1	BA4	GXB_RX_R1p,GXB_REFCLK_R1p	GXB_TX_R1p	AV6	SMA_TX_P1
SMA_RX_N1	BA3	GXB_RX_R1n,GXB_REFCLK_R1n	GXB_TX_R1n	AV5	SMA_TX_N1
QSFP0_RX_P0	AW4	GXB_RX_R2p,GXB_REFCLK_R2p	GXB_TX_R2p	AT6	QSFP0_TX_P0
QSFP0_RX_N0	AW3	GXB_RX_R2n,GXB_REFCLK_R2n	GXB_TX_R2n	AT5	QSFP0_TX_N0
QSFP0_RX_P1	AY2	GXB_RX_R3p,GXB_REFCLK_R3p	GXB_TX_R3p	AU4	QSFP0_TX_P1
QSFP0_RX_N1	AY1	GXB_RX_R3n,GXB_REFCLK_R3n	GXB_TX_R3n	AU3	QSFP0_TX_N1
QSFP0_RX_P2	AV2	GXB_RX_R4p,GXB_REFCLK_R4p	GXB_TX_R4p	AR4	QSFP0_TX_P2
QSFP0_RX_N2	AV1	GXB_RX_R4n,GXB_REFCLK_R4n	GXB_TX_R4n	AR3	QSFP0_TX_N2
QSFP0_RX_P3	AT2	GXB_RX_R5p,GXB_REFCLK_R5p	GXB_TX_R5p	AN4	QSFP0_TX_P3
QSFP0_RX_N3	AT1	GXB_RX_R5n,GXB_REFCLK_R5n	GXB_TX_R5n	AN3	QSFP0_TX_N3
REFCLK_CAP_QL0_P	AK7	REFCLK0Rp			
REFCLK_CAP_QL0_N	AK6	REFCLK0Rn			
REFCLKB_CAP_QL0_P	AH6	REFCLK1Rp			
REFCLKB_CAP_QL0_N	AH5	REFCLK1Rn			

Bank QR1

CFP_RX_P0	AP2	GXB_RX_R6p,GXB_REFCLK_R6p	GXB_TX_R6p	AL4	CFP_TX_P0
CFP_RX_N0	AP1	GXB_RX_R6n,GXB_REFCLK_R6n	GXB_TX_R6n	AL3	CFP_TX_N0
CFP_RX_P1	AM2	GXB_RX_R7p,GXB_REFCLK_R7p	GXB_TX_R7p	AJ4	CFP_TX_P1
CFP_RX_N1	AM1	GXB_RX_R7n,GXB_REFCLK_R7n	GXB_TX_R7n	AJ3	CFP_TX_N1
CFP_RX_P2	AK2	GXB_RX_R8p,GXB_REFCLK_R8p	GXB_TX_R8p	AG4	CFP_TX_P2
CFP_RX_N2	AK1	GXB_RX_R8n,GXB_REFCLK_R8n	GXB_TX_R8n	AG3	CFP_TX_N2
CFP_RX_P3	AH2	GXB_RX_R9p,GXB_REFCLK_R9p	GXB_TX_R9p	AE4	CFP_TX_P3
CFP_RX_N3	AH1	GXB_RX_R9n,GXB_REFCLK_R9n	GXB_TX_R9n	AE3	CFP_TX_N3
SFP0_RDp	AF2	GXB_RX_R10p,GXB_REFCLK_R10p	GXB_TX_R10p	AC4	SFP0_TDp
SFP0_RDn	AF1	GXB_RX_R10n,GXB_REFCLK_R10n	GXB_TX_R10n	AC3	SFP0_TDn
CFP_RX_P4	AD2	GXB_RX_R11p,GXB_REFCLK_R11p	GXB_TX_R11p	AA4	CFP_TX_P4
CFP_RX_N4	AD1	GXB_RX_R11n,GXB_REFCLK_R11n	GXB_TX_R11n	AA3	CFP_TX_N4
REFCLK_CAP_QL1_P	AF7	REFCLK2Rp			
REFCLK_CAP_QL1_N	AF6	REFCLK2Rn			
PRGCLK_QL1_P	AD6	REFCLK3Rp			
PRGCLK_QL1_N	AD5	REFCLK3Rn			

Bank QR2

CFP_RX_P5	AB2	GXB_RX_R12p,GXB_REFCLK_R12p	GXB_TX_R12p	W4	CFP_TX_P5
CFP_RX_N5	AB1	GXB_RX_R12n,GXB_REFCLK_R12n	GXB_TX_R12n	W3	CFP_TX_N5
CFP_RX_P6	Y2	GXB_RX_R13p,GXB_REFCLK_R13p	GXB_TX_R13p	U4	CFP_TX_P6
CFP_RX_N6	Y1	GXB_RX_R13n,GXB_REFCLK_R13n	GXB_TX_R13n	U3	CFP_TX_N6
CFP_RX_P7	V2	GXB_RX_R14p,GXB_REFCLK_R14p	GXB_TX_R14p	R4	CFP_TX_P7
CFP_RX_N7	V1	GXB_RX_R14n,GXB_REFCLK_R14n	GXB_TX_R14n	R3	CFP_TX_N7
CFP_RX_P8	T2	GXB_RX_R15p,GXB_REFCLK_R15p	GXB_TX_R15p	N4	CFP_TX_P8
CFP_RX_N8	T1	GXB_RX_R15n,GXB_REFCLK_R15n	GXB_TX_R15n	N3	CFP_TX_N8
SFP1_RDp	P2	GXB_RX_R16p,GXB_REFCLK_R16p	GXB_TX_R16p	L4	SFP1_TDp
SFP1_RDn	P1	GXB_RX_R16n,GXB_REFCLK_R16n	GXB_TX_R16n	L3	SFP1_TDn
CFP_RX_P9	M2	GXB_RX_R17p,GXB_REFCLK_R17p	GXB_TX_R17p	J4	CFP_TX_P9
CFP_RX_N9	M1	GXB_RX_R17n,GXB_REFCLK_R17n	GXB_TX_R17n	J3	CFP_TX_N9
REFCLK_CAP_QL2_P	AB6	REFCLK4Rp			
REFCLK_CAP_QL2_N	AB5	REFCLK4Rn			
REFCLKB_CAP_QL2_P	Y7	REFCLK5Rp			
REFCLKB_CAP_QL2_N	Y6	REFCLK5Rn			

Bank QR3

QSFP1_RX_P0	K2	GXB_RX_R18p,GXB_REFCLK_R18p	GXB_TX_R18p	K6	QSFP1_TX_P0
QSFP1_RX_N0	K1	GXB_RX_R18n,GXB_REFCLK_R18n	GXB_TX_R18n	K5	QSFP1_TX_N0
QSFP1_RX_P1	H2	GXB_RX_R19p,GXB_REFCLK_R19p	GXB_TX_R19p	H6	QSFP1_TX_P1
QSFP1_RX_N1	H1	GXB_RX_R19n,GXB_REFCLK_R19n	GXB_TX_R19n	H5	QSFP1_TX_N1
QSFP1_RX_P2	F2	GXB_RX_R20p,GXB_REFCLK_R20p	GXB_TX_R20p	G4	QSFP1_TX_P2
QSFP1_RX_N2	F1	GXB_RX_R20n,GXB_REFCLK_R20n	GXB_TX_R20n	G3	QSFP1_TX_N2
QSFP1_RX_P3	D2	GXB_RX_R21p,GXB_REFCLK_R21p	GXB_TX_R21p	E4	QSFP1_TX_P3
QSFP1_RX_N3	D1	GXB_RX_R21n,GXB_REFCLK_R21n	GXB_TX_R21n	E3	QSFP1_TX_N3
SFP2_RDp	B2	GXB_RX_R22p,GXB_REFCLK_R22p	GXB_TX_R22p	F6	SFP2_TDp
SFP2_RDn	B1	GXB_RX_R22n,GXB_REFCLK_R22n	GXB_TX_R22n	F5	SFP2_TDn
SFP3_RDp	C4	GXB_RX_R23p,GXB_REFCLK_R23p	GXB_TX_R23p	D6	SFP3_TDp
SFP3_RDn	C3	GXB_RX_R23n,GXB_REFCLK_R23n	GXB_TX_R23n	D5	SFP3_TDn
REFCLK_CAP_QL3_P	V6	REFCLK6Rp			
REFCLK_CAP_QL3_N	V5	REFCLK6Rn			
SMA_REFCLK_CAP_P	T7	REFCLK7Rp			
SMA_REFCLK_CAP_N	T6	REFCLK7Rn			
R294 2.00K	A4	RREF_TR	RREF_BR	BD2	R345 2.00K

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35 CFP_RX_P[9..0] → CFP_RX_P[9..0]
35 CFP_RX_N[9..0] → CFP_RX_N[9..0]

REFCLK_QL0_P / REFCLK_QL0_N → REFCLK_QL0_P 18 / REFCLK_QL0_N 18
REFCLK_QL1_P / REFCLK_QL1_N → REFCLK_QL1_P 18 / REFCLK_QL1_N 18
REFCLK_QL2_P / REFCLK_QL2_N → REFCLK_QL2_P 18 / REFCLK_QL2_N 18
REFCLK_QL3_P / REFCLK_QL3_N → REFCLK_QL3_P 18 / REFCLK_QL3_N 18
REFCLKB_CAP_QL0_P / REFCLKB_CAP_QL0_N → REFCLKB_CAP_QL0_P 16 / REFCLKB_CAP_QL0_N 16
REFCLKB_CAP_QL2_P / REFCLKB_CAP_QL2_N → REFCLKB_CAP_QL2_P 16 / REFCLKB_CAP_QL2_N 16

REFCLK_QL0_P 0.1uF C146 REFCLK_CAP_QL0_P
REFCLK_QL0_N 0.1uF C145 REFCLK_CAP_QL0_N
REFCLK_QL1_P 0.1uF C160 REFCLK_CAP_QL1_P
REFCLK_QL1_N 0.1uF C159 REFCLK_CAP_QL1_N
REFCLK_QL2_P 0.1uF C157 REFCLK_CAP_QL2_P
REFCLK_QL2_N 0.1uF C158 REFCLK_CAP_QL2_N
REFCLK_QL3_P 0.1uF C155 REFCLK_CAP_QL3_P
REFCLK_QL3_N 0.1uF C156 REFCLK_CAP_QL3_N
PRGCLK_QL1_P 0.1uF C212 PRGCLK_CAP_QL1_P
PRGCLK_QL1_N 0.1uF C211 PRGCLK_CAP_QL1_N

J32: LTI-SASF546-P26-X1 — 1 SMA_C_RX_P0 0.1uF C236 SMA_RX_P0
J37: LTI-SASF546-P26-X1 — 1 SMA_C_RX_N0 0.1uF C237 SMA_RX_N0
J30: LTI-SASF546-P26-X1 — 1 SMA_C_RX_P1 0.1uF C234 SMA_RX_P1
J35: LTI-SASF546-P26-X1 — 1 SMA_C_RX_N1 0.1uF C235 SMA_RX_N1

VCXOA_UP / VCXOA_DN — R52 4.99K / R51 4.99K — SDI_CLK_CTL
R50 180K, C217 0.001uF
From FPGA
2.5V — C213 0.1uF, C210 0.1uF, C218 0.1uF

2.5V — R48 10.0K, R49 10.0K
SDI_CLK_CTL
CLK_SFP_SEL
VCXOA_SDA
VCXOA_SCL
U39 SI552_570: VC, FS_OE, NC_SDA, NC_SCL, GND, VCC, CLK-, CLK+
2.5V
PRGCLK_CAP_QL1_N
PRGCLK_CAP_QL1_P
From EPM2210

SFP0_RDp / SFP0_RDn (34) ↔ SFP0_TDp / SFP0_TDn (34)
SFP1_RDp / SFP1_RDn (34) ↔ SFP1_TDp / SFP1_TDn (34)
SFP2_RDp / SFP2_RDn (34) ↔ SFP2_TDp / SFP2_TDn (34)
SFP3_RDp / SFP3_RDn (34) ↔ SFP3_TDp / SFP3_TDn (34)

QSFP0_RX_P[3..0] → QSFP0_RX_P[3..0]83
QSFP0_RX_N[3..0] → QSFP0_RX_N[3..0]83
QSFP0_TX_P[3..0] ← QSFP0_TX_P[3..0]33
QSFP0_TX_N[3..0] ← QSFP0_TX_N[3..0]33
QSFP1_RX_P[3..0] → QSFP1_RX_P[3..0]83
QSFP1_RX_N[3..0] → QSFP1_RX_N[3..0]83
QSFP1_TX_P[3..0] ← QSFP1_TX_P[3..0]33
QSFP1_TX_N[3..0] ← QSFP1_TX_N[3..0]33

CFP_TX_P[9..0] ← CFP_TX_P[9..0] 35
CFP_TX_N[9..0] ← CFP_TX_N[9..0] 35

J31: LTI-SASF546-P26-X1 — SMA_TX_P0 1
J36: LTI-SASF546-P26-X1 — SMA_TX_N0 1
J29: LTI-SASF546-P26-X1 — SMA_TX_P1 1
J34: LTI-SASF546-P26-X1 — SMA_TX_N1 1

J18: LTI-SASF546-P26-X1 — 1 SMA_REFCLK_P 0.1uF C152 SMA_REFCLK_CAP_P
J22: LTI-SASF546-P26-X1 — 1 SMA_REFCLK_N 0.1uF C153 SMA_REFCLK_CAP_N

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INT_CAP_RX_P5	BB43	GXB_RX_L0p,GXB_REFCLK_L0p	Bank QL0	GXB_TX_L0p	AY39	INT_TX_P5
INT_CAP_RX_N5	BB44	GXB_RX_L0n,GXB_REFCLK_L0n		GXB_TX_L0n	AY40	INT_TX_N5
INT_CAP_RX_P11	BA41	GXB_RX_L1p,GXB_REFCLK_L1p		GXB_TX_L1p	AV39	INT_TX_P11
INT_CAP_RX_N11	BA42	GXB_RX_L1n,GXB_REFCLK_L1n		GXB_TX_L1n	AV40	INT_TX_N11
INT_CAP_RX_P9	AW41	GXB_RX_L2p,GXB_REFCLK_L2p		GXB_TX_L2p	AT39	INT_TX_P9
INT_CAP_RX_N9	AW42	GXB_RX_L2n,GXB_REFCLK_L2n		GXB_TX_L2n	AT40	INT_TX_N9
INT_CAP_RX_P4	AY43	GXB_RX_L3p,GXB_REFCLK_L3p		GXB_TX_L3p	AU41	INT_TX_P4
INT_CAP_RX_N4	AY44	GXB_RX_L3n,GXB_REFCLK_L3n		GXB_TX_L3n	AU42	INT_TX_N4
INT_CAP_RX_P6	AV43	GXB_RX_L4p,GXB_REFCLK_L4p		GXB_TX_L4p	AR41	INT_TX_P6
INT_CAP_RX_N6	AV44	GXB_RX_L4n,GXB_REFCLK_L4n		GXB_TX_L4n	AR42	INT_TX_N6
INT_CAP_RX_P8	AT43	GXB_RX_L5p,GXB_REFCLK_L5p		GXB_TX_L5p	AN41	INT_TX_P8
INT_CAP_RX_N8	AT44	GXB_RX_L5n,GXB_REFCLK_L5n		GXB_TX_L5n	AN42	INT_TX_N8
REFCLK_CAP_QR0_P	AK38	REFCLK0Lp				
REFCLK_CAP_QR0_N	AK39	REFCLK0Ln				
	AH39	REFCLK1Lp				
	AH40	REFCLK1Ln				
INT_CAP_RX_P7	AP43	GXB_RX_L6p,GXB_REFCLK_L6p	Bank QL1	GXB_TX_L6p	AL41	INT_TX_P7
INT_CAP_RX_N7	AP44	GXB_RX_L6n,GXB_REFCLK_L6n		GXB_TX_L6n	AL42	INT_TX_N7
INT_CAP_RX_P10	AM43	GXB_RX_L7p,GXB_REFCLK_L7p		GXB_TX_L7p	AJ41	INT_TX_P10
INT_CAP_RX_N10	AM44	GXB_RX_L7n,GXB_REFCLK_L7n		GXB_TX_L7n	AJ42	INT_TX_N10
INT_CAP_RX_P1	AK43	GXB_RX_L8p,GXB_REFCLK_L8p		GXB_TX_L8p	AG41	INT_TX_P1
INT_CAP_RX_N1	AK44	GXB_RX_L8n,GXB_REFCLK_L8n		GXB_TX_L8n	AG42	INT_TX_N1
INT_CAP_RX_P0	AH43	GXB_RX_L9p,GXB_REFCLK_L9p		GXB_TX_L9p	AE41	INT_TX_P0
INT_CAP_RX_N0	AH44	GXB_RX_L9n,GXB_REFCLK_L9n		GXB_TX_L9n	AE42	INT_TX_N0
INT_CAP_RX_P2	AF43	GXB_RX_L10p,GXB_REFCLK_L10p		GXB_TX_L10p	AC41	INT_TX_P2
INT_CAP_RX_N2	AF44	GXB_RX_L10n,GXB_REFCLK_L10n		GXB_TX_L10n	AC42	INT_TX_N2
INT_CAP_RX_P3	AD43	GXB_RX_L11p,GXB_REFCLK_L11p		GXB_TX_L11p	AA41	INT_TX_P3
INT_CAP_RX_N3	AD44	GXB_RX_L11n,GXB_REFCLK_L11n		GXB_TX_L11n	AA42	INT_TX_N3
REFCLK_CAP_QR1_P	AF38	REFCLK2Lp				
REFCLK_CAP_QR1_N	AF39	REFCLK2Ln				
	AD39	REFCLK3Lp				
	AD40	REFCLK3Ln				
INT_CAP_RX_P17	AB43	GXB_RX_L12p,GXB_REFCLK_L12p	Bank QL2	GXB_TX_L12p	W41	INT_TX_P17
INT_CAP_RX_N17	AB44	GXB_RX_L12n,GXB_REFCLK_L12n		GXB_TX_L12n	W42	INT_TX_N17
INT_CAP_RX_P23	Y43	GXB_RX_L13p,GXB_REFCLK_L13p		GXB_TX_L13p	U41	INT_TX_P23
INT_CAP_RX_N23	Y44	GXB_RX_L13n,GXB_REFCLK_L13n		GXB_TX_L13n	U42	INT_TX_N23
INT_CAP_RX_P16	V43	GXB_RX_L14p,GXB_REFCLK_L14p		GXB_TX_L14p	R41	INT_TX_P16
INT_CAP_RX_N16	V44	GXB_RX_L14n,GXB_REFCLK_L14n		GXB_TX_L14n	R42	INT_TX_N16
INT_CAP_RX_P21	T43	GXB_RX_L15p,GXB_REFCLK_L15p		GXB_TX_L15p	N41	INT_TX_P21
INT_CAP_RX_N21	T44	GXB_RX_L15n,GXB_REFCLK_L15n		GXB_TX_L15n	N42	INT_TX_N21
INT_CAP_RX_P18	P43	GXB_RX_L16p,GXB_REFCLK_L16p		GXB_TX_L16p	L41	INT_TX_P18
INT_CAP_RX_N18	P44	GXB_RX_L16n,GXB_REFCLK_L16n		GXB_TX_L16n	L42	INT_TX_N18
INT_CAP_RX_P20	M43	GXB_RX_L17p,GXB_REFCLK_L17p		GXB_TX_L17p	J41	INT_TX_P20
INT_CAP_RX_N20	M44	GXB_RX_L17n,GXB_REFCLK_L17n		GXB_TX_L17n	J42	INT_TX_N20
REFCLK_CAP_QR2_P	AB39	REFCLK4Lp				
REFCLK_CAP_QR2_N	AB40	REFCLK4Ln				
	Y38	REFCLK5Lp				
	Y39	REFCLK5Ln				
INT_CAP_RX_P19	K43	GXB_RX_L18p,GXB_REFCLK_L18p	Bank QL3	GXB_TX_L18p	K39	INT_TX_P19
INT_CAP_RX_N19	K44	GXB_RX_L18n,GXB_REFCLK_L18n		GXB_TX_L18n	K40	INT_TX_N19
INT_CAP_RX_P22	H43	GXB_RX_L19p,GXB_REFCLK_L19p		GXB_TX_L19p	H39	INT_TX_P22
INT_CAP_RX_N22	H44	GXB_RX_L19n,GXB_REFCLK_L19n		GXB_TX_L19n	H40	INT_TX_N22
INT_CAP_RX_P13	F43	GXB_RX_L20p,GXB_REFCLK_L20p		GXB_TX_L20p	G41	INT_TX_P13
INT_CAP_RX_N13	F44	GXB_RX_L20n,GXB_REFCLK_L20n		GXB_TX_L20n	G42	INT_TX_N13
INT_CAP_RX_P14	D43	GXB_RX_L21p,GXB_REFCLK_L21p		GXB_TX_L21p	E41	INT_TX_P14
INT_CAP_RX_N14	D44	GXB_RX_L21n,GXB_REFCLK_L21n		GXB_TX_L21n	E42	INT_TX_N14
INT_CAP_RX_P12	B43	GXB_RX_L22p,GXB_REFCLK_L22p		GXB_TX_L22p	F39	INT_TX_P12
INT_CAP_RX_N12	B44	GXB_RX_L22n,GXB_REFCLK_L22n		GXB_TX_L22n	F40	INT_TX_N12
INT_CAP_RX_P15	C41	GXB_RX_L23p,GXB_REFCLK_L23p		GXB_TX_L23p	D39	INT_TX_P15
INT_CAP_RX_N15	C42	GXB_RX_L23n,GXB_REFCLK_L23n		GXB_TX_L23n	D40	INT_TX_N15
REFCLK_CAP_QR3_P	V39	REFCLK6Lp				
REFCLK_CAP_QR3_N	V40	REFCLK6Ln				
	T38	REFCLK7Lp				
	T39	REFCLK7Ln				
R293 2.00K	A41	RREF_TL		RREF_BL	BD43	R344 2.00K

5SGXA7_F1932
0.4 Preliminary

10.0K R301

INT_RX_P[23..0] 37 → INT_RX_P[23..0]
INT_RX_N[23..0] 37 → INT_RX_N[23..0]

INT_TX_P[23..0] → INT_TX_P[23..0] 37
INT_TX_N[23..0] → INT_TX_N[23..0] 37

INT_MSB_CON_TX_CLK_P → INT_MSB_CON_TX_CLK_P 37
INT_MSB_CON_TX_CLK_N → INT_MSB_CON_TX_CLK_N 37

INT_LSB_CON_TX_CLK_P → INT_LSB_CON_TX_CLK_P 37
INT_LSB_CON_TX_CLK_N → INT_LSB_CON_TX_CLK_N 37

REFCLK_QR0_P → REFCLK_QR0_P 18
REFCLK_QR0_N → REFCLK_QR0_N 18

REFCLK_QR3_P → REFCLK_QR3_P 18
REFCLK_QR3_N → REFCLK_QR3_N 18

INT_LSB_CON_TX_CLK_P 1 — J58
INT_LSB_CON_TX_CLK_N 1 — J63

INT_MSB_CON_TX_CLK_P 1 — J20
INT_MSB_CON_TX_CLK_N 1 — J23

INT_RX_P0	0.1uF	C691 INT_CAP_RX_P0
INT_RX_N0	0.1uF	C692 INT_CAP_RX_N0
INT_RX_P1	0.1uF	C701 INT_CAP_RX_P1
INT_RX_N1	0.1uF	C702 INT_CAP_RX_N1
INT_RX_P2	0.1uF	C684 INT_CAP_RX_P2
INT_RX_N2	0.1uF	C685 INT_CAP_RX_N2
INT_RX_P3	0.1uF	C675 INT_CAP_RX_P3
INT_RX_N3	0.1uF	C676 INT_CAP_RX_N3
INT_RX_P4	0.1uF	C730 INT_CAP_RX_P4
INT_RX_N4	0.1uF	C731 INT_CAP_RX_N4
INT_RX_P5	0.1uF	C732 INT_CAP_RX_P5
INT_RX_N5	0.1uF	C733 INT_CAP_RX_N5
INT_RX_P6	0.1uF	C714 INT_CAP_RX_P6
INT_RX_N6	0.1uF	C715 INT_CAP_RX_N6
INT_RX_P7	0.1uF	C712 INT_CAP_RX_P7
INT_RX_N7	0.1uF	C713 INT_CAP_RX_N7
INT_RX_P8	0.1uF	C716 INT_CAP_RX_P8
INT_RX_N8	0.1uF	C717 INT_CAP_RX_N8
INT_RX_P9	0.1uF	C710 INT_CAP_RX_P9
INT_RX_N9	0.1uF	C711 INT_CAP_RX_N9
INT_RX_P10	0.1uF	C699 INT_CAP_RX_P10
INT_RX_N10	0.1uF	C700 INT_CAP_RX_N10
INT_RX_P11	0.1uF	C728 INT_CAP_RX_P11
INT_RX_N11	0.1uF	C729 INT_CAP_RX_N11
INT_RX_P12	0.1uF	C525 INT_CAP_RX_P12
INT_RX_N12	0.1uF	C526 INT_CAP_RX_N12
INT_RX_P13	0.1uF	C407 INT_CAP_RX_P13
INT_RX_N13	0.1uF	C406 INT_CAP_RX_N13
INT_RX_P14	0.1uF	C527 INT_CAP_RX_P14
INT_RX_N14	0.1uF	C537 INT_CAP_RX_N14
INT_RX_P15	0.1uF	C538 INT_CAP_RX_P15
INT_RX_N15	0.1uF	C539 INT_CAP_RX_N15
INT_RX_P16	0.1uF	C358 INT_CAP_RX_P16
INT_RX_N16	0.1uF	C359 INT_CAP_RX_N16
INT_RX_P17	0.1uF	C356 INT_CAP_RX_P17
INT_RX_N17	0.1uF	C357 INT_CAP_RX_N17
INT_RX_P18	0.1uF	C362 INT_CAP_RX_P18
INT_RX_N18	0.1uF	C363 INT_CAP_RX_N18
INT_RX_P19	0.1uF	C404 INT_CAP_RX_P19
INT_RX_N19	0.1uF	C405 INT_CAP_RX_N19
INT_RX_P20	0.1uF	C373 INT_CAP_RX_P20
INT_RX_N20	0.1uF	C372 INT_CAP_RX_N20
INT_RX_P21	0.1uF	C360 INT_CAP_RX_P21
INT_RX_N21	0.1uF	C361 INT_CAP_RX_N21
INT_RX_P22	0.1uF	C451 INT_CAP_RX_P22
INT_RX_N22	0.1uF	C450 INT_CAP_RX_N22
INT_RX_P23	0.1uF	C354 INT_CAP_RX_P23
INT_RX_N23	0.1uF	C355 INT_CAP_RX_N23

REFCLK_QR1_P → REFCLK_QR1_P
REFCLK_QR1_N → REFCLK_QR1_N
REFCLK_QR2_P → REFCLK_QR2_P
REFCLK_QR2_N → REFCLK_QR2_N

REFCLK_QR0_P	0.1uF	C267 REFCLK_CAP_QR0_P
REFCLK_QR0_N	0.1uF	C268 REFCLK_CAP_QR0_N
REFCLK_QR1_P	0.1uF	C263 REFCLK_CAP_QR1_P
REFCLK_QR1_N	0.1uF	C264 REFCLK_CAP_QR1_N
REFCLK_QR2_P	0.1uF	C265 REFCLK_CAP_QR2_P
REFCLK_QR2_N	0.1uF	C266 REFCLK_CAP_QR2_N
REFCLK_QR3_P	0.1uF	C269 REFCLK_CAP_QR3_P
REFCLK_QR3_N	0.1uF	C270 REFCLK_CAP_QR3_N

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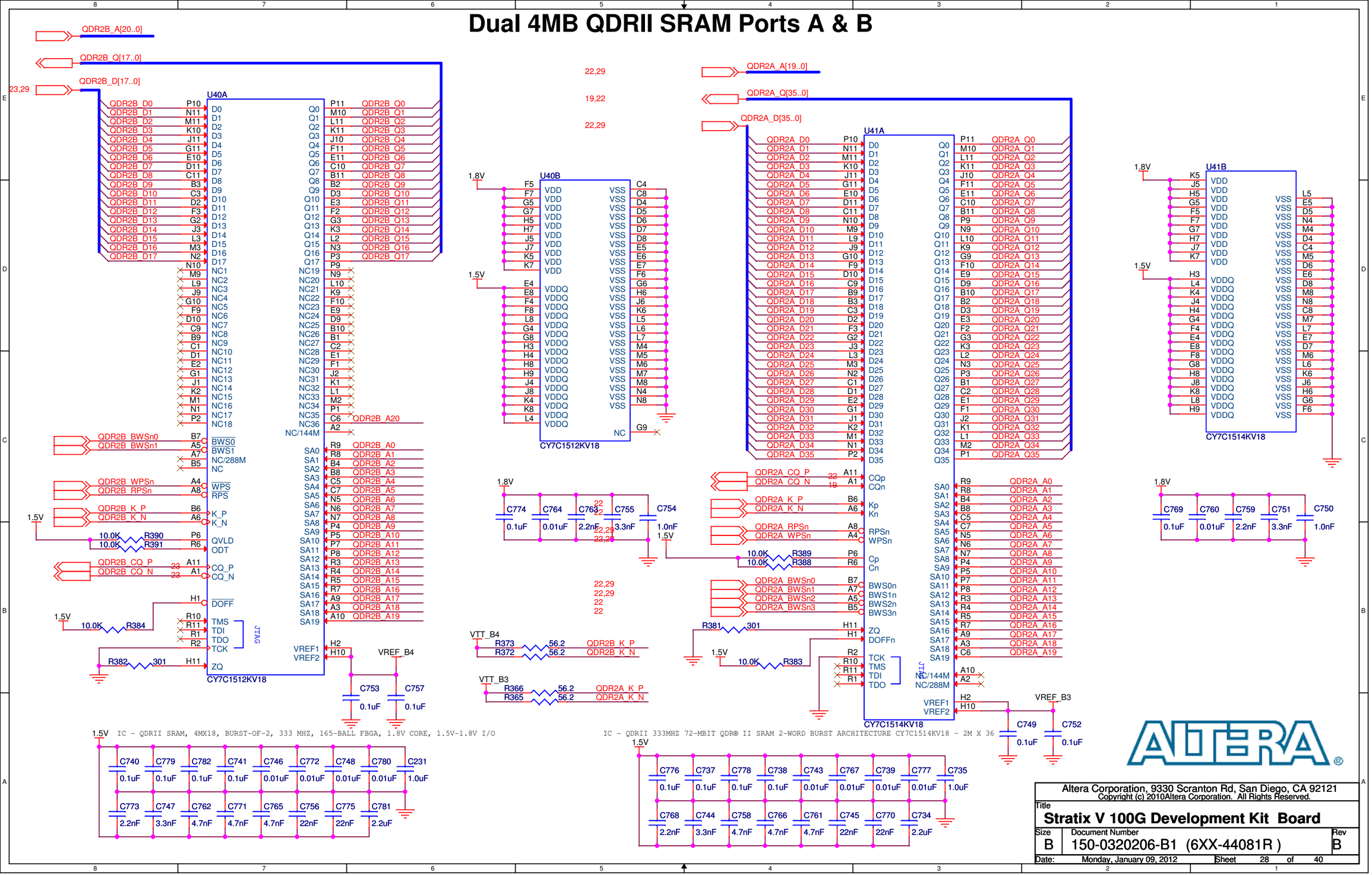
Dual 4MB QDRII SRAM Ports A & B



IC - QDRII SRAM, 4MX18, BURST-OF-2, 333 MHZ, 165-BALL FBGA, 1.8V CORE, 1.5V-1.8V I/O

IC - QDRII 333MHZ 72-MBIT QDR® II SRAM 2-WORD BURST ARCHITECTURE CY7C1514KV18 - 2M X 36

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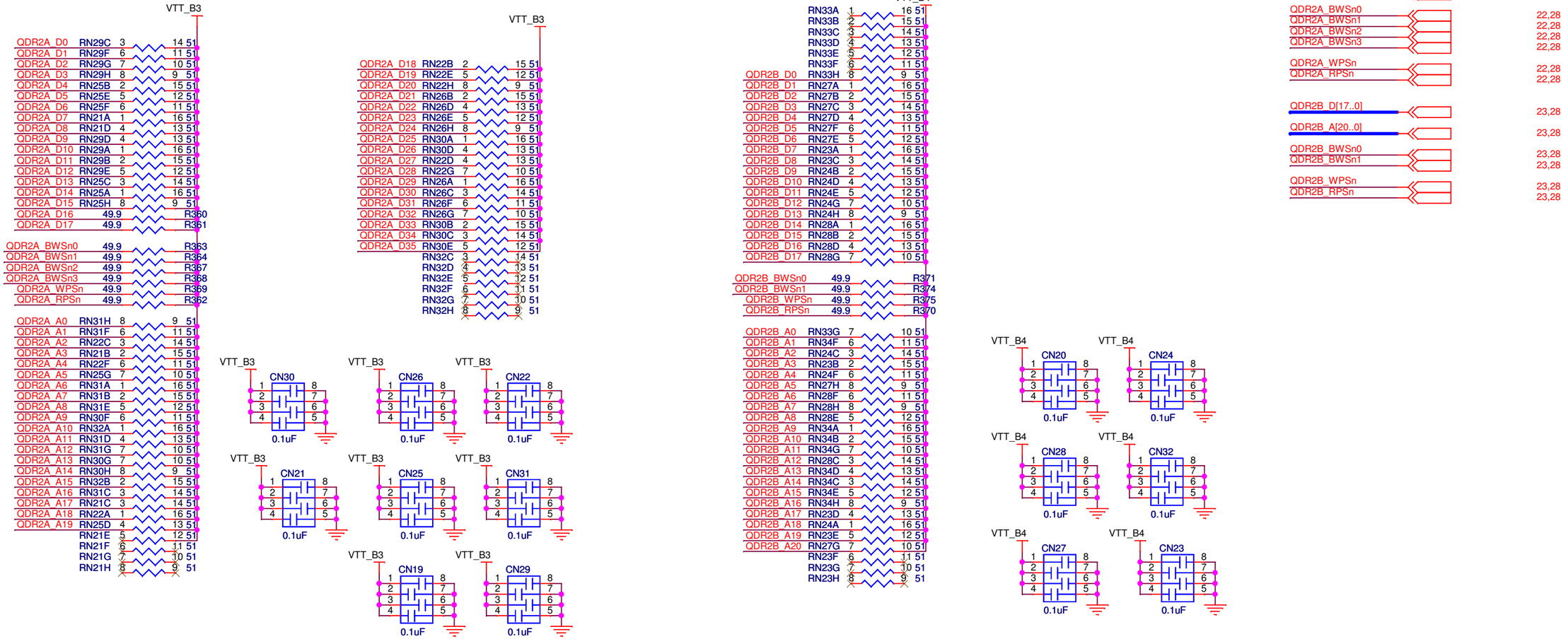
QDRII MEMORY TERMINATION



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512MB DDR3 PortS A & B

DDR3A_BA[2..0]
DDR3A_DQS_P[3..0] 24
DDR3A_DQS_N[3..0] 24
DDR3B_BA[2..0]
DDR3B_DQS_P[3..0] 24
DDR3B_DQS_N[3..0] 24

DDR3A_CK_P — 100, 1% — R274 — DDR3A_CK_N
DDR3B_CK_P — 100, 1% — R273 — DDR3B_CK_N

Note: ADDR/CMD signals daisy chain

VTT_DDR3 — CN3, CN6, CN1, CN14, CN9, CN2 — 0.1uF

DDR3A_A0	RN20B 2	15 51	DDR3A_CSn	RN20G 7	10 51	DDR3B_A0	RN17B 2	15 51	DDR3B_CSn	RN17G 7	10 51
DDR3A_A1	RN19C 3	14 51	DDR3A_WEn	RN20D 4	13 51	DDR3B_A1	RN16C 3	14 51	DDR3B_WEn	RN17D 4	13 51
DDR3A_A2	RN19G 7	10 51	DDR3A_RASn	RN20C 3	14 51	DDR3B_A2	RN16G 7	10 51	DDR3B_RASn	RN17C 3	14 51
DDR3A_A3	RN20F 6	11 51	DDR3A_BA0	RN20E 5	12 51	DDR3B_A3	RN17F 6	11 51	DDR3B_BA0	RN17E 5	12 51
DDR3A_A4	RN19A 1	16 51	DDR3A_BA1	RN19B 2	15 51	DDR3B_A4	RN16A 1	16 51	DDR3B_BA1	RN16B 2	15 51
DDR3A_A5	RN18H 8	9 51	DDR3A_BA2	RN19H 8	9 51	DDR3B_A5	RN15H 8	9 51	DDR3B_BA2	RN16H 8	9 51
DDR3A_A6	RN18G 7	10 51	DDR3A_CASn	RN20A 1	16 51	DDR3B_A6	RN15G 7	10 51	DDR3B_CASn	RN17A 1	16 51
DDR3A_A7	RN18A 1	16 51	DDR3A_ODT	RN20H 8	9 51	DDR3B_A7	RN15A 1	16 51	DDR3B_ODT	RN17H 8	9 51
DDR3A_A8	RN18E 5	12 51	DDR3A_A12	RN19E 5	12 51	DDR3B_A8	RN15E 5	12 51	DDR3B_A12	RN16E 5	12 51
DDR3A_A9	RN18D 4	13 51	DDR3A_A13	RN18C 3	14 51	DDR3B_A9	RN15D 4	13 51	DDR3B_A13	RN15C 3	14 51
DDR3A_A10	RN19F 6	11 51	DDR3A_RSTn	RN18B 2	15 51	DDR3B_A10	RN16F 6	11 51	DDR3B_RSTn	RN15B 2	15 51
DDR3A_A11	RN18F 6	11 51	DDR3A_CKE	RN19D 4	13 51	DDR3B_A11	RN15F 6	11 51	DDR3B_CKE	RN16D 4	13 51

DDR3A_DQ[31..0] 24
DDR3A_A[13..0]
DDR3B_A[13..0]
DDR3B_DQ[31..0] 24

U31, U24, U32, U25 — DDR3 Device — MT41J128M16HA

U31	U24	U32	U25
DDR3A_A0 N3	DDR3A_A0 N3	DDR3B_A0 N3	DDR3B_A0 N3
DDR3A_A1 P7	DDR3A_A1 P7	DDR3B_A1 P7	DDR3B_A1 P7
DDR3A_A2 P3	DDR3A_A2 P3	DDR3B_A2 P3	DDR3B_A2 P3
DDR3A_A3 N2	DDR3A_A3 N2	DDR3B_A3 N2	DDR3B_A3 N2
DDR3A_A4 P8	DDR3A_A4 P8	DDR3B_A4 P8	DDR3B_A4 P8
DDR3A_A5 P2	DDR3A_A5 P2	DDR3B_A5 P2	DDR3B_A5 P2
DDR3A_A6 R8	DDR3A_A6 R8	DDR3B_A6 R8	DDR3B_A6 R8
DDR3A_A7 R2	DDR3A_A7 R2	DDR3B_A7 R2	DDR3B_A7 R2
DDR3A_A8 T8	DDR3A_A8 T8	DDR3B_A8 T8	DDR3B_A8 T8
DDR3A_A9 R3	DDR3A_A9 R3	DDR3B_A9 R3	DDR3B_A9 R3
DDR3A_A10 L7	DDR3A_A10 L7	DDR3B_A10 L7	DDR3B_A10 L7
DDR3A_A11 R7	DDR3A_A11 R7	DDR3B_A11 R7	DDR3B_A11 R7
DDR3A_A12 N7	DDR3A_A12 N7	DDR3B_A12 N7	DDR3B_A12 N7
DDR3A_A13 T3	DDR3A_A13 T3	DDR3B_A13 T3	DDR3B_A13 T3
DDR3A_CKE K9	DDR3A_CKE K9	DDR3B_CKE K9	DDR3B_CKE K9
DDR3A_CK_P J7	DDR3A_CK_P J7	DDR3B_CK_P J7	DDR3B_CK_P J7
DDR3A_CK_N K7	DDR3A_CK_N K7	DDR3B_CK_N K7	DDR3B_CK_N K7
DDR3A_CSn L2	DDR3A_CSn L2	DDR3B_CSn L2	DDR3B_CSn L2
DDR3A_WEn L3	DDR3A_WEn L3	DDR3B_WEn L3	DDR3B_WEn L3
DDR3A_RASn J3	DDR3A_RASn J3	DDR3B_RASn J3	DDR3B_RASn J3
DDR3A_CASn K3	DDR3A_CASn K3	DDR3B_CASn K3	DDR3B_CASn K3
DDR3A_BA0 M2	DDR3A_BA0 M2	DDR3B_BA0 M2	DDR3B_BA0 M2
DDR3A_BA1 N8	DDR3A_BA1 N8	DDR3B_BA1 N8	DDR3B_BA1 N8
DDR3A_BA2 M3	DDR3A_BA2 M3	DDR3B_BA2 M3	DDR3B_BA2 M3
DDR3A_RSTn T2	DDR3A_RSTn T2	DDR3B_RSTn T2	DDR3B_RSTn T2
DDR3A_ODT K1	DDR3A_ODT K1	DDR3B_ODT K1	DDR3B_ODT K1
DDR3A_ZQ01 L8	DDR3A_ZQ02 L8	DDR3B_ZQ01 L8	DDR3B_ZQ02 L8
DDR3A_DQ0 E3	DDR3A_DQ16 E3	DDR3B_DQ0 E3	DDR3B_DQ16 E3
DDR3A_DQ1 F7	DDR3A_DQ17 F7	DDR3B_DQ1 F7	DDR3B_DQ17 F7
DDR3A_DQ2 F2	DDR3A_DQ18 F2	DDR3B_DQ2 F2	DDR3B_DQ18 F2
DDR3A_DQ3 F8	DDR3A_DQ19 F8	DDR3B_DQ3 F8	DDR3B_DQ19 F8
DDR3A_DQ4 H3	DDR3A_DQ20 H3	DDR3B_DQ4 H3	DDR3B_DQ20 H3
DDR3A_DQ5 H8	DDR3A_DQ21 H8	DDR3B_DQ5 H8	DDR3B_DQ21 H8
DDR3A_DQ6 G2	DDR3A_DQ22 G2	DDR3B_DQ6 G2	DDR3B_DQ22 G2
DDR3A_DQ7 H7	DDR3A_DQ23 H7	DDR3B_DQ7 H7	DDR3B_DQ23 H7
DDR3A_DQ8 D7	DDR3A_DQ24 D7	DDR3B_DQ8 D7	DDR3B_DQ24 D7
DDR3A_DQ9 C3	DDR3A_DQ25 C3	DDR3B_DQ9 C3	DDR3B_DQ25 C3
DDR3A_DQ10 C8	DDR3A_DQ26 C8	DDR3B_DQ10 C8	DDR3B_DQ26 C8
DDR3A_DQ11 C2	DDR3A_DQ27 C2	DDR3B_DQ11 C2	DDR3B_DQ27 C2
DDR3A_DQ12 A7	DDR3A_DQ28 A7	DDR3B_DQ12 A7	DDR3B_DQ28 A7
DDR3A_DQ13 A2	DDR3A_DQ29 A2	DDR3B_DQ13 A2	DDR3B_DQ29 A2
DDR3A_DQ14 B8	DDR3A_DQ30 B8	DDR3B_DQ14 B8	DDR3B_DQ30 B8
DDR3A_DQ15 A3	DDR3A_DQ31 A3	DDR3B_DQ15 A3	DDR3B_DQ31 A3
DDR3A_DQS_P0 F3	DDR3A_DQS_P2 F3	DDR3B_DQS_P0 F3	DDR3B_DQS_P2 F3
DDR3A_DQS_N0 G3	DDR3A_DQS_N2 G3	DDR3B_DQS_N0 G3	DDR3B_DQS_N2 G3
DDR3A_DQS_P1 C7	DDR3A_DQS_P3 C7	DDR3B_DQS_P1 C7	DDR3B_DQS_P3 C7
DDR3A_DQS_N1 B7	DDR3A_DQS_N3 B7	DDR3B_DQS_N1 B7	DDR3B_DQS_N3 B7

R280 240 — R267 240 — R279 240 — R266 240 — 1.5V

C395 C396 C401 C402 C439 C440 C446 C447 C513 C514 C520 C521 C477 C478 C483 C484 C486 C443 C517 C445 C438 C519 C448 C441 C522 C515 C476 C400
2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 3.3nF 3.3nF 4.7nF 4.7nF 4.7nF 0.01uF 0.01uF 0.01uF 0.01uF 0.01uF 0.01uF

C480 C482 C394 C485 C479 C518 C512 C437 C444 C403 C397 C398 C516 C523 C436 C399 C475 C481 C442 C449
0.01uF 0.01uF 0.01uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.47uF 0.47uF 0.47uF 0.47uF 0.47uF 0.47uF 0.47uF 0.47uF

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512MB DDR3 PortS C & D

DDR3C_BA[2..0]
DDR3C_DQS_P[3..0] 10,24
DDR3C_DQS_N[3..0] 10,24
DDR3D_BA[2..0]
DDR3D_DQS_P[3..0] 10,25
DDR3D_DQS_N[3..0] 10,25

DDR3C_CK_P — 100, 1% — R272 — DDR3C_CK_N
DDR3D_CK_P — 100, 1% — R271 — DDR3D_CK_N

Note: ADDR/CMD signals daisy chain

VTT_DDR3 — CN12, CN7, CN5, CN8, CN11, CN10 — 0.1uF

DDR3C_A0	RN14B	2	15	51	DDR3C_CSn	RN14G	7	10	51
DDR3C_A1	RN13C	3	14	51	DDR3C_WEn	RN14D	4	13	51
DDR3C_A2	RN13G	7	10	51	DDR3C_RASn	RN14C	3	14	51
DDR3C_A3	RN14F	6	11	51	DDR3C_BA0	RN14E	5	12	51
DDR3C_A4	RN13A	1	16	51	DDR3C_BA1	RN13B	2	15	51
DDR3C_A5	RN12H	8	9	51	DDR3C_BA2	RN13H	8	9	51
DDR3C_A6	RN12G	7	10	51	DDR3C_CASn	RN14A	1	16	51
DDR3C_A7	RN12A	1	16	51	DDR3C_ODT	RN14H	8	9	51
DDR3C_A8	RN12E	5	12	51	DDR3C_A12	RN13E	5	12	51
DDR3C_A9	RN12D	4	13	51	DDR3C_A13	RN12C	3	14	51
DDR3C_A10	RN13F	6	11	51	DDR3C_RSTn	RN12B	2	15	51
DDR3C_A11	RN12F	6	11	51	DDR3C_CKE	RN13D	4	13	51

DDR3D_A0	RN11B	2	15	51	DDR3D_CSn	RN11G	7	10	51
DDR3D_A1	RN10C	3	14	51	DDR3D_WEn	RN11D	4	13	51
DDR3D_A2	RN10G	7	10	51	DDR3D_RASn	RN11C	3	14	51
DDR3D_A3	RN11F	6	11	51	DDR3D_BA0	RN11E	5	12	51
DDR3D_A4	RN10A	1	16	51	DDR3D_BA1	RN10B	2	15	51
DDR3D_A5	RN9H	8	9	51	DDR3D_BA2	RN10H	8	9	51
DDR3D_A6	RN9G	7	10	51	DDR3D_CASn	RN11A	1	16	51
DDR3D_A7	RN9A	1	16	51	DDR3D_ODT	RN11H	8	9	51
DDR3D_A8	RN9E	5	12	51	DDR3D_A12	RN10E	5	12	51
DDR3D_A9	RN9D	4	13	51	DDR3D_A13	RN9C	3	14	51
DDR3D_A10	RN10F	6	11	51	DDR3D_RSTn	RN9B	2	15	51
DDR3D_A11	RN9F	6	11	51	DDR3D_CKE	RN10D	4	13	51

DDR3C_DQ[31..0] 10,24
DDR3C_A[13..0] 24,25
DDR3D_A[13..0] 24,25
DDR3D_DQ[31..0] 10,25

U33, U26, U34, U27 — DDR3 Device — MT41J128M16HA

Pin	U33	U26	U34	U27
A0	DDR3C_A0	DDR3C_A0	DDR3D_A0	DDR3D_A0
A1	DDR3C_A1	DDR3C_A1	DDR3D_A1	DDR3D_A1
A2	DDR3C_A2	DDR3C_A2	DDR3D_A2	DDR3D_A2
A3	DDR3C_A3	DDR3C_A3	DDR3D_A3	DDR3D_A3
A4	DDR3C_A4	DDR3C_A4	DDR3D_A4	DDR3D_A4
A5	DDR3C_A5	DDR3C_A5	DDR3D_A5	DDR3D_A5
A6	DDR3C_A6	DDR3C_A6	DDR3D_A6	DDR3D_A6
A7	DDR3C_A7	DDR3C_A7	DDR3D_A7	DDR3D_A7
A8	DDR3C_A8	DDR3C_A8	DDR3D_A8	DDR3D_A8
A9	DDR3C_A9	DDR3C_A9	DDR3D_A9	DDR3D_A9
A10/AP	DDR3C_A10	DDR3C_A10	DDR3D_A10	DDR3D_A10
A11	DDR3C_A11	DDR3C_A11	DDR3D_A11	DDR3D_A11
A12/BCn	DDR3C_A12	DDR3C_A12	DDR3D_A12	DDR3D_A12
A13	DDR3C_A13	DDR3C_A13	DDR3D_A13	DDR3D_A13
CKE	DDR3C_CKE	DDR3C_CKE	DDR3D_CKE	DDR3D_CKE
CK_P	DDR3C_CK_P	DDR3C_CK_P	DDR3D_CK_P	DDR3D_CK_P
CK_N	DDR3C_CK_N	DDR3C_CK_N	DDR3D_CK_N	DDR3D_CK_N
CS	DDR3C_CSn	DDR3C_CSn	DDR3D_CSn	DDR3D_CSn
WE	DDR3C_WEn	DDR3C_WEn	DDR3D_WEn	DDR3D_WEn
RAS	DDR3C_RASn	DDR3C_RASn	DDR3D_RASn	DDR3D_RASn
CAS	DDR3C_CASn	DDR3C_CASn	DDR3D_CASn	DDR3D_CASn
BA0	DDR3C_BA0	DDR3C_BA0	DDR3D_BA0	DDR3D_BA0
BA1	DDR3C_BA1	DDR3C_BA1	DDR3D_BA1	DDR3D_BA1
BA2	DDR3C_BA2	DDR3C_BA2	DDR3D_BA2	DDR3D_BA2
RESETn	DDR3C_RSTn	DDR3C_RSTn	DDR3D_RSTn	DDR3D_RSTn
ODT	DDR3C_ODT	DDR3C_ODT	DDR3D_ODT	DDR3D_ODT
ZQ	DDR3C_ZQ01	DDR3C_ZQ02	DDR3D_ZQ01	DDR3D_ZQ02
DQ0	DDR3C_DQ0	DDR3C_DQ16	DDR3D_DQ0	DDR3D_DQ16
DQ1	DDR3C_DQ1	DDR3C_DQ17	DDR3D_DQ1	DDR3D_DQ17
DQ2	DDR3C_DQ2	DDR3C_DQ18	DDR3D_DQ2	DDR3D_DQ18
DQ3	DDR3C_DQ3	DDR3C_DQ19	DDR3D_DQ3	DDR3D_DQ19
DQ4	DDR3C_DQ4	DDR3C_DQ20	DDR3D_DQ4	DDR3D_DQ20
DQ5	DDR3C_DQ5	DDR3C_DQ21	DDR3D_DQ5	DDR3D_DQ21
DQ6	DDR3C_DQ6	DDR3C_DQ22	DDR3D_DQ6	DDR3D_DQ22
DQ7	DDR3C_DQ7	DDR3C_DQ23	DDR3D_DQ7	DDR3D_DQ23
DQ8	DDR3C_DQ8	DDR3C_DQ24	DDR3D_DQ8	DDR3D_DQ24
DQ9	DDR3C_DQ9	DDR3C_DQ25	DDR3D_DQ9	DDR3D_DQ25
DQ10	DDR3C_DQ10	DDR3C_DQ26	DDR3D_DQ10	DDR3D_DQ26
DQ11	DDR3C_DQ11	DDR3C_DQ27	DDR3D_DQ11	DDR3D_DQ27
DQ12	DDR3C_DQ12	DDR3C_DQ28	DDR3D_DQ12	DDR3D_DQ28
DQ13	DDR3C_DQ13	DDR3C_DQ29	DDR3D_DQ13	DDR3D_DQ29
DQ14	DDR3C_DQ14	DDR3C_DQ30	DDR3D_DQ14	DDR3D_DQ30
DQ15	DDR3C_DQ15	DDR3C_DQ31	DDR3D_DQ15	DDR3D_DQ31
DQS_P0	DDR3C_DQS_P0	DDR3C_DQS_P2	DDR3D_DQS_P0	DDR3D_DQS_P2
DQS_N0	DDR3C_DQS_N0	DDR3C_DQS_N2	DDR3D_DQS_N0	DDR3D_DQS_N2
DQS_P1	DDR3C_DQS_P1	DDR3C_DQS_P3	DDR3D_DQS_P1	DDR3D_DQS_P3
DQS_N1	DDR3C_DQS_N1	DDR3C_DQS_N3	DDR3D_DQS_N1	DDR3D_DQS_N3
VREFDQ	R278 240	R265 240	R277 240	R264 240
VREFCA				

1.5V

C391 C416 C417 C433 C432 C460 C461 C472 C473 C393 C381 C382 C390 C495 C496 C508 C509 C505 C420 C494 C507 C431 C421 C459 C471 C380 C389 C497
2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 2.2nF 3.3nF 3.3nF 4.7nF 4.7nF 4.7nF 0.01uF 0.01uF 0.01uF 0.01uF 0.01uF 0.01uF

1.5V

C510 C418 C434 C493 C462 C474 C392 C383 C463 C415 C506 C430 C379 C458 C470 C429 C498 C511 C419 C435
0.01uF 0.01uF 0.01uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.47uF 0.47uF 0.47uF 0.47uF 0.47uF 0.47uF 0.47uF 0.47uF

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512MB DDR3 PortS E & F

DDR3E_BA[2..0]
DDR3E_DQS_P[3..0] 25
DDR3E_DQS_N[3..0] 25
DDR3F_BA[2..0]
DDR3F_DQS_P[3..0] 25
DDR3F_DQS_N[3..0] 25

DDR3E_CK_P — 100, 1% — R270 — DDR3E_CK_N
DDR3F_CK_P — 100, 1% — R269 — DDR3F_CK_N

Note: ADDR/CMD signals daisy chain

VTT_DDR3: CN15, CN18, CN17, CN16, CN13, CN4 — 0.1uF

DDR3E_A0	RN8B	2	15 51	DDR3E_CSn	RN8G	7	10 51	DDR3F_A0	RN5B	2	15 51	DDR3F_CSn	RN5G	7	10 51
DDR3E_A1	RN7C	3	14 51	DDR3E_WEn	RN8D	4	13 51	DDR3F_A1	RN4C	3	14 51	DDR3F_WEn	RN5D	4	13 51
DDR3E_A2	RN7G	7	10 51	DDR3E_RASn	RN8C	3	14 51	DDR3F_A2	RN4G	7	10 51	DDR3F_RASn	RN5C	3	14 51
DDR3E_A3	RN8F	6	11 51	DDR3E_BA0	RN8E	5	12 51	DDR3F_A3	RN5F	6	11 51	DDR3F_BA0	RN5E	5	12 51
DDR3E_A4	RN7A	1	16 51	DDR3E_BA1	RN7B	2	15 51	DDR3F_A4	RN4A	1	16 51	DDR3F_BA1	RN4B	2	15 51
DDR3E_A5	RN6H	8	9 51	DDR3E_BA2	RN7H	8	9 51	DDR3F_A5	RN3H	8	9 51	DDR3F_BA2	RN4H	8	9 51
DDR3E_A6	RN6G	7	10 51	DDR3E_CASn	RN8A	1	16 51	DDR3F_A6	RN3G	7	10 51	DDR3F_CASn	RN5A	1	16 51
DDR3E_A7	RN6A	1	16 51	DDR3E_ODT	RN8H	8	9 51	DDR3F_A7	RN3A	1	16 51	DDR3F_ODT	RN5H	8	9 51
DDR3E_A8	RN6E	5	12 51	DDR3E_A12	RN7E	5	12 51	DDR3F_A8	RN3E	5	12 51	DDR3F_A12	RN4E	5	12 51
DDR3E_A9	RN6D	4	13 51	DDR3E_A13	RN6C	3	14 51	DDR3F_A9	RN3D	4	13 51	DDR3F_A13	RN3C	3	14 51
DDR3E_A10	RN7F	6	11 51	DDR3E_RSTn	RN6B	2	15 51	DDR3F_A10	RN4F	6	11 51	DDR3F_RSTn	RN3B	2	15 51
DDR3E_A11	RN6F	6	11 51	DDR3E_CKE	RN7D	4	13 51	DDR3F_A11	RN3F	6	11 51	DDR3F_CKE	RN4D	4	13 51

DDR3E_DQ[31..0] 25
DDR3E_A[13..0]
DDR3F_A[13..0]
DDR3F_DQ[31..0] 25

U35, U28, U36, U29 — DDR3 Device — MT41J128M16HA

DDR3E_A0 N3	DDR3E_DQ0 E3	DDR3E_DQ16 E3	DDR3F_A0 N3	DDR3F_DQ0 E3	DDR3F_DQ16 E3
DDR3E_A1 P7	DDR3E_DQ1 F7	DDR3E_DQ17 F7	DDR3F_A1 P7	DDR3F_DQ1 F7	DDR3F_DQ17 F7
DDR3E_A2 P3	DDR3E_DQ2 F2	DDR3E_DQ18 F2	DDR3F_A2 P3	DDR3F_DQ2 F2	DDR3F_DQ18 F2
DDR3E_A3 N2	DDR3E_DQ3 F8	DDR3E_DQ19 F8	DDR3F_A3 N2	DDR3F_DQ3 F8	DDR3F_DQ19 F8
DDR3E_A4 P8	DDR3E_DQ4 H3	DDR3E_DQ20 H3	DDR3F_A4 P8	DDR3F_DQ4 H3	DDR3F_DQ20 H3
DDR3E_A5 P2	DDR3E_DQ5 H8	DDR3E_DQ21 H8	DDR3F_A5 P2	DDR3F_DQ5 H8	DDR3F_DQ21 H8
DDR3E_A6 R8	DDR3E_DQ6 G2	DDR3E_DQ22 G2	DDR3F_A6 R8	DDR3F_DQ6 G2	DDR3F_DQ22 G2
DDR3E_A7 R2	DDR3E_DQ7 H7	DDR3E_DQ23 H7	DDR3F_A7 R2	DDR3F_DQ7 H7	DDR3F_DQ23 H7
DDR3E_A8 T8	DDR3E_DQ8 D7	DDR3E_DQ24 D7	DDR3F_A8 T8	DDR3F_DQ8 D7	DDR3F_DQ24 D7
DDR3E_A9 R3	DDR3E_DQ9 C3	DDR3E_DQ25 C3	DDR3F_A9 R3	DDR3F_DQ9 C3	DDR3F_DQ25 C3
DDR3E_A10 L7	DDR3E_DQ10 C8	DDR3E_DQ26 C8	DDR3F_A10 L7	DDR3F_DQ10 C8	DDR3F_DQ26 C8
DDR3E_A11 R7	DDR3E_DQ11 C2	DDR3E_DQ27 C2	DDR3F_A11 R7	DDR3F_DQ11 C2	DDR3F_DQ27 C2
DDR3E_A12 N7	DDR3E_DQ12 A7	DDR3E_DQ28 A7	DDR3F_A12 N7	DDR3F_DQ12 A7	DDR3F_DQ28 A7
DDR3E_A13 T3	DDR3E_DQ13 A2	DDR3E_DQ29 A2	DDR3F_A13 T3	DDR3F_DQ13 A2	DDR3F_DQ29 A2
	DDR3E_DQ14 B8	DDR3E_DQ30 B8		DDR3F_DQ14 B8	DDR3F_DQ30 B8
DDR3E_CKE K9	DDR3E_DQ15 A3	DDR3E_DQ31 A3	DDR3F_CKE K9	DDR3F_DQ15 A3	DDR3F_DQ31 A3
DDR3E_CK_P J7	25,32	25,32	DDR3F_CK_P J7	25,32	19,32
DDR3E_CK_N K7	DDR3E_DQS_P0 F3	DDR3E_DQS_P2 F3	DDR3F_CK_N K7	DDR3F_DQS_P0 F3	DDR3F_DQS_P2 F3
	25,32	25,32		19,32	19,32
	DDR3E_DQS_N0 G3	DDR3E_DQS_N2 G3		DDR3F_DQS_N0 G3	DDR3F_DQS_N2 G3
E7	DDR3E_DQS_P1 C7	DDR3E_DQS_P3 C7	E7	DDR3F_DQS_P1 C7	DDR3F_DQS_P3 C7
D3	DDR3E_DQS_N1 B7	DDR3E_DQS_N3 B7	D3	DDR3F_DQS_N1 B7	DDR3F_DQS_N3 B7
DDR3E_CSn L2	25,32	25,32	DDR3F_CSn L2	25,32	25,32
DDR3E_WEn L3	NC1 J1	NC1 J1	DDR3F_WEn L3	NC1 J1	NC1 J1
DDR3E_RASn J3	NC2 J9	NC2 J9	DDR3F_RASn J3	NC2 J9	NC2 J9
DDR3E_CASn K3	NC3 L1	NC3 L1	DDR3F_CASn K3	NC3 L1	NC3 L1
	NC4 L9	NC4 L9		NC4 L9	NC4 L9
DDR3E_BA0 M2	NC5 M7	NC5 M7	DDR3F_BA0 M2	NC5 M7	NC5 M7
DDR3E_BA1 N8	NC6 T7	NC6 T7	DDR3F_BA1 N8	NC6 T7	NC6 T7
DDR3E_BA2 M3			DDR3F_BA2 M3		
DDR3E_RSTn T2			DDR3F_RSTn T2		
DDR3E_ODT K1	25,32	25,32	DDR3F_ODT K1	25,32	25,32
DDR3E_ZQ01 L8	25,32	25,32	DDR3F_ZQ02 L8	25,32	25,32

VREF_B7_B8 — H1, M8 — VREFDQ, VREFCA — R276 / R263 / R275 / R262 240 — 1.5V

VDD: B2, D9, G7, K2, K8, N1, N9, R1, R9
VDDQ: A1, A8, C1, C9, D2, E9, F1, H2, H9
VSS: J2, J8, A9, M1, M9, B3, P1, P9, E1, T1, T9, G8
VSSQ: B1, B9, D1, D8, E2, E8, F9, G1, G9

1.5V

C469	C376	C377	C386	C387	C410	C411	C425	C426	C454	C455	C466	C467	C488	C489	C501	C502	C422	C492	C409	C424	C500	C457	C375	C385	C453	C465	C412
2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	3.3nF	3.3nF	4.7nF	4.7nF	4.7nF	0.01uF	0.01uF	0.01uF	0.01uF	0.01uF	0.01uF

1.5V

C427	C503	C490	C414	C388	C378	C423	C408	C468	C456	C487	C499	C504	C491	C452	C464	C413	C428	C374	C384					
0.01uF	0.01uF	0.01uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.47uF	0.47uF	0.47uF	0.47uF	0.47uF	0.47uF	0.47uF	0.47uF					

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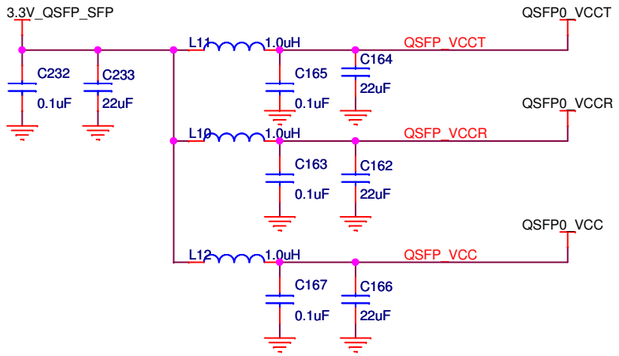
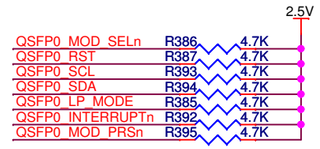
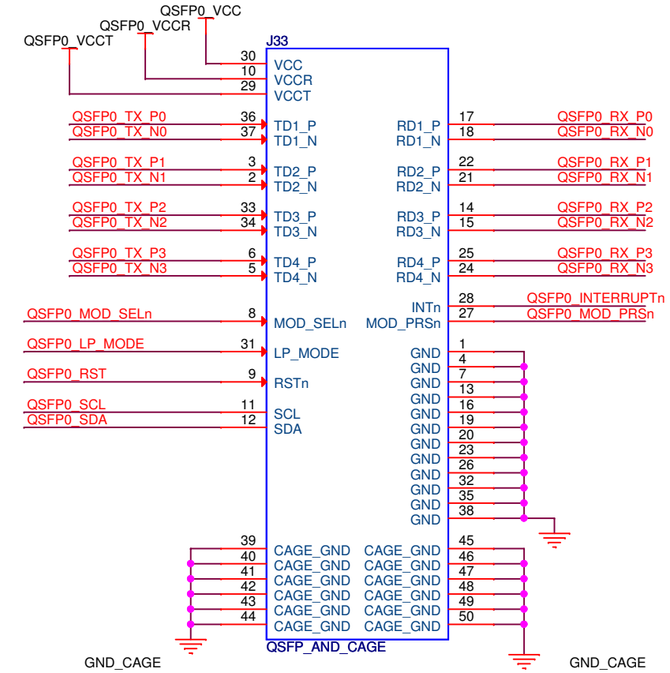
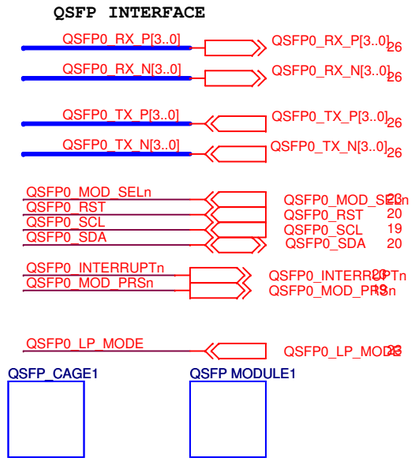
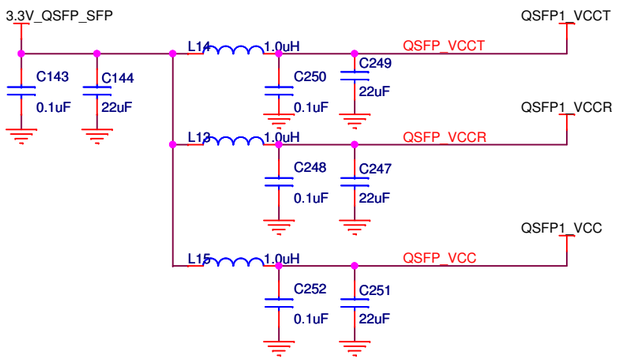
Quad Small Form-factor Pluggable (QSFP) Interface

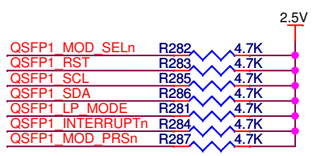


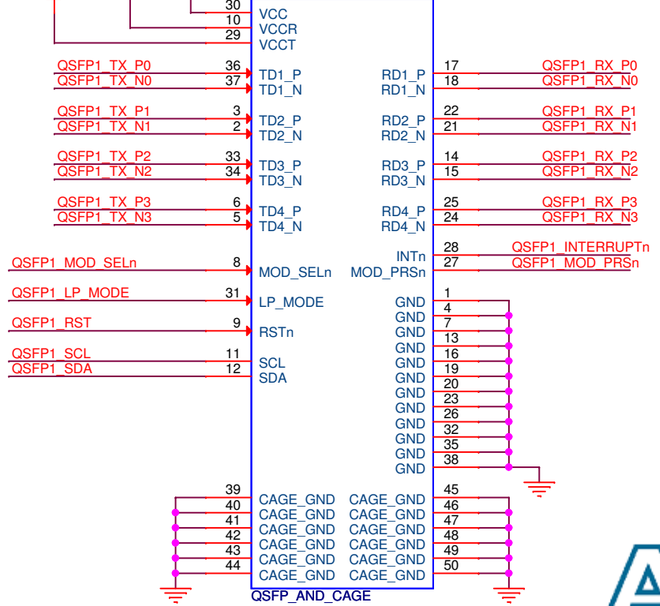


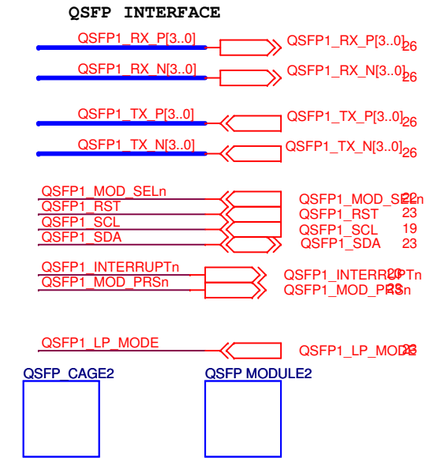












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XCVR Based SFP Connectors

NOTE 1: 1uH ferrite bead should have a DC resistance of less than 1-ohm.

NOTE 2: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

NOTE 3: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

SFPs 0-3

J10A

SFP/+ MODULE 0

SFP/+ MODULE 1

SFP/+ MODULE 2

SFP/+ MODULE 3

747280415_BELLY

3.3V_QSFP_SFP

L1 4.7uH, C89 0.1uF, C75 0.1uF, C76 22uF — SFP3_VCCT

L3 4.7uH, C90 0.1uF, C91 22uF — SFP3_VCCR

Wurth Electronics Inc.
74479887247

L4 4.7uH, C102 0.1uF, C99 0.1uF, C100 22uF — SFP2_VCCT

L5 4.7uH, C104 0.1uF, C103 22uF — SFP2_VCCR

L6 4.7uH, C115 0.1uF, C113 0.1uF, C114 22uF — SFP1_VCCT

L7 4.7uH, C118 0.1uF, C119 22uF — SFP1_VCCR

L8 4.7uH, C128 0.1uF, C122 0.1uF, C123 22uF — SFP0_VCCT

L9 4.7uH, C132 0.1uF, C133 22uF — SFP0_VCCR

SFP Modules - Signal Connections will be made in the schematic on the connectors.

SFP1, SFP4, SFP3, SFP2 (MH1, MH2) — SFP20

3.3V_QSFP_SFP

R268 4.7K SFP0_RS1
R252 4.7K SFP1_RS1
R238 4.7K SFP2_RS1
R230 4.7K SFP3_RS1

If using SFP this pin must be grounded.
If using SFP+:
0= TX datarates <= 4.25GB/s
1= TX datarates > 4.25GB/s

3.3V_QSFP_SFP

R256 4.7K SFP0_TXFAULT
R259 4.7K SFP0_MOD0_PRSNTn
R258 4.7K SFP0_MOD1_SCL
R257 4.7K SFP0_MOD2_SDA
R261 4.7K SFP0_LOS
R260 4.7K SFP0_RATESEL

R241 4.7K SFP1_TXFAULT
R245 4.7K SFP1_MOD0_PRSNTn
R244 4.7K SFP1_MOD1_SCL
R242 4.7K SFP1_MOD2_SDA
R251 4.7K SFP1_LOS
R250 4.7K SFP1_RATESEL

3.3V_QSFP_SFP

R232 4.7K SFP2_TXFAULT
R235 4.7K SFP2_MOD0_PRSNTn
R234 4.7K SFP2_MOD1_SCL
R233 4.7K SFP2_MOD2_SDA
R237 4.7K SFP2_LOS
R236 4.7K SFP2_RATESEL

R220 4.7K SFP3_TXFAULT
R223 4.7K SFP3_MOD0_PRSNTn
R222 4.7K SFP3_MOD1_SCL
R221 4.7K SFP3_MOD2_SDA
R229 4.7K SFP3_LOS
R228 4.7K SFP3_RATESEL

3.3V_QSFP_SFP

SFP3_MOD0_PRSNTn — D11 GREEN LED — 49.9 — R219
SFP2_MOD0_PRSNTn — D14 GREEN LED — 49.9 — R231
SFP1_MOD0_PRSNTn — D15 GREEN LED — 49.9 — R239
SFP0_MOD0_PRSNTn — D16 GREEN LED — 49.9 — R255

J10B

CAGE GND & MOUNTING HOLES

747280415_BELLY

GND_SFP

Optical (SFP) Transceiver Cage & Connector

R35 100K, C142 DNI — GND_SFP

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Transceiver Power and CFP

J25B

CFP_MOD

LTI-SASF546-P26-X1

J40

J49

GND_CAGE

3.3V_CFP

3.3V L17 3.3V_CFP

10A BEAD

J25A

CFP_MOD

U38O

Stratix V GX Transceiver Power

Transceiver Analog Driver Power

Receiver Analog Power

Transmitter Analog Power

Transceiver I/O Buffer

PCI/IP Digital Power

Transceiver Analog Power

5SGXA7_F1932

0.4 Preliminary

J39

J48

CFP_MOD_ABS R318 10.0K 2.5V

B2 Rail

B3 rail

B4 Recpt Cover

B5 Receptical

B6 heat sink

B7 Backer Plate

U68 MAX3373

R58 100K

C161 DNI

GND_CAGE

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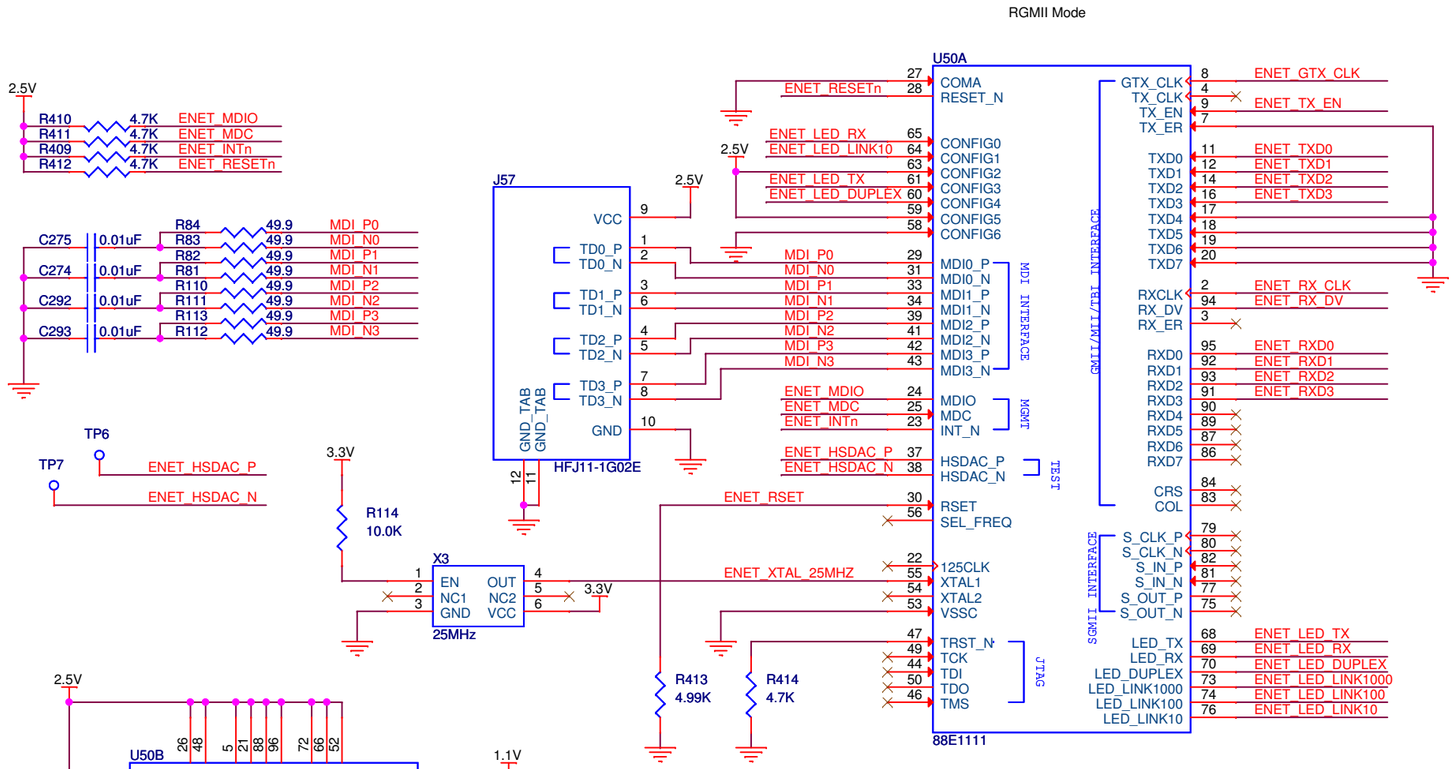
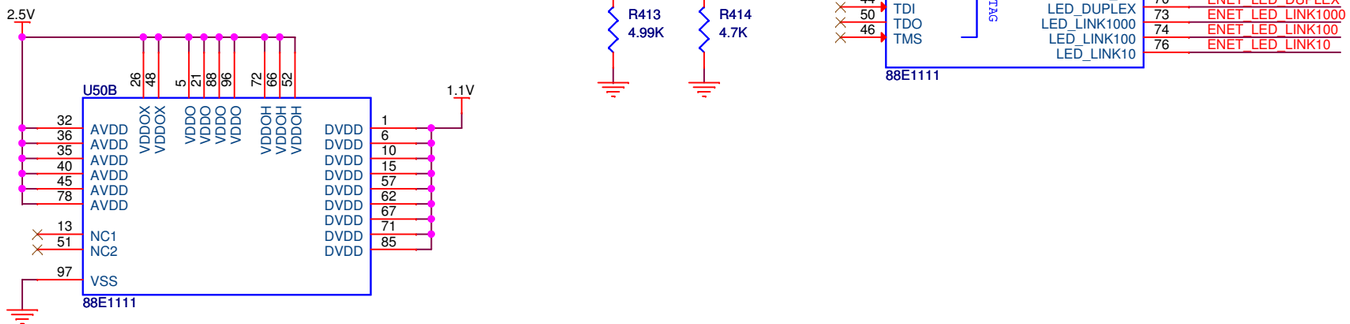
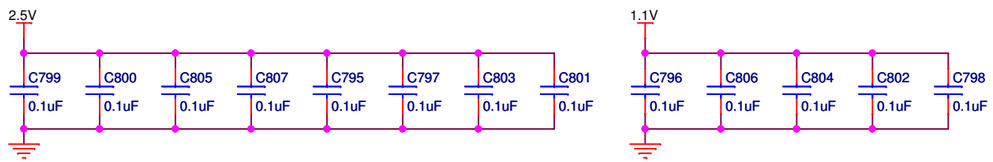
10/100/1000 Ethernet

RGMII Mode

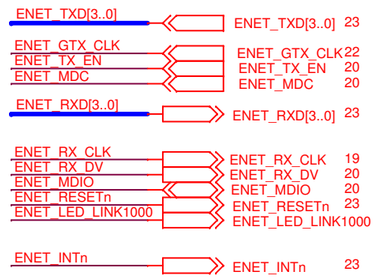


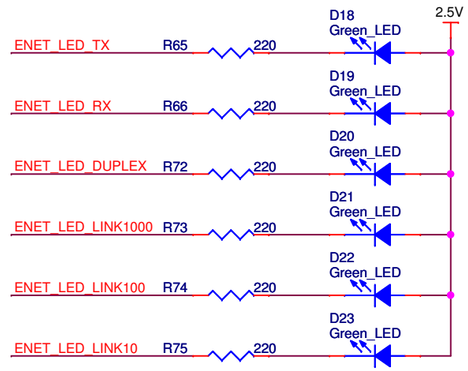


Place near 88E1111 PHY



ETHERNET INTERFACE





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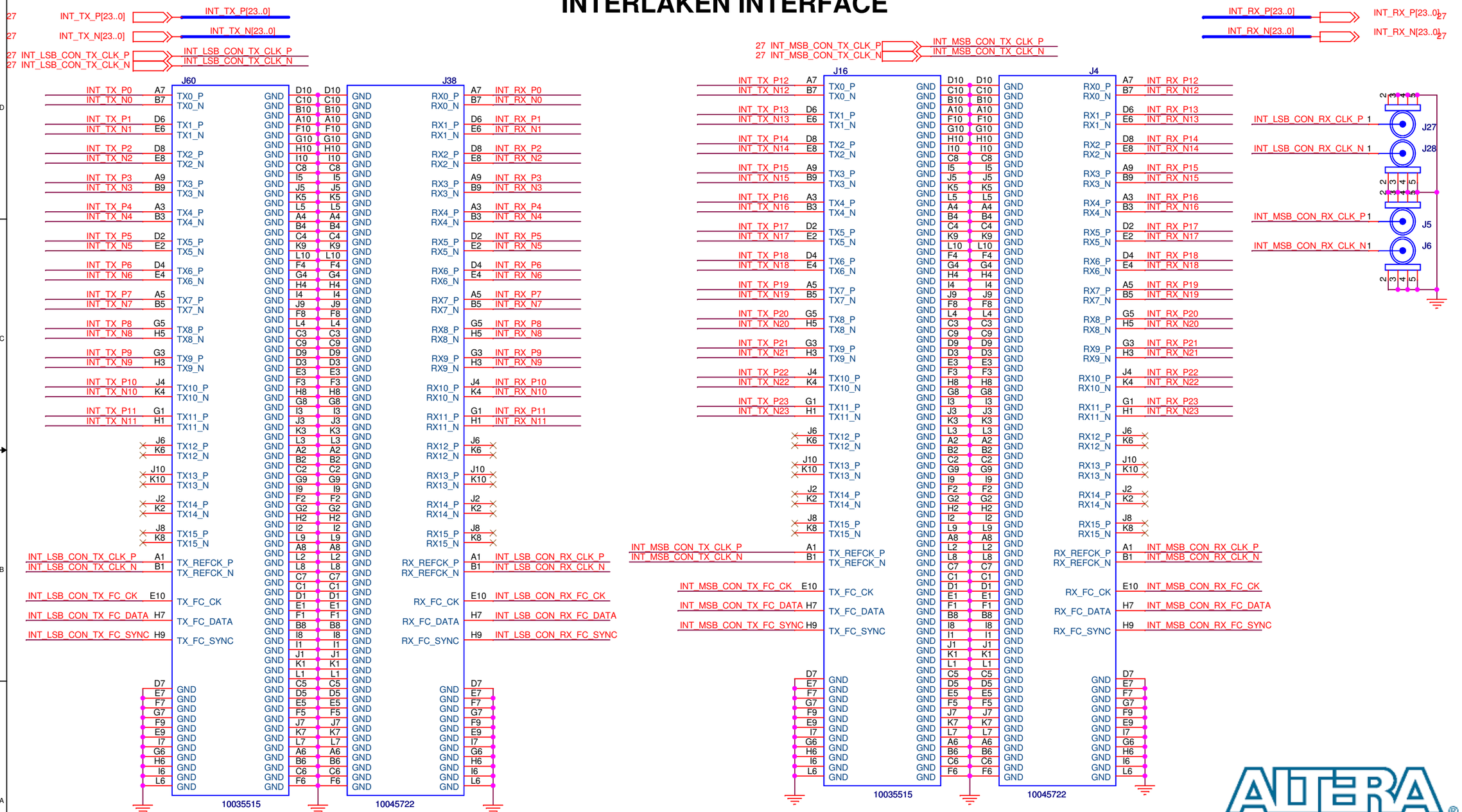
INTERLAKEN INTERFACE



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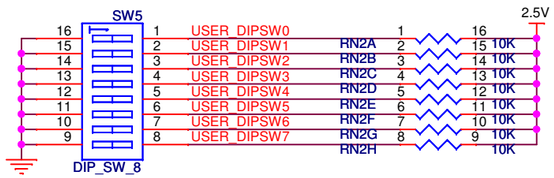
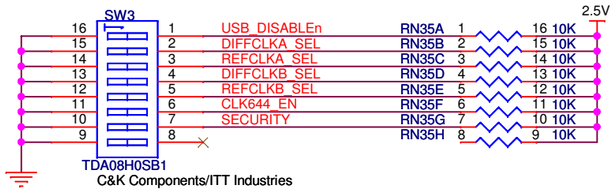
User IO & Connector

MAX USER DIPSWITCH



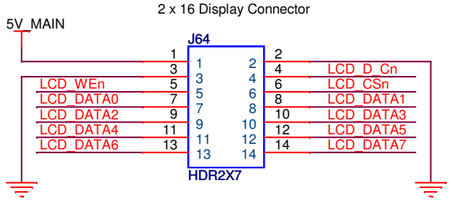
BOARD SETTINGS DIPSWITCH

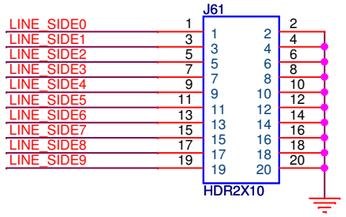


B8 — 2x16 LCD

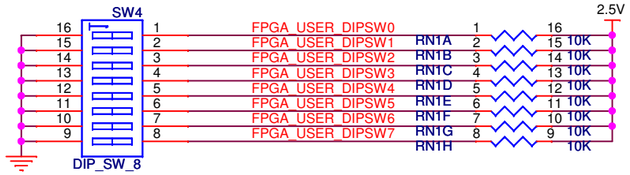
B9 — 2x7 HDR

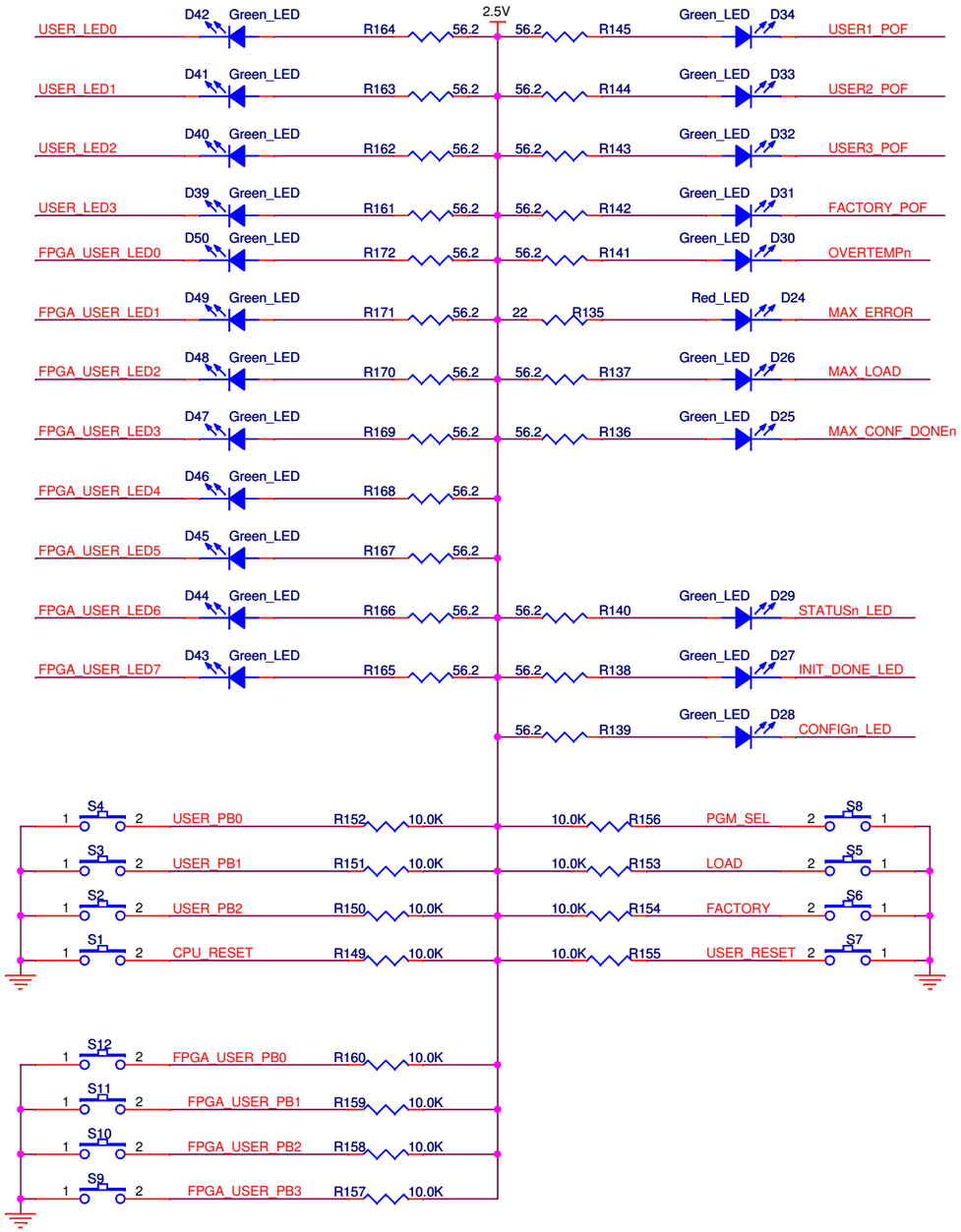
2 x 16 Display Connector





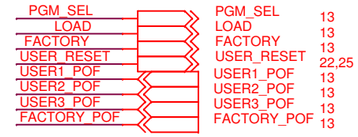
FPGA USER DIPSWITCH



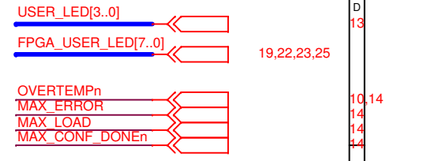


2x16 LED DISPLAY INTERFACE

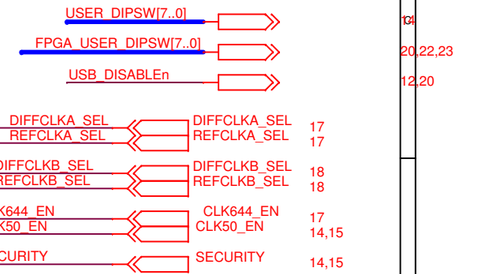
PUSH BUTTON INTERFACE

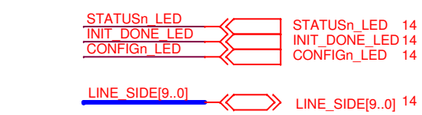


LED INTERFACE



DIP SWITCH INTERFACE





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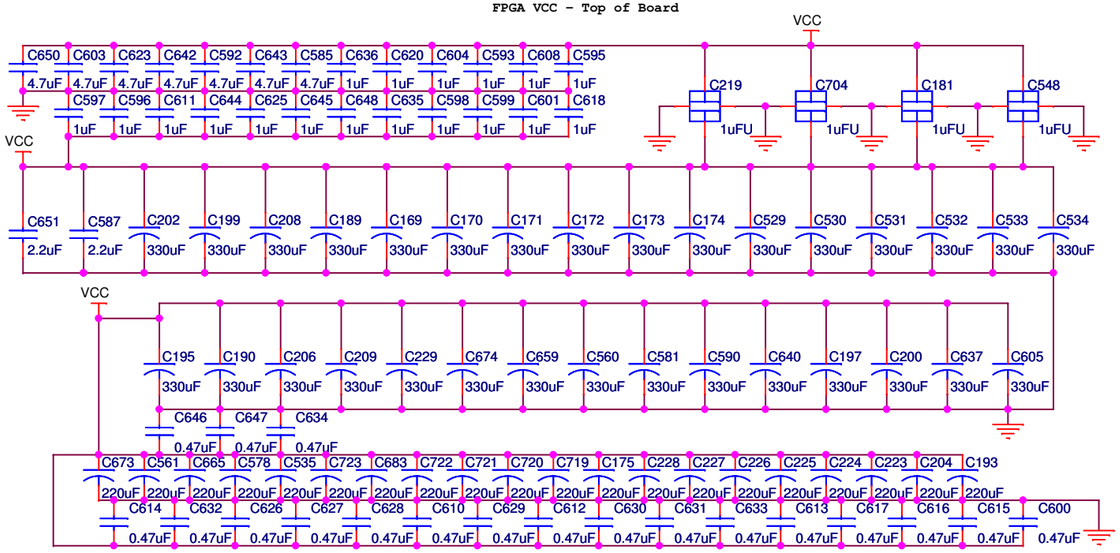
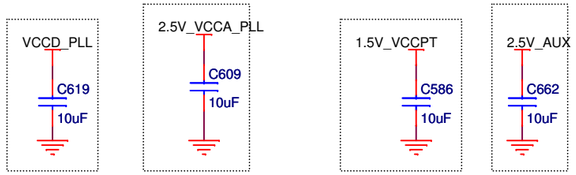
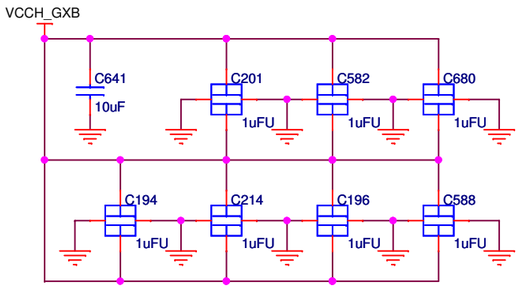
Decoupling

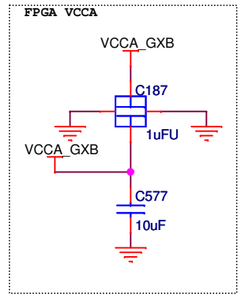
Place 6 vias minimum on each X2Y cap.

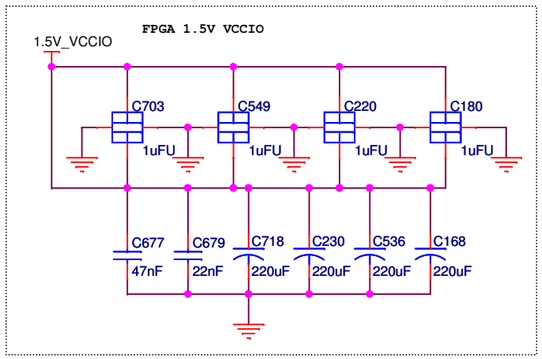
FPGA VCC - Top of Board

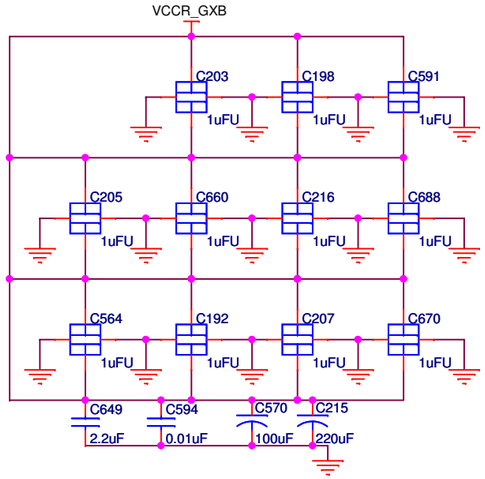


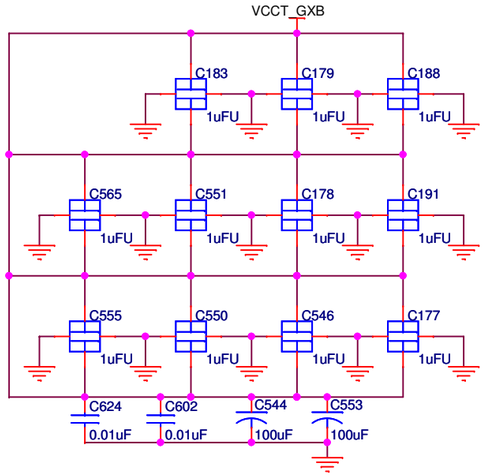


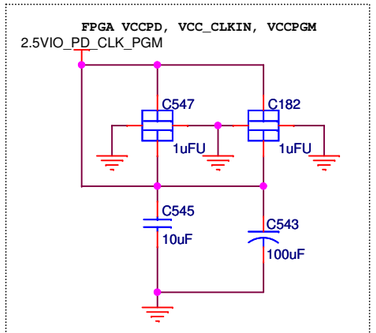












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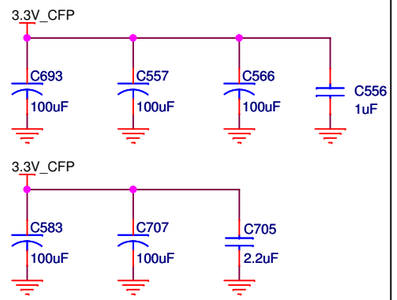
CFP DECOUPLING

Place near CFP



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B	150-0310914-01 (6XX-43106R)	A

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