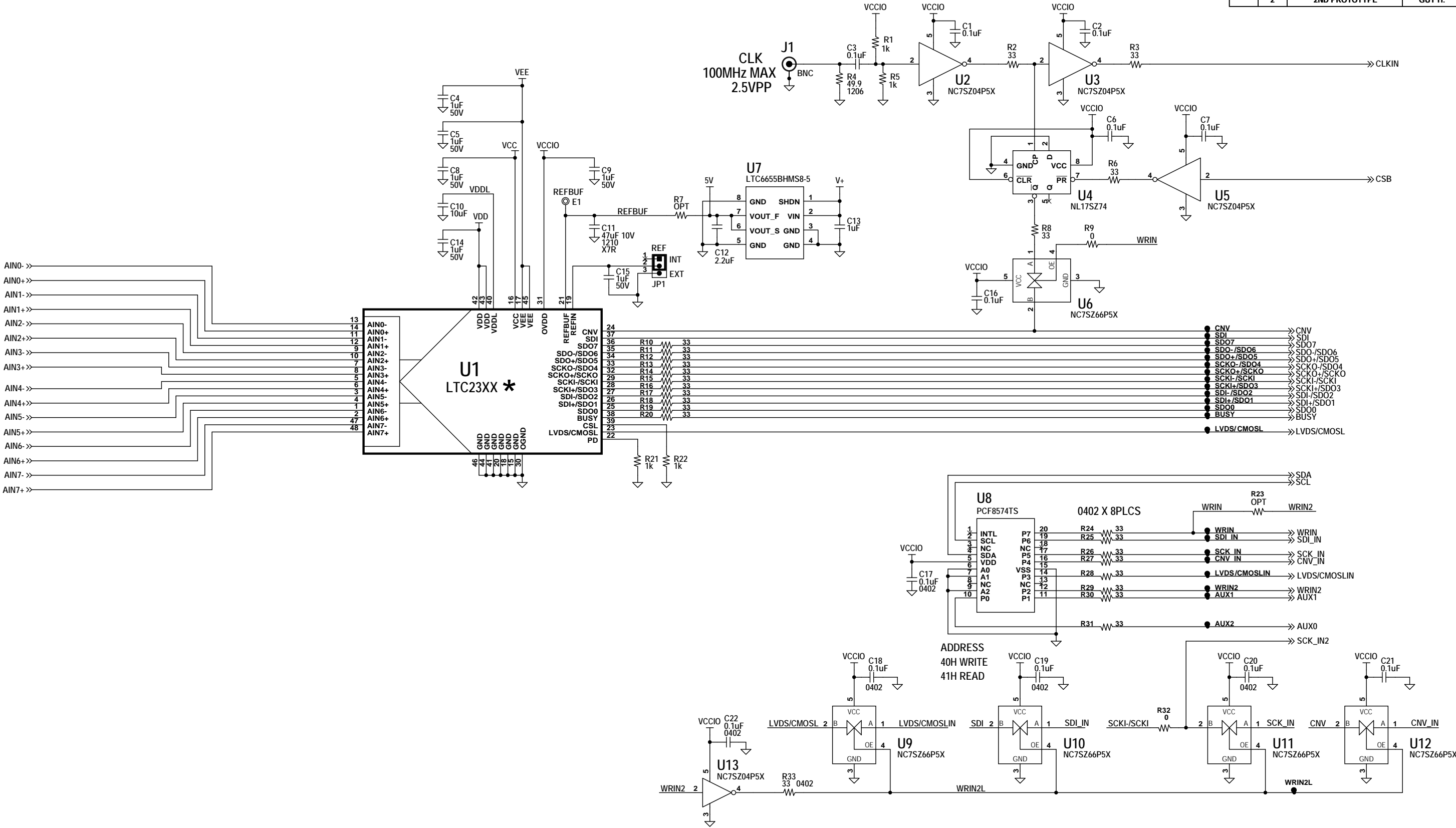


REVISION HISTORY				
ECO	REV	DESCRIPTION	APPROVED	DATE
	2	2ND PROTOTYPE	GUY H.	12-17-15

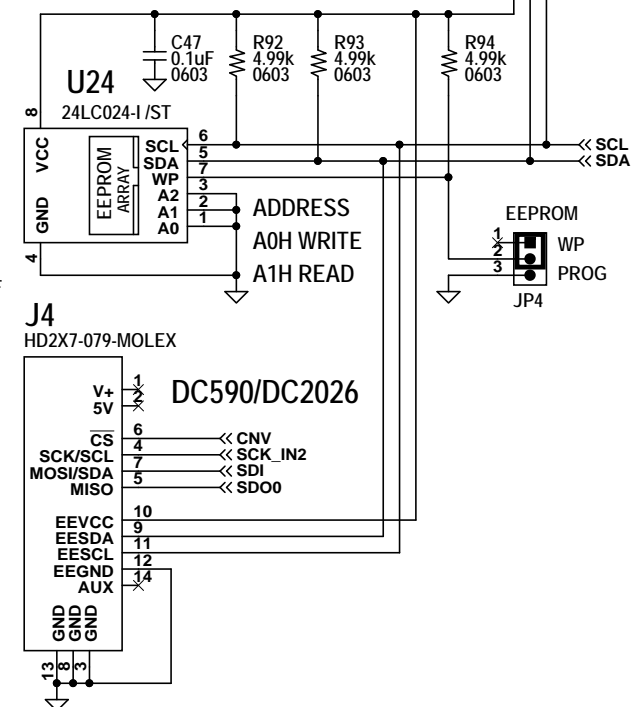
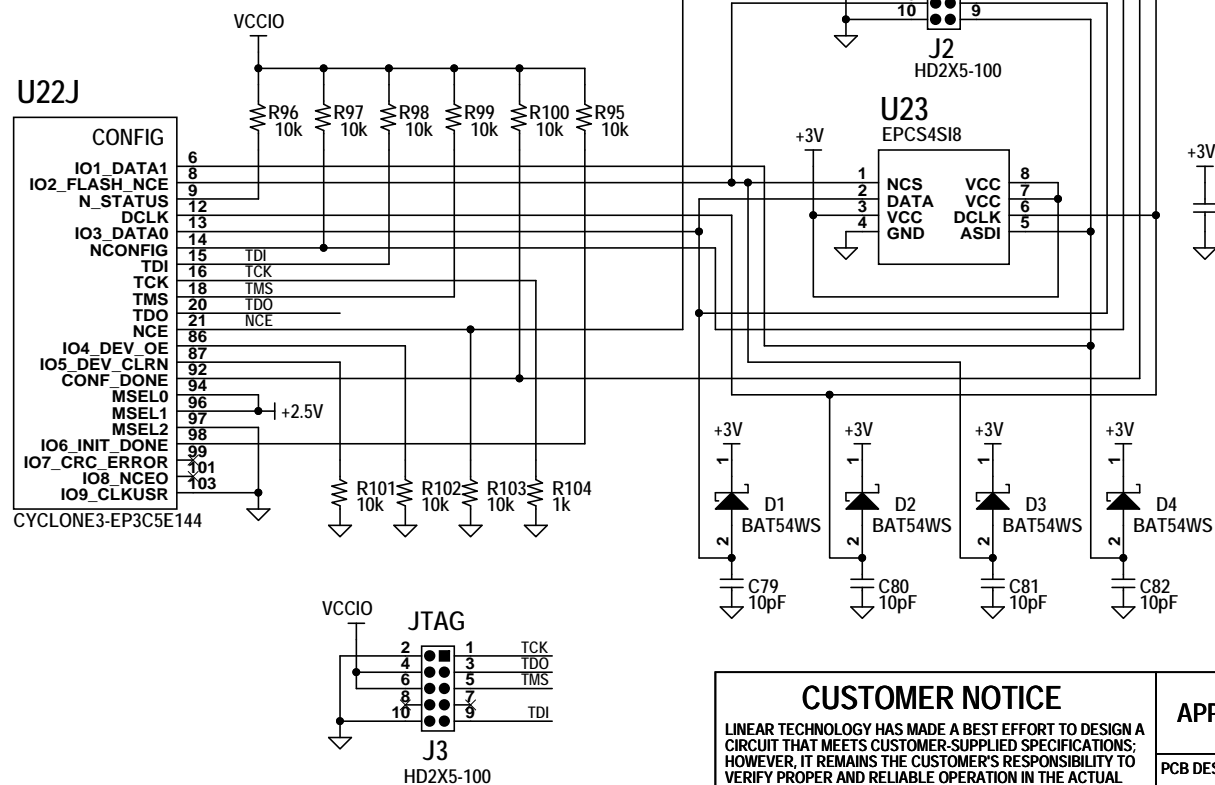
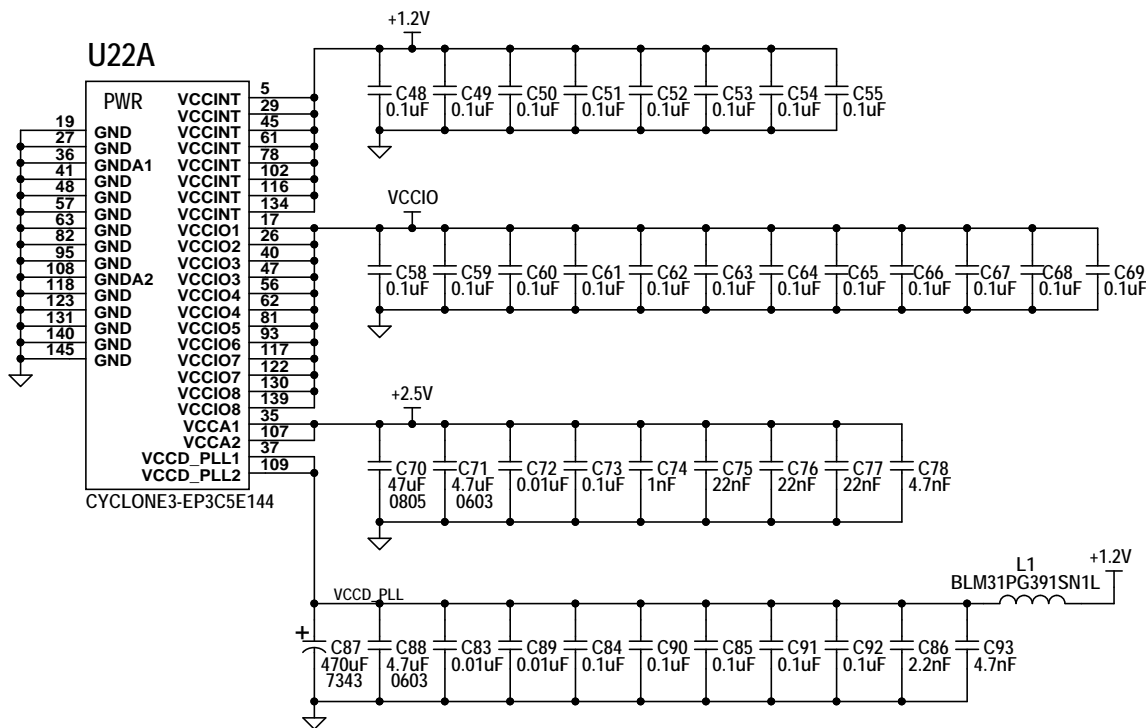
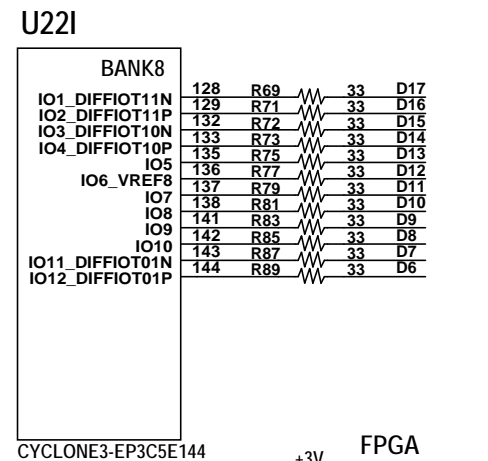
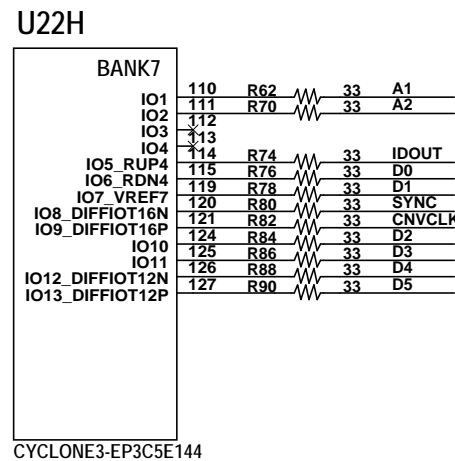
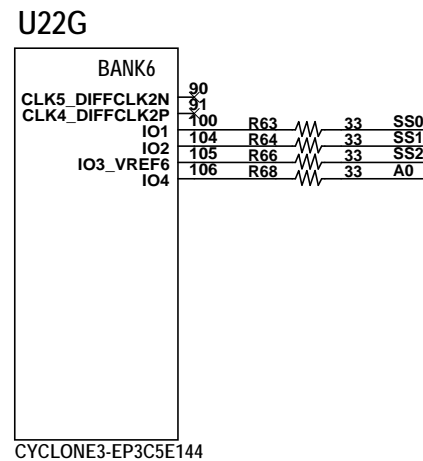
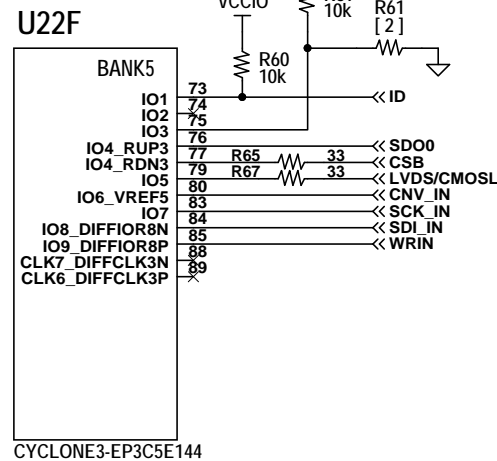
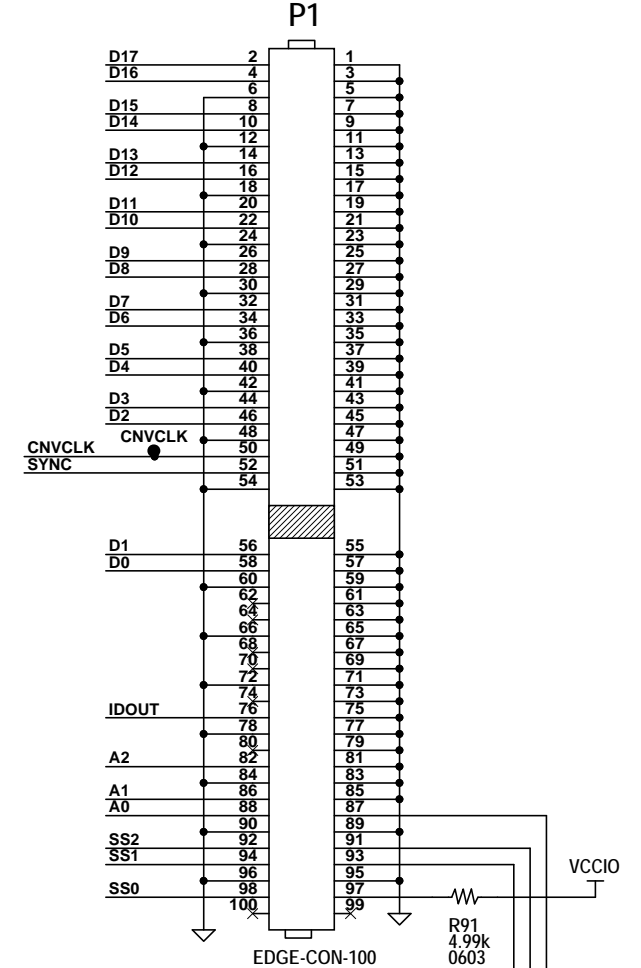
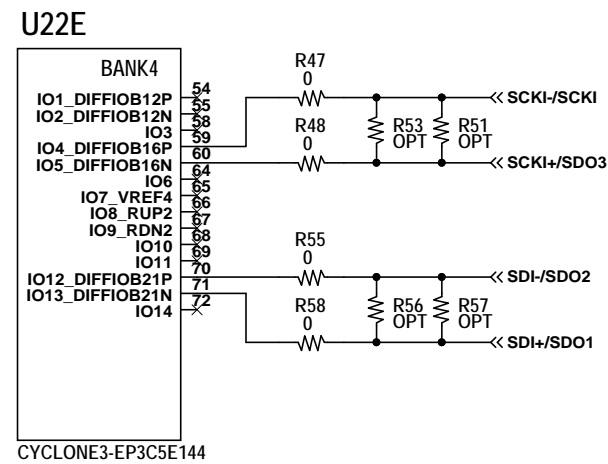
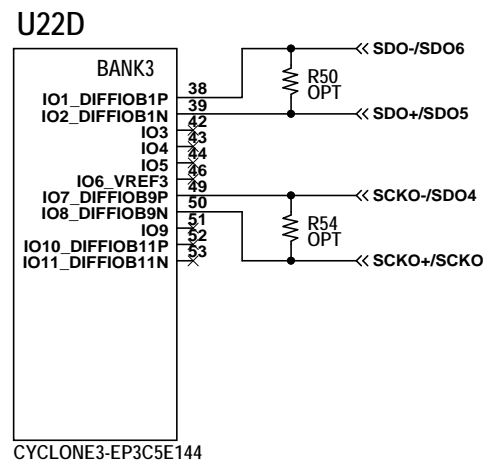
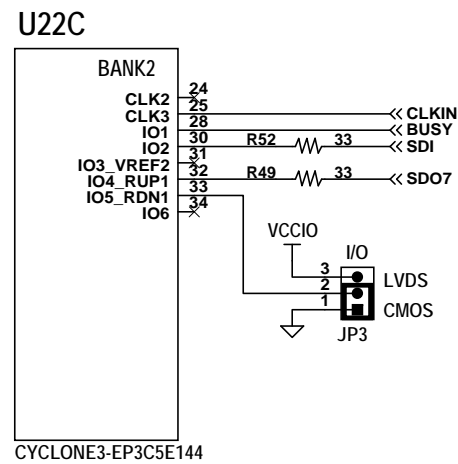
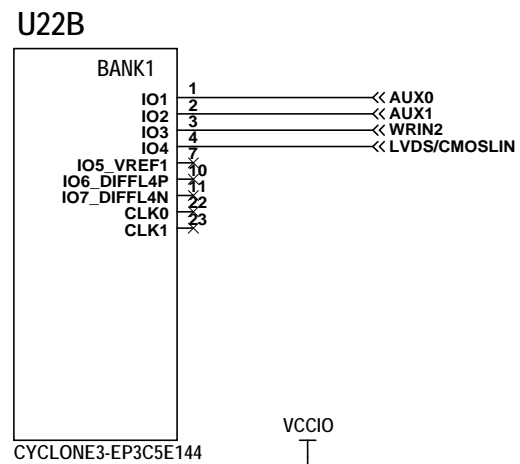


*	ASSY	U1	SUFFIX	-Bit	Ksps	-CHANNEL	R61 (PAGE 3)
	-A	LTC2358-18	58-18	18	200	8	0
	-B	LTC2357-18	57-18	18	400	4	0
	-C	LTC2353-18	53-18	18	600	2	0
	-D	LTC2333-18	33-18	18	1000	8	0
	-E	LTC2358-16	58-16	16	200	8	OPT
	-F	LTC2357-16	57-16	16	400	4	OPT
	-G	LTC2353-16	53-16	16	600	2	OPT
	-H	LTC2333-16	33-16	16	1000	8	OPT

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS AND CAPACITORS ON THIS PAGE ARE 0603.

CUSTOMER NOTICE		APPROVALS		LINEAR TECHNOLOGY	
LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.		PCB DES.	KIM T.	1630 McCarthy Blvd. Milpitas, CA 95035 Phone: (408)432-1900 www.linear.com Fax: (408)434-0507 LTC Confidential-For Customer Use Only	
		APP ENG.	GUY H.		
THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.		SCALE = NONE		TITLE: SCHEMATIC 8/4/2-CHANNEL, BUFFERED SOFTSPAN SIMULTANEOUS SAMPLING AND MULTIPLEXED ADCS	
		SIZE	IC NO.	LTC23XXILX FAMILY	
		B		DEMO CIRCUIT 2365A	
		DATE:	Thursday, December 17, 2015	REV. 2	
				SHEET 1 OF 4	



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS AND CAPACITORS ON THIS PAGE ARE 0402.
2. R61 IS 0 OHMS ON ASSEMBLY TYPES A,B,C,D AND OPTIONAL ON E,F,G,H. (SEE ASSY TABLE ON PAGE 1)

CUSTOMER NOTICE

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**THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND
SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.**

APPROVALS

PCB DES.	KIM T.
APP ENG.	GUY H.

SCALE = NONE

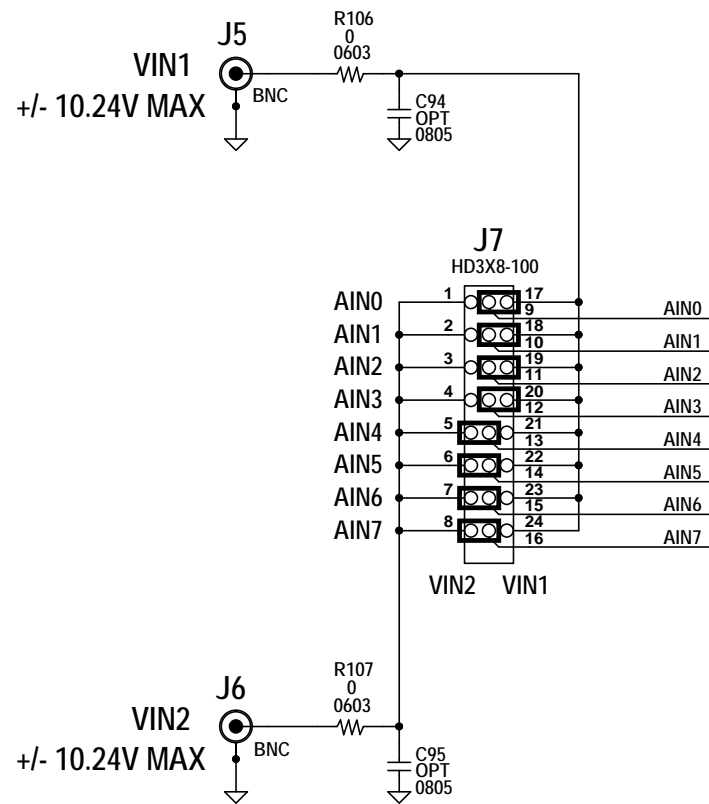


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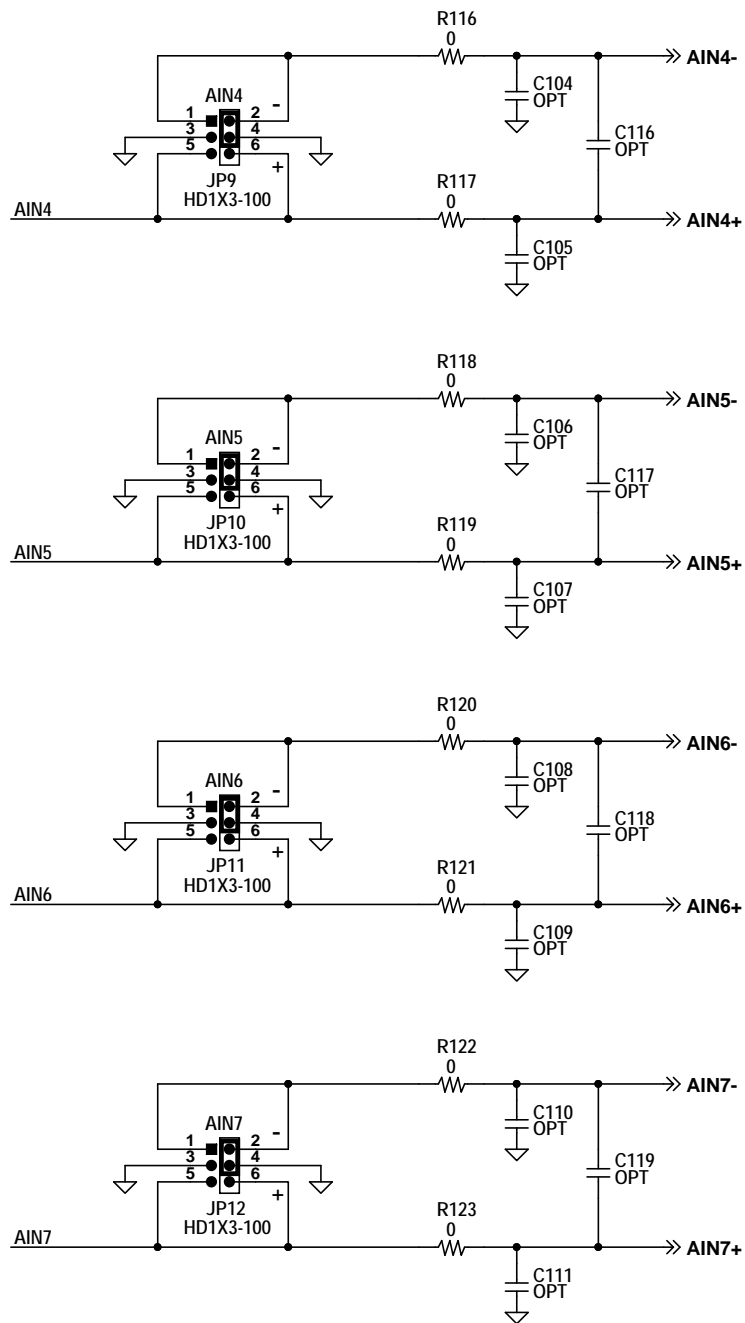
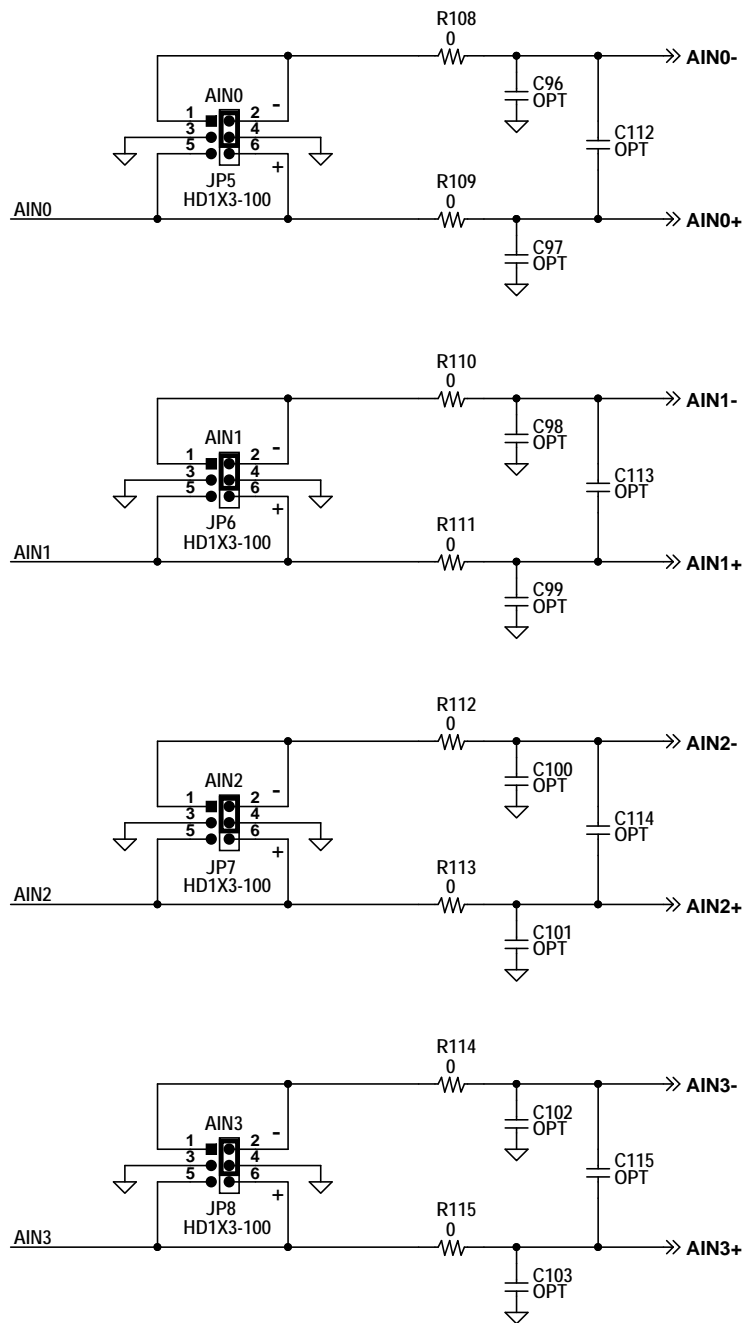
TITLE: SCHEMATIC
8/4/2-CHANNEL, BUFFERED SOFTSPAN
SIMULTANEOUS SAMPLING AND MULTIPLEXED ADCS

SIZE B	IC NO. LTC23XXILX FAMILY DEMO CIRCUIT 2365A	REV 2
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DATE: Wednesday, December 09, 2015 SHEET 3 OF 4



	AIN7 (JP12)	AIN6 (JP11)	AIN5 (JP10)	AIN4 (JP9)	AIN3 (JP8)	AIN2 (JP7)	AIN1 (JP6)	AIN0 (JP5)
8-CH	X	X	X	X	X	X	X	X
4-CH	X		X			X		X
2-CH			X			X		



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS AND CAPACITORS ON THIS PAGE ARE 0402.
2. FOR JP5 TO JP12, INSTALL ONLY 3 PINS JUMPER, HD1X3-100, AS SHOWN.

CUSTOMER NOTICE

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THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.

APPROVALS

PCB DES. KIM T.
APP ENG. GUY H.

SCALE = NONE



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TITLE: SCHEMATIC
8/4/2-CHANNEL, BUFFERED SOFTSPAN
SIMULTANEOUS SAMPLING AND MULTIPLEXED ADCS

SIZE B IC NO. LTC23XXILX FAMILY
DEMO CIRCUIT 2365A

REV. 2

DATE: Thursday, December 17, 2015

SHEET 4 OF 4