

| | |
|-----------------------------|----------------|
| 1. Project Drawing Numbers: | |
| Raw PCB | 100-0320806-C1 |
| Gerber Files | 110-0320806-C1 |
| PCB Design Files | 120-0320806-C1 |
| Assembly Drawing | 130-0320806-C1 |
| Fab Drawing | 140-0320806-C1 |
| Schematic Drawing | 150-0320806-C1 |
| PCB Film | 160-0320806-C1 |
| Bill of Materials | 170-0320806-C1 |
| Schematic Design Files | 180-0320806-C1 |
| Functional Specification | 210-0320806-C1 |
| PCB Layout Guidelines | 220-0320806-C1 |
| Assembly Rework | 320-0320806-C1 |

Known Issue List:

- (1) Full duplex x8 transceivers @ 6G interface at HSMC connector can not be compiled in the same Quartus II project. Up to x7 transceivers @ 6G can be compiled at in one Quartus II project.
- (2) LVDS channels in bank 2 and bank 3 of HSMC connector with total of 17 channels can not be compiled in the same Quartus II project. LVDS channels in HSMC bank 2 needs clock source from bottom banks while bank 3 needs clock source from top banks of FPGA.

The diagram illustrates the system architecture of the Altera Arria V 5AGXFB3H4F35C4N SoC. The central component is the **ALTERA Arria V 5AGXFB3H4F35C4N** SoC. Key interfaces and components include:

- Top Interface:** LVDS/Single-Ended interface connected to an **hsmc** component.
- Left Interface:** Type-B USB 2.0 connected to an **ALTERA MAX II EPM570GM100C4N Embedded USB Blaster II** via an x19 USB Interface. A JTAG Chain is also shown.
- Bottom-Left Interface:** Refclk SMA IN (x1 LVPECL), Trigger SMA OUT (x1), GigE PHY (x1), and SDI TX/RX (XCVR x1).
- Bottom Interface:** Oscillators Programmable (125M, 50M), **PCI EXPRESS x8 Edge**, and **ALTERA MAX V 5M2210ZF256C4N** (connected via x4, XCVR x8, x16 Config, Addr x26, and Data x32).
- Right Interface:** 256MB DDR3 (x32), x4 XCVR (HDMI TX), x1 XCVR (XCVR SMA OUT & IN), x11 LCD Character, x3 Button & Switches, x4 LED, x10 LED, x16 2MB SSRAM, x16 128MB Flash, and x16 128MB Flash.

| PAGE | DESCRIPTION | PAGE | DESCRIPTION |
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| 1 | Title, Notes, Block Diagram, Rev. History | 30 | Power 5 - Linear Regulator |
| 2 | FPGA Package Top | 31 | Power 6 - Power Monitor |
| 3 | System Block Diagram | 32 | Power 7 - Arria V GX Power |
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| 22 | HSMC Port | | |
| 23 | Ethernet PHY & RJ-45 | | |
| 24 | On-Board USB Blaster II | | |
| 25 | User I/O (LEDs, Buttons, Switches, LCD) | | |
| 26 | Power 1 - DC Input, 12V, 3.3V | | |
| 27 | Power 2 - 1.1V & 2.5V FPGA | | |
| 28 | Power 3 - 1.15V & 1.5V FPGA | | |
| 29 | Power 4 - 2.5V | | |

Rev
C1.1

FPGA Package Top View

Top View - Flip Chip
Arria V – 5AGXFB3H4F35C4N

Bank 7A VCCIO = 2.5V
Bank 7B HSMC LVDS,
Bank 7C MAX V

Bank 7D PCIe side band, user IO

Bank 8A VCCIO = 1.5V
Bank 8B DDR3
Bank 8C

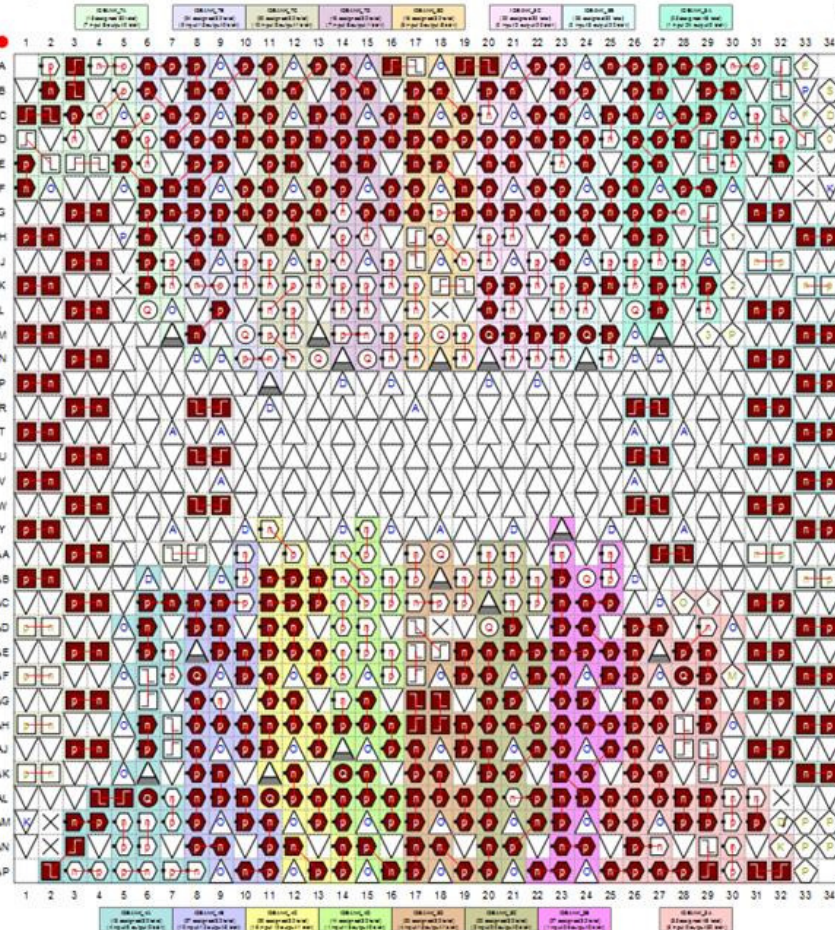
Bank 8D VCCIO = 1.5V
User IO

XCVR Bank QR1
HSMC x8

XCVR Bank QR0
HSMC x8
HDMI

XCVR Bank QL1
PCI Express x8
SDI
SMA

XCVR Bank QL0
PCI Express x8



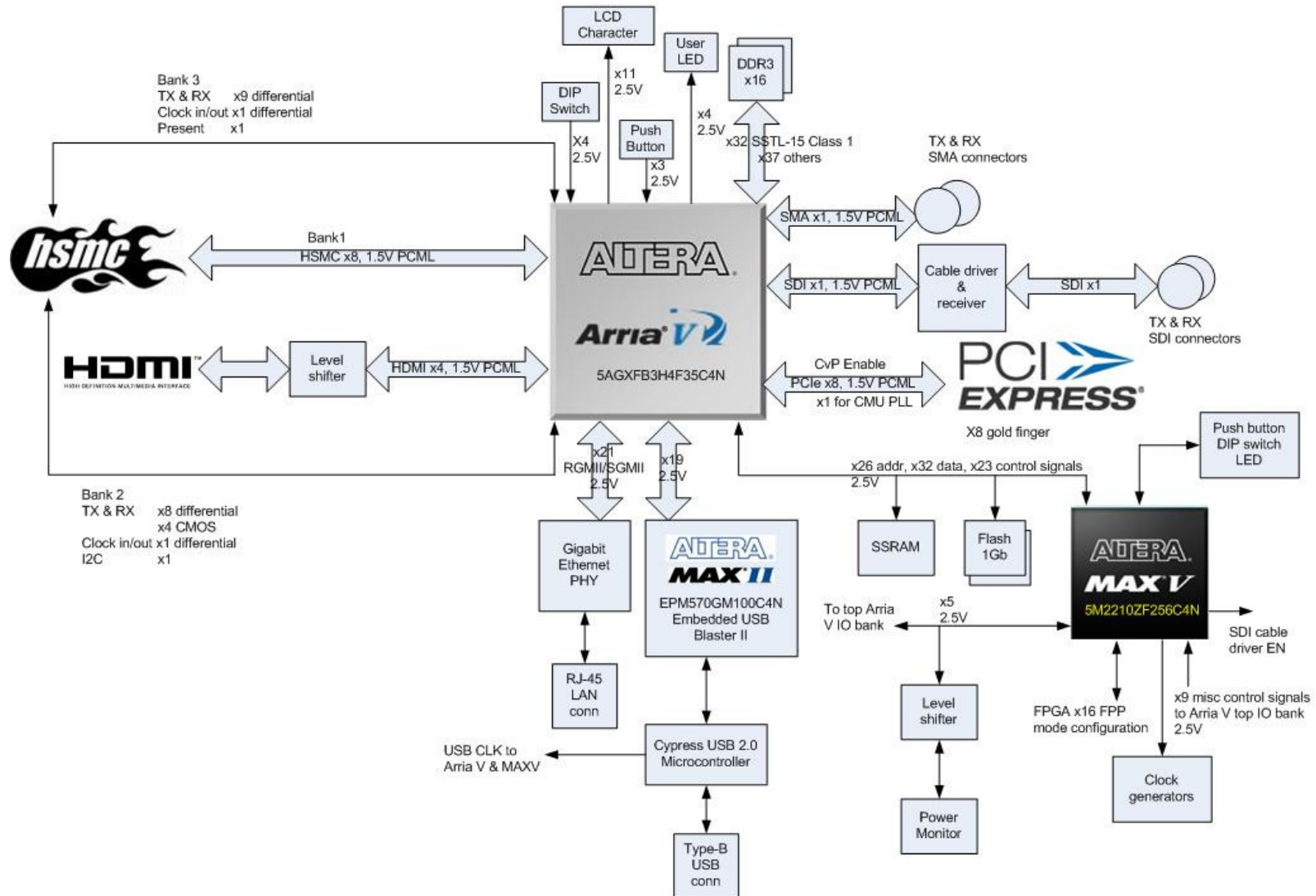
Bank 4A VCCIO = 2.5V
Bank 4B HSMC LVDS
Bank 4C HDMI control, Ethernet
Bank 4D USB Blaster II

Bank 3A VCCIO = 2.5V
Bank 3B Flash, SSRAM, SDI
Bank 3C control, USB Blaster II
Bank 3D



| | | | |
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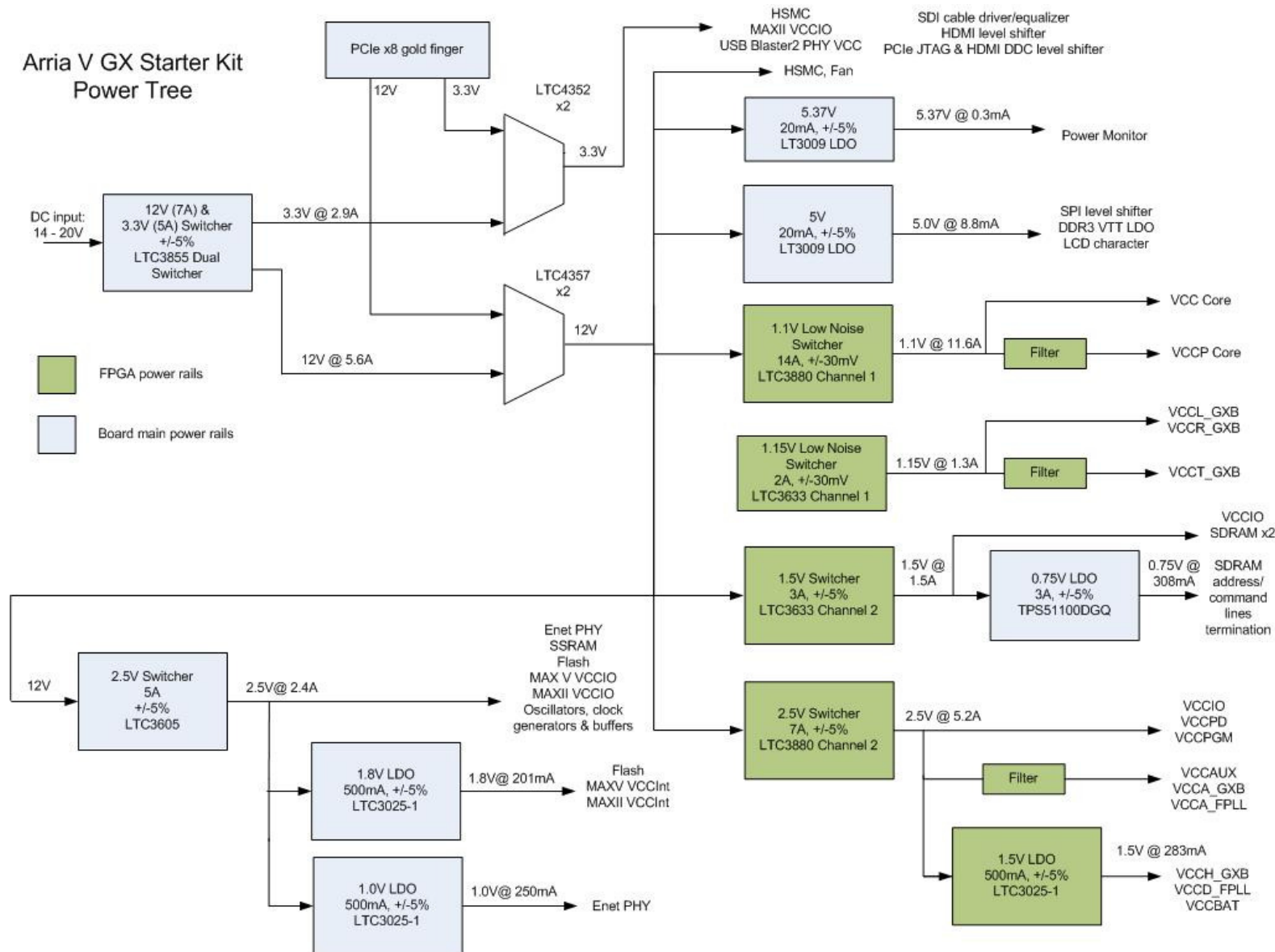
Arria V GX Starter Kit System Block Diagram



ALTERA

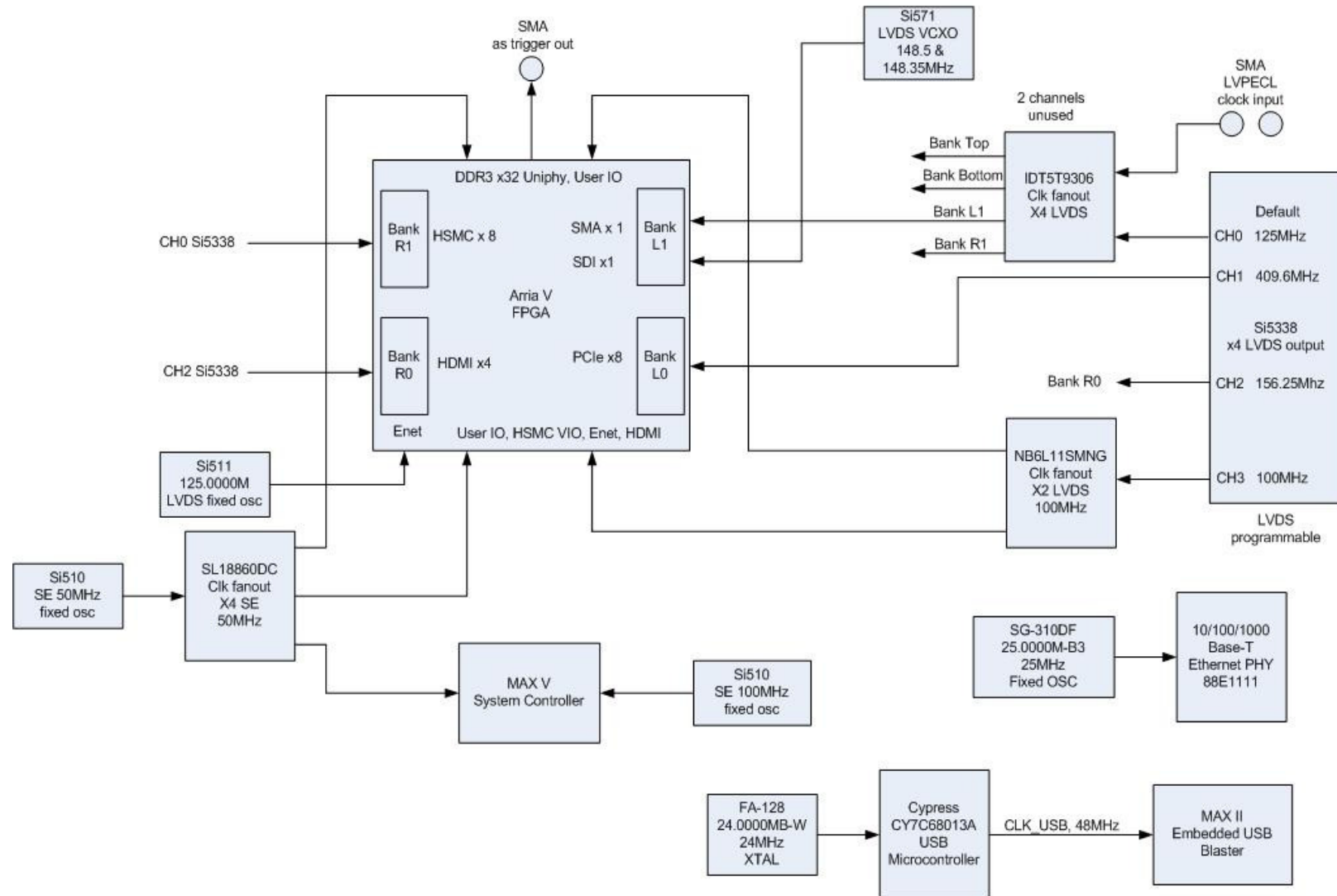
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Arria V GX Starter Kit Power Tree



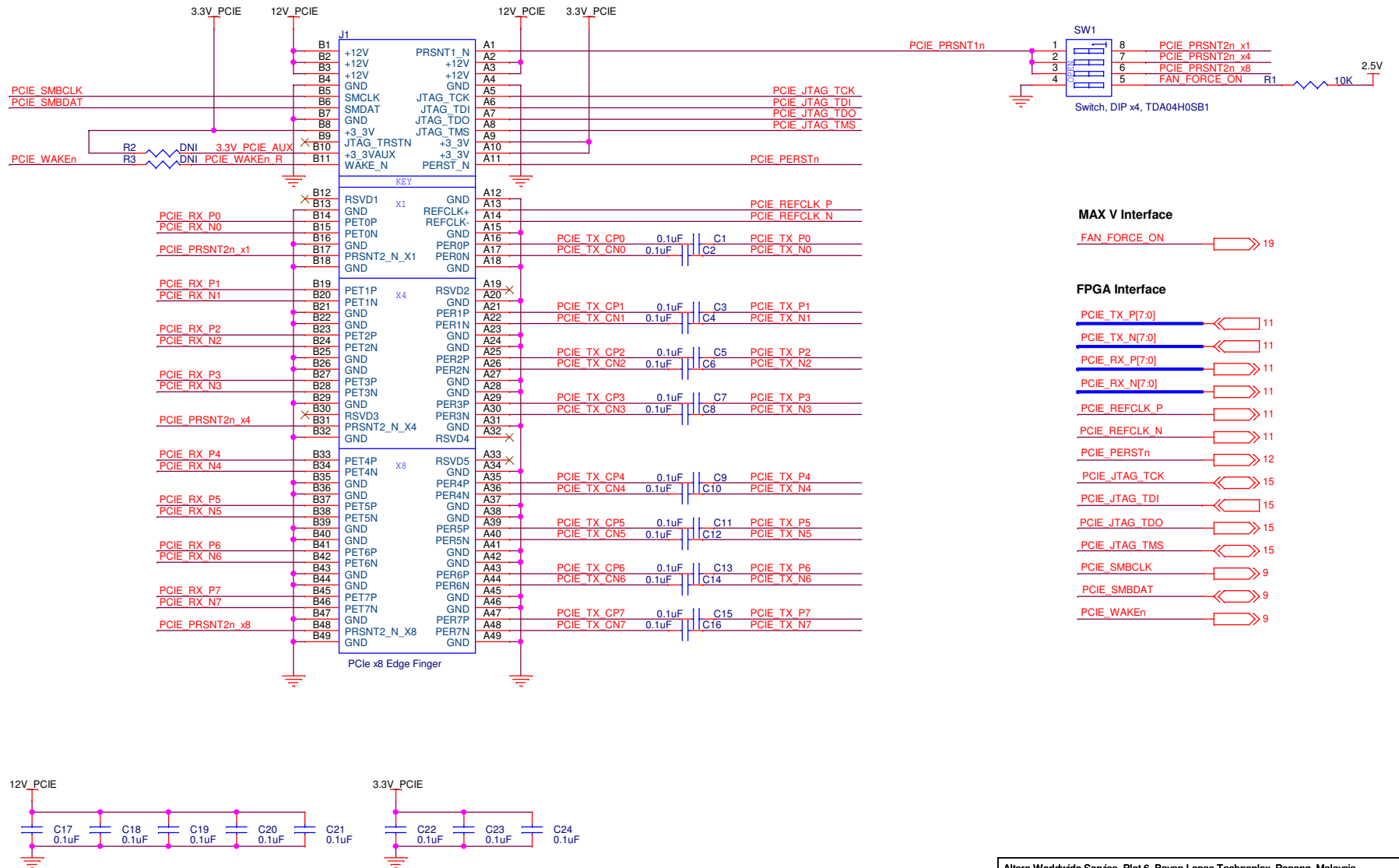
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Arria V GX Starter Kit Clock Tree



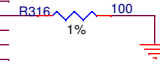
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PCI Express x8 Edge Connector

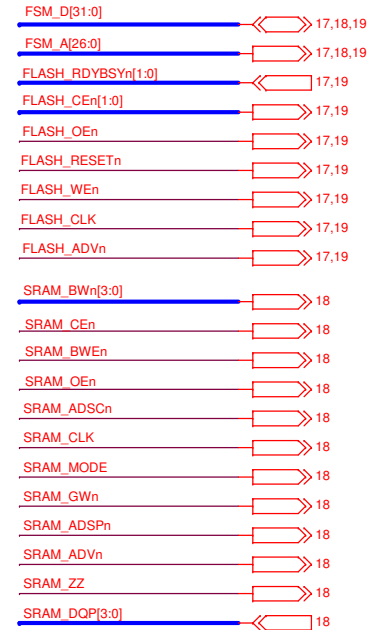


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Arria V GX Bank 3



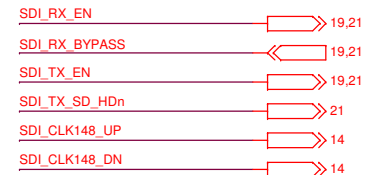
SRAM, Flash, MAX V Interface



On-board USB Blaster II Interface



SDI Interface

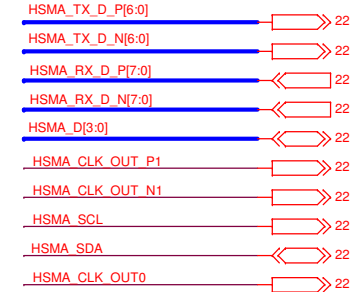


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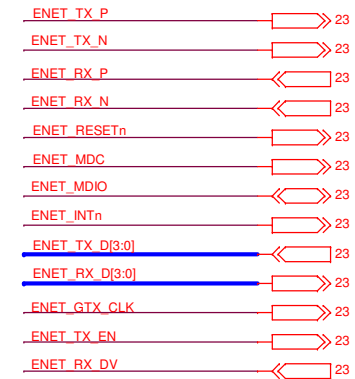
Arria V GX Bank 4



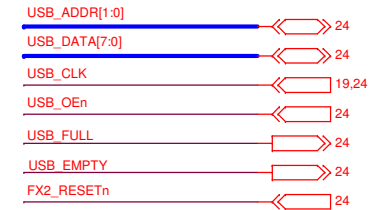
HSMC Port Interface



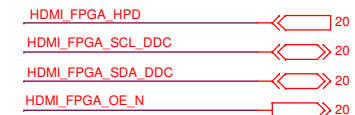
Ethernet PHY Interface



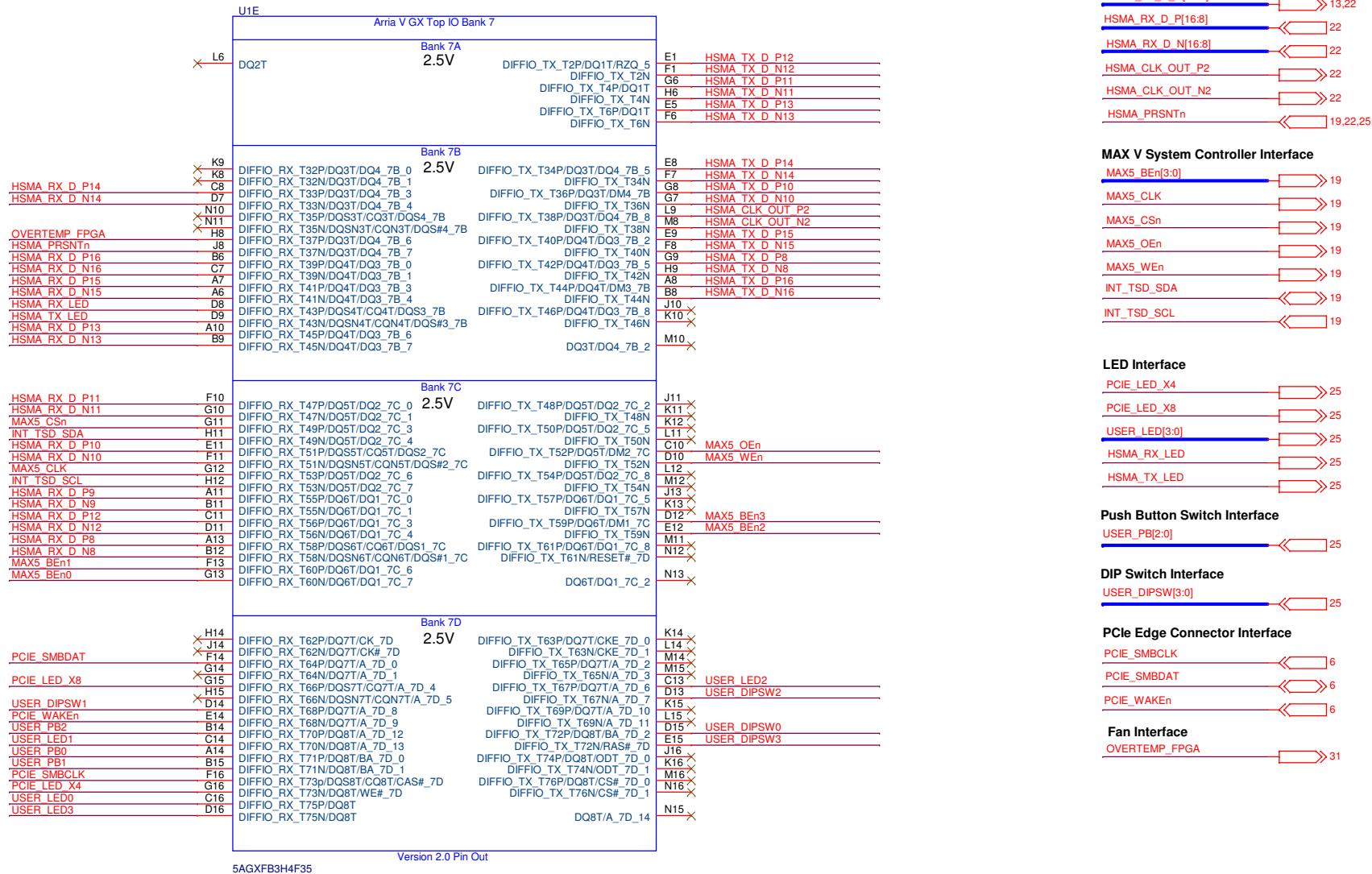
On-board USB Blaster II Interface



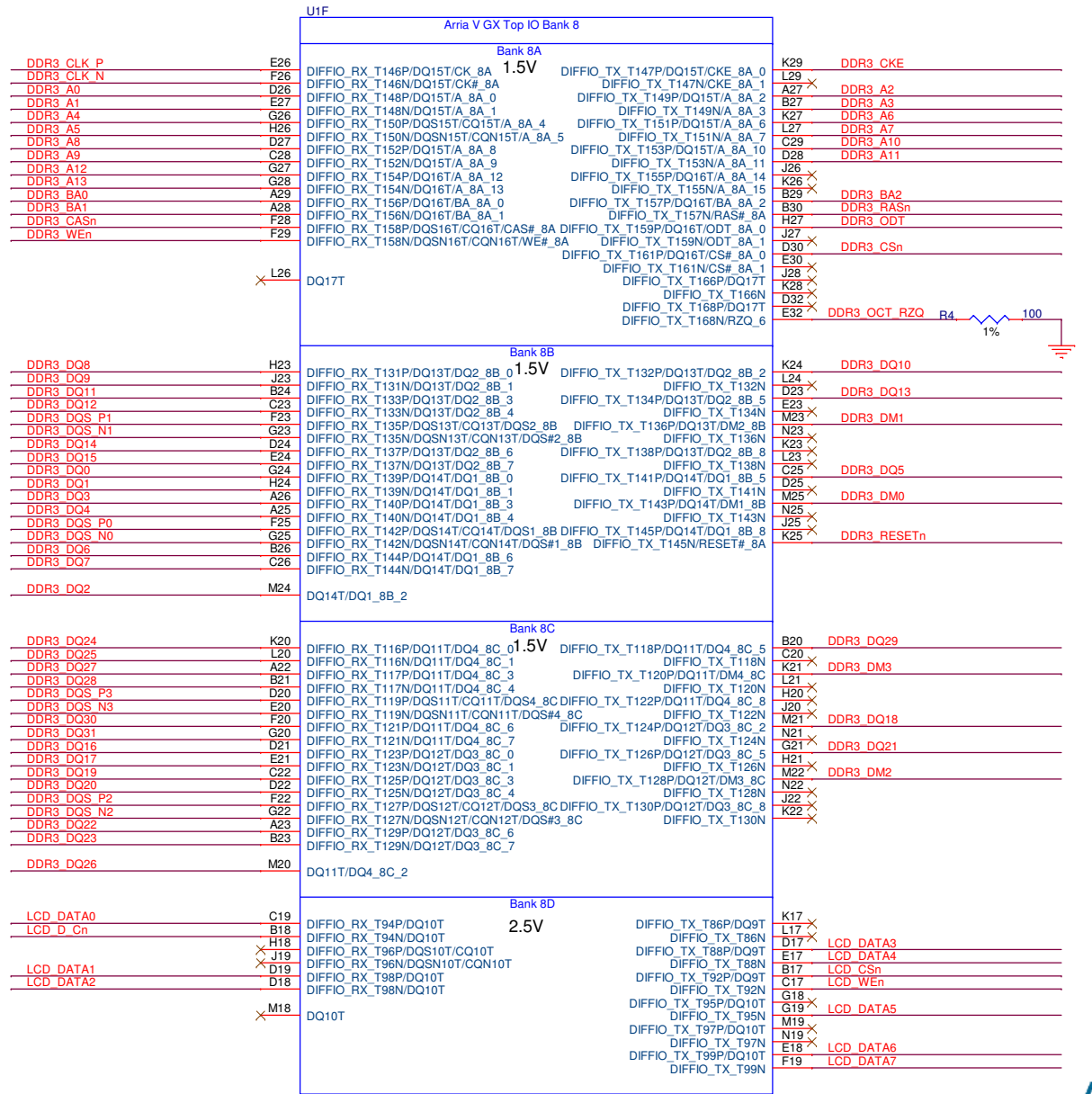
HDMI Interface



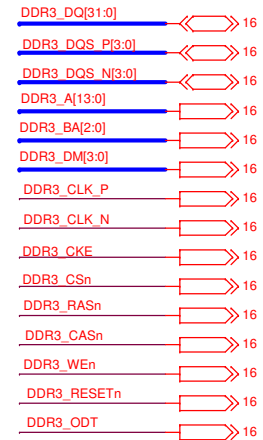
Arria V GX Bank 7



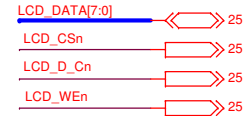
Arria V GX Bank 8



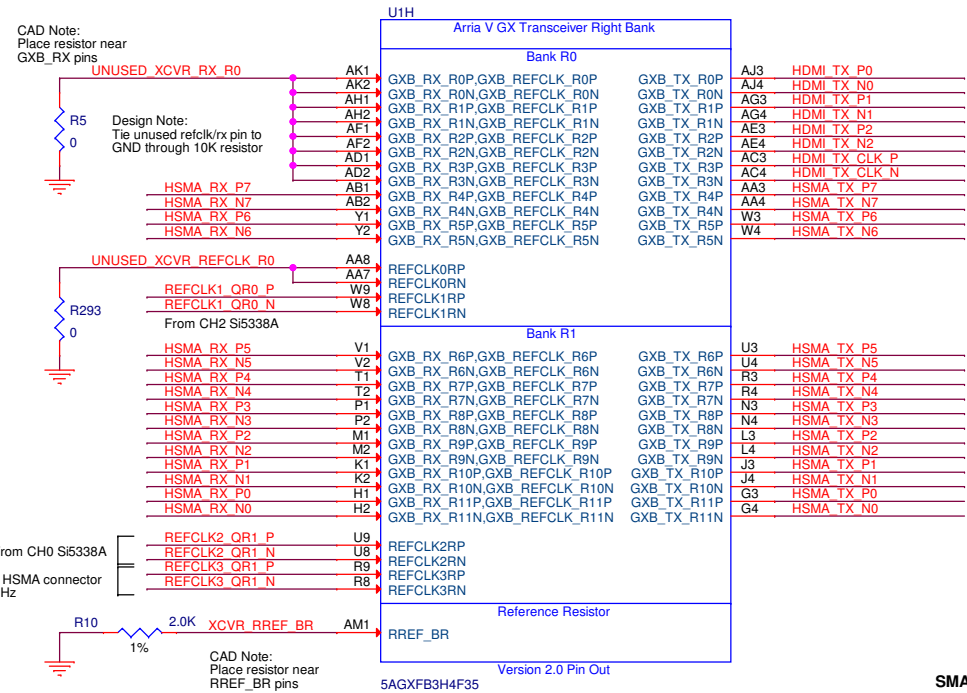
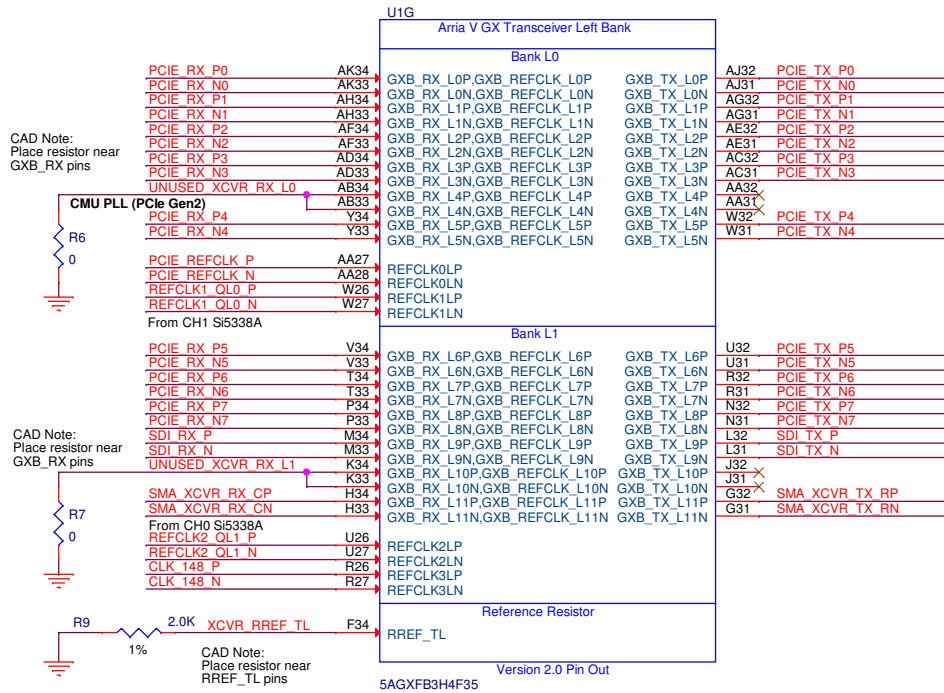
DDR3 X32 SDRAM INTERFACE



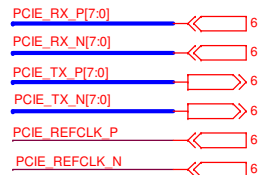
2x16 LCD DISPLAY INTERFACE



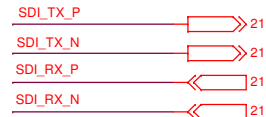
Arria V GX Transceivers Banks



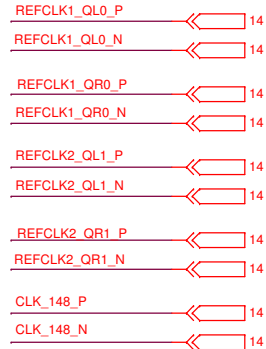
PCIe Connector Interface



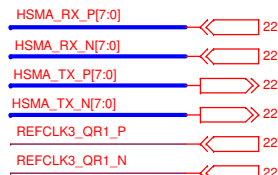
SDI Cable Driver/Equalizer Interface



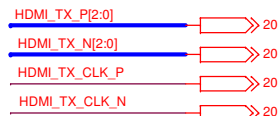
PLL Interface



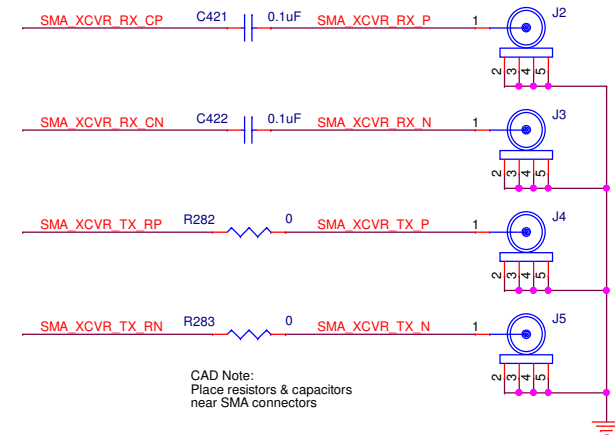
HSM Connector Interface



HDMI Level Shifter Interface



SMA Connector Interface



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Arria V GX Configuration

U1A

Arria V GX Configuration

Bank 3A

FPGA_DCLK AM32
FPGA_CONFIG_D0 AN34
FPGA_CONFIG_D1 AN33
FPGA_CONFIG_D2 AP33
FPGA_CONFIG_D3 AM33
FPGA_CONFIG_D4 AM34

Bank 4A

AL7 DATA5/DIFFIO_RX_B155N/DQ16B
AM7 DATA6/DIFFIO_RX_B155P/DQ16B
AP6 DATA7/DIFFIO_RX_B157N/DQSN16B/CQN16B
AP5 DATA8/DIFFIO_RX_B157P/DQSN16B/CQ16B
AM5 DATA9/DIFFIO_RX_B159N/DQ16B
AP8 DATA10/DIFFIO_TX_B154N
AP7 DATA11/DIFFIO_TX_B154P/DQ16B
AM6 DATA12/DIFFIO_TX_B156N
AN6 DATA13/DIFFIO_TX_B156P/DQ16B
AE7 DATA14/DIFFIO_TX_B158N
AF7 DATA15/DIFFIO_TX_B158P/DQ16B

Bank 7A

C6 DEV_OE/DIFFIO_RX_T10P/DQ2T
D5 DEV_CLRND/DIFFIO_RX_T10N/DQ2T
C4 CRC_ERROR/DIFFIO_RX_T12N/DQSN2T/CQN2T
D6 INIT_DONE/DIFFIO_RX_T14P/DQ2T
E6 NCE/DIFFIO_RX_T14N/DQ2T

Bank 8A

C34 CONF_DONE
B34 NSTATUS
C33 NCONFIG
A33 NCE

Do Not Use

E33 DNU_1
F33 DNU_2
AL32 DNU_3
AD18 DNU_4

Version 2.0 Pin Out

5AGXFB3H4F35

On-board USB Blaster II Interface

AN32 JTAG_TCK
AF30 JTAG_TMS
AC28 JTAG_FPGA_TDO
AC29 JTAG_BLAISTER_TDO

2.5V_VCCIO_VCCPD_VCCPGM

R12 10K
R13 10K
R14 10K
R11 10K

A2
B2
A5
A4
J7
K7
B5

MAX V System Controller Interface

FPGA_CONFIG_D[15:0]
FPGA_DCLK
MSEL[4:0]
FPGA_CONF_DONE
FPGA_nSTATUS
FPGA_nCONFIG
FPGA_CvP_CONF_DONE
FPGA_PR_ERROR
FPGA_PR_READY
FPGA_PR_DONE
FPGA_PR_REQUEST

Push Button Interface

CPU_RESETn

PCIe Edge Connector Interface

PCIe_PERSTn

2.5V_VCCIO_VCCPD_VCCPGM

R294 0
R296 0
R298 0
R300 0
R302 0
R295 DNI
R297 DNI
R299 DNI
R301 DNI
R303 DNI

CAD Note:
Overlap resistor pads

Design Note:
Remove pull up/pull down resistors
and populate series resistors before
changing the MSEL setting by
editing MAX V system controller
code

Default Configuration Mode:
- MSEL[4:0] = 00000
- FPP x16
- Fast POR Delay
- Decompression feature is disabled
- Design Security feature is disabled

Warning!!
Follow MSEL setting in datasheet strictly
to avoid undesirable behavior of FPGA

Design Note:
Optional termination resistor
for DCLK

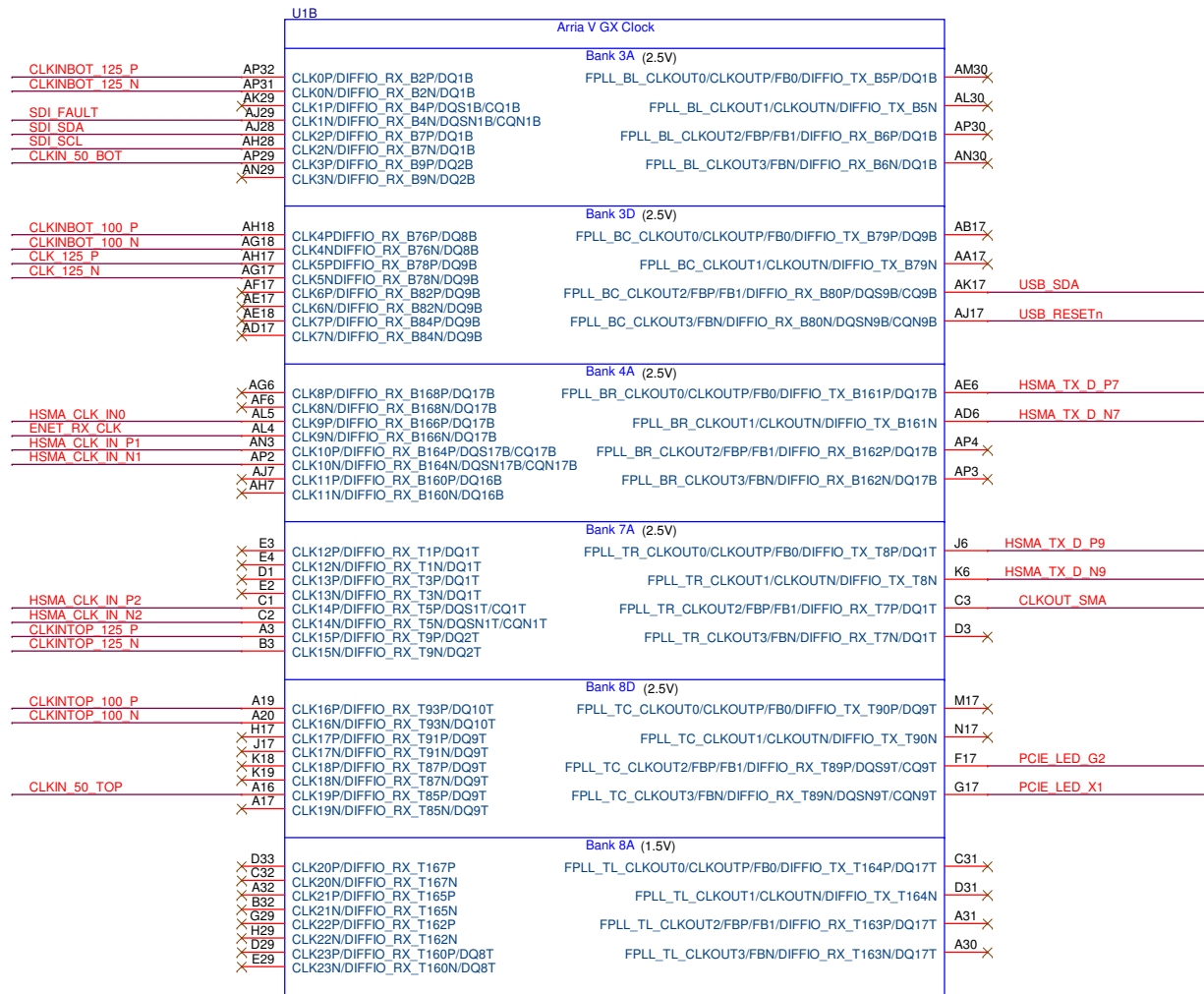
CAD Note:
Place near FPGA DCLK pin

2.5V_VCCIO_VCCPD_VCCPGM
R23 DNI
R24 DNI
C25 DNI
R25 DNI

ALTERA

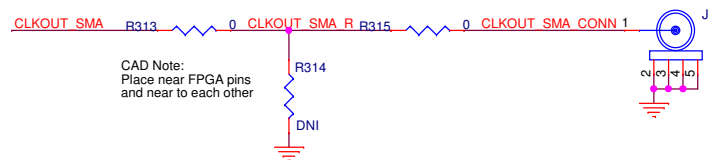
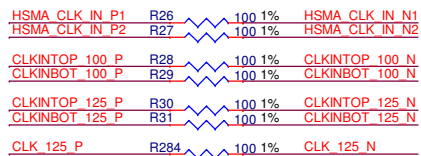
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Arria V GX Clock

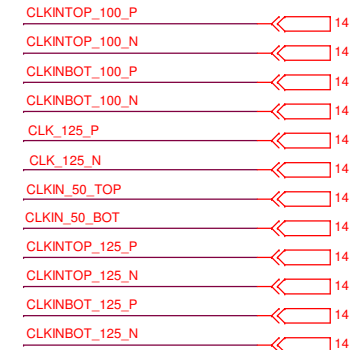


LVDS Clock Input Termination

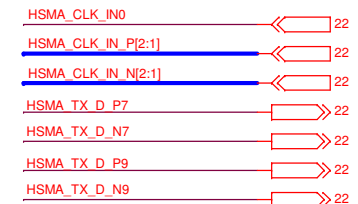
CAD Note:
Place near FPGA pins



PLL Interface



HSMC PORT Interface



On-board USB Blaster II Interface



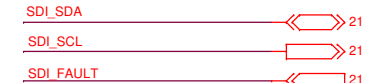
LED INTERFACE



Ethernet PHY INTERFACE

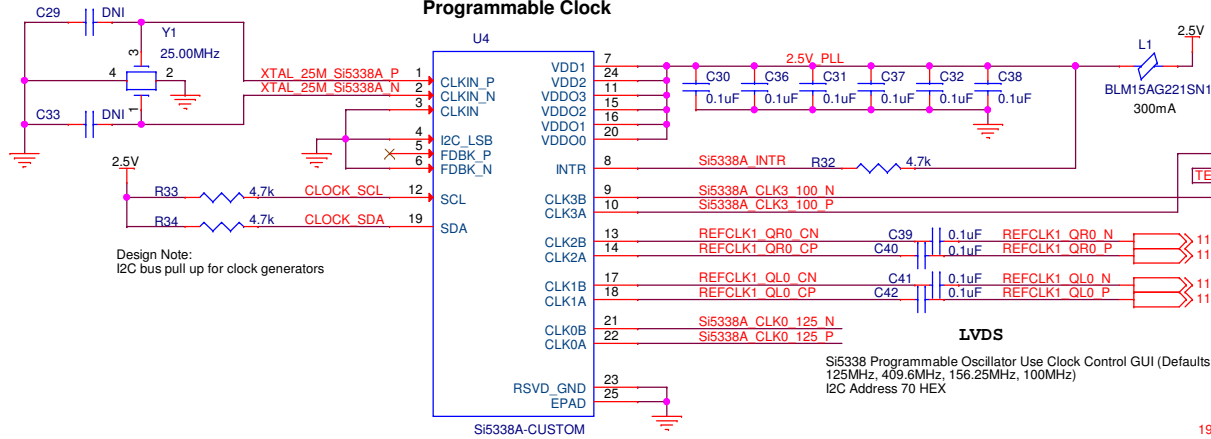


SDI Interface

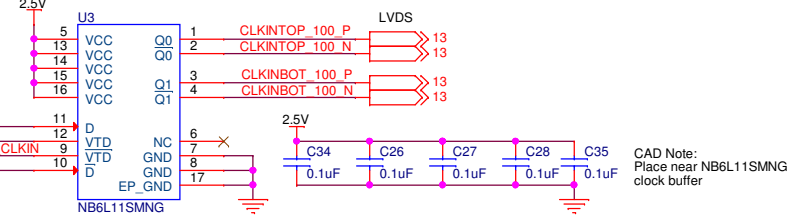


PLL

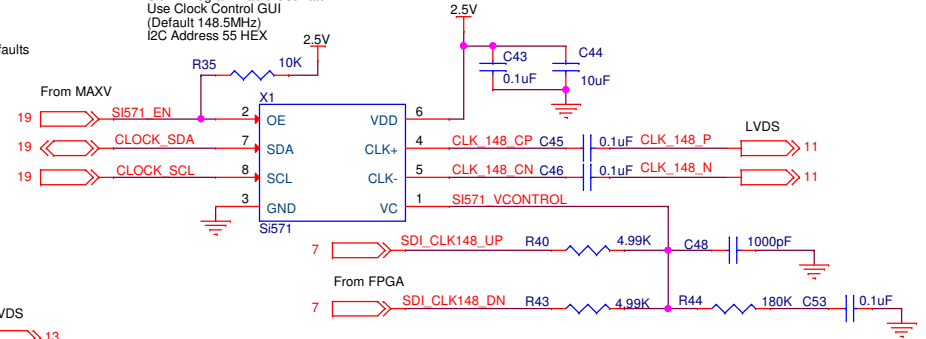
Programmable Clock



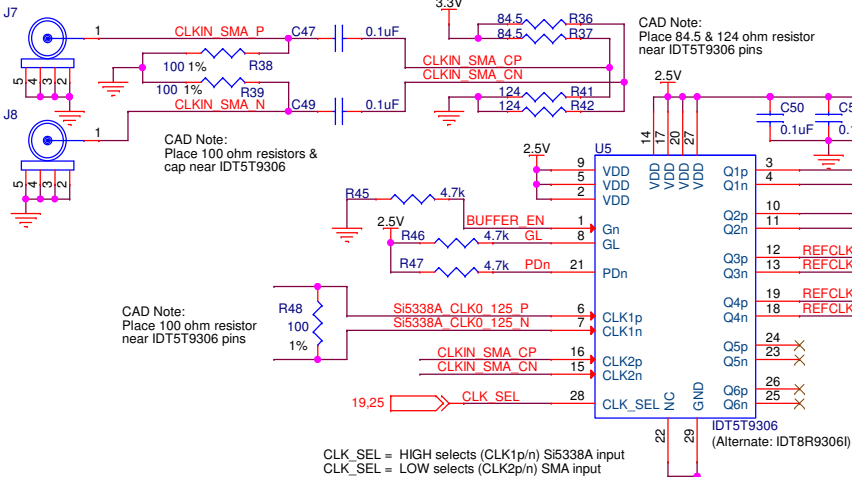
100MHz Clock Distribution to Top & Bottom Banks



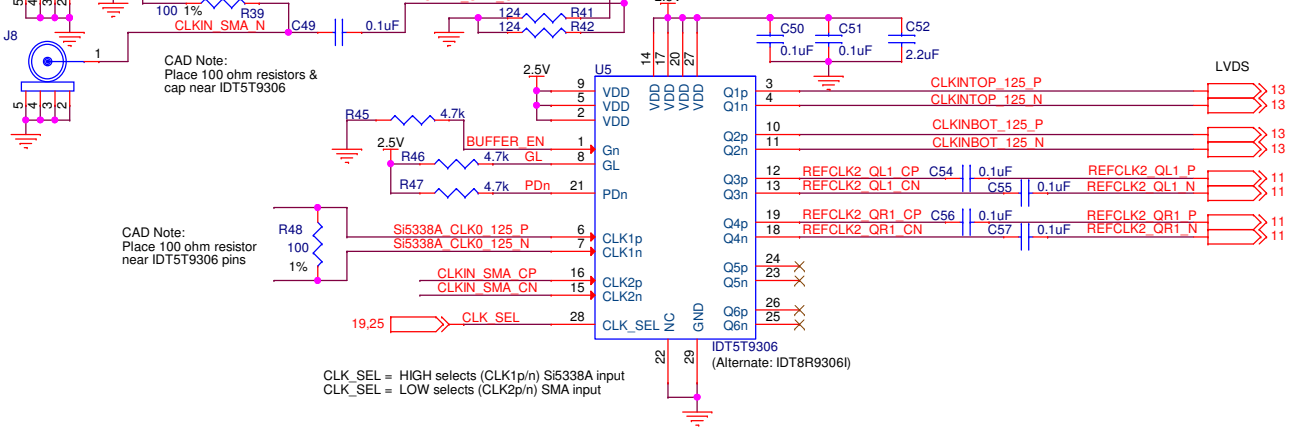
SDI Reference Clocks



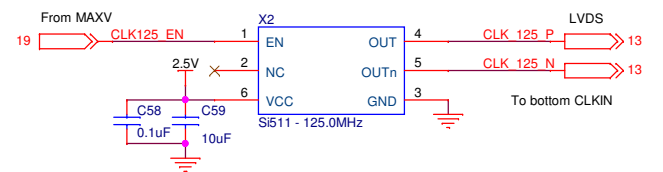
User Clock Input



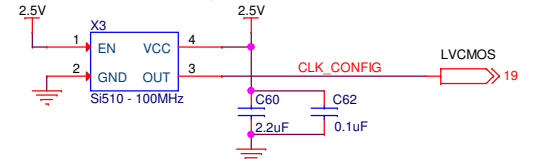
Clock Distribution to Top & Bottom Left & Right Transceiver Banks



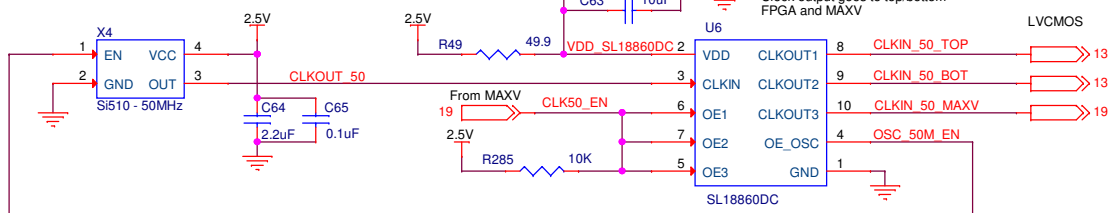
125MHz Clocks for ENET

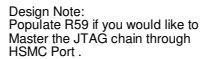


100MHz Configuration Clock



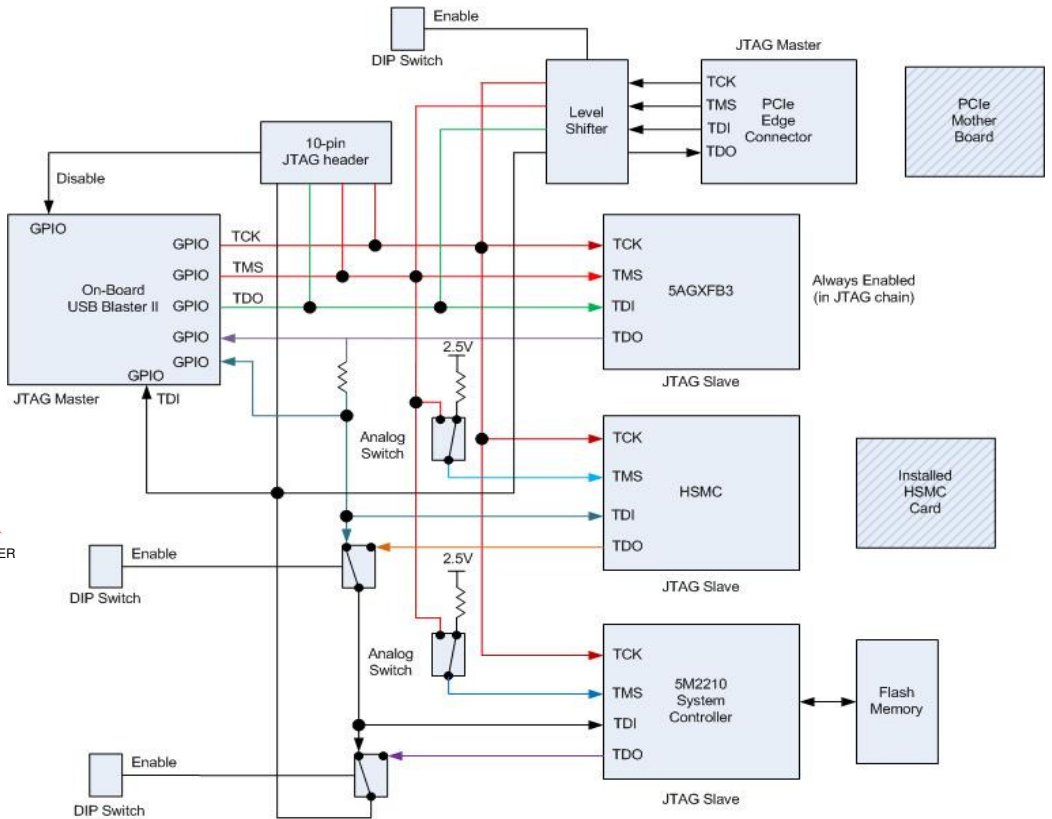
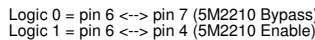
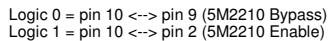
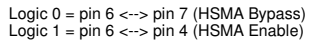
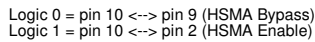
50MHz LVMOS Clocks for FPGA and MAXV



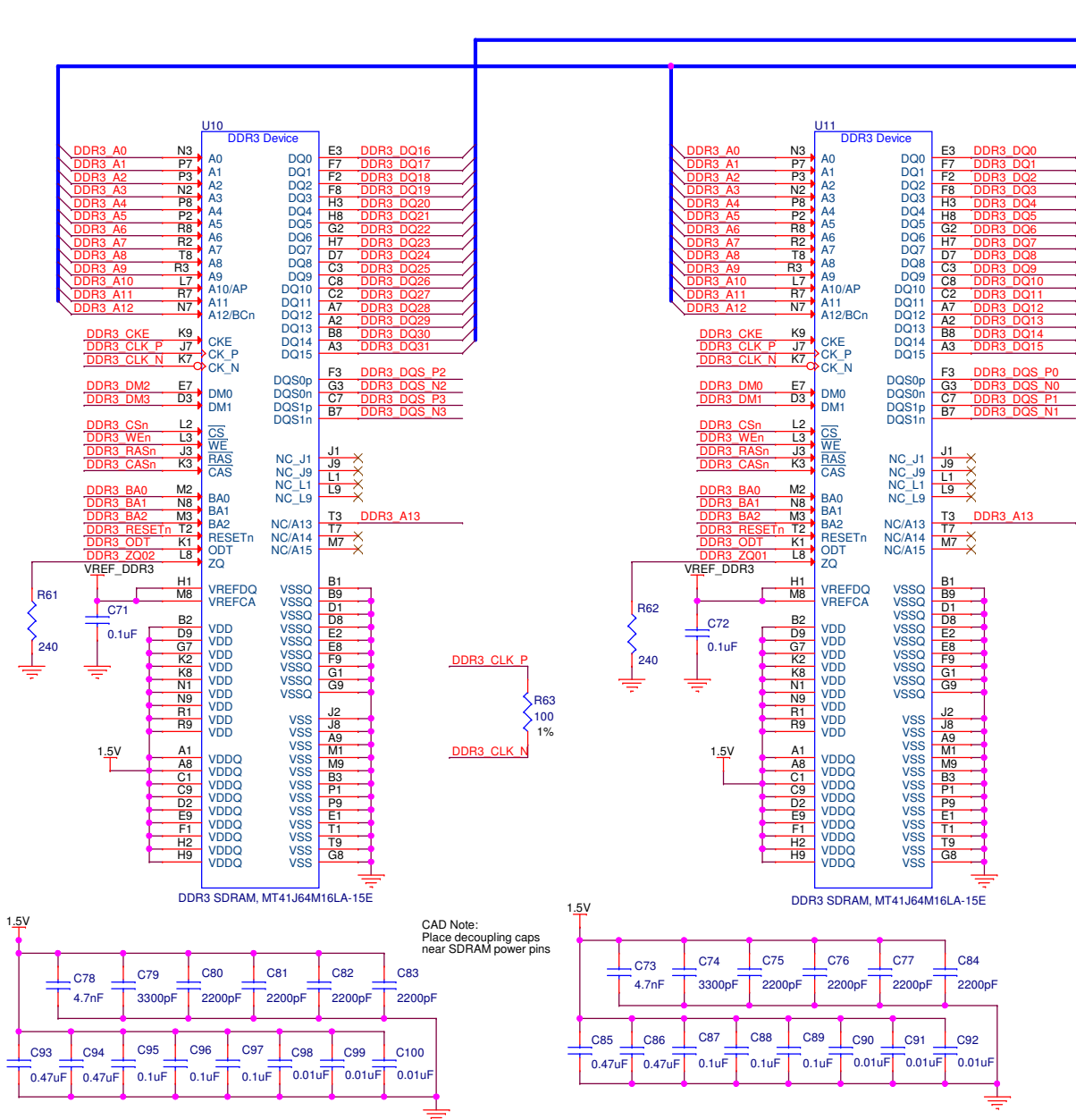


TS5A23157 Switch Functions

When Pins 1 & 5 are:
 LOW --> NC to/from COM = ON and NO to/from COM = OFF
 HIGH --> NC to/from COM = OFF and NO to/from COM = ON

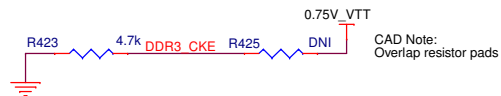


256MB DDR3 x32 SDRAM



Arria V Interface

| | |
|-----------------|----|
| DDR3_DQ[31:0] | 10 |
| DDR3_A[13:0] | 10 |
| DDR3_DQS_P[3:0] | 10 |
| DDR3_DQS_N[3:0] | 10 |
| DDR3_BA[2:0] | 10 |
| DDR3_DM[3:0] | 10 |
| DDR3_CKE | 10 |
| DDR3_CLK_P | 10 |
| DDR3_CLK_N | 10 |
| DDR3_CSn | 10 |
| DDR3_WEn | 10 |
| DDR3_RASn | 10 |
| DDR3_CASn | 10 |
| DDR3_RESEn | 10 |
| DDR3_ODT | 10 |



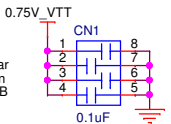
CAD Note:
Overlap resistor pads

| Signal | Pin | Value |
|----------|--------|-------|
| DDR3_A4 | RN1A 1 | 16 56 |
| | RN1B 2 | 15 56 |
| DDR3_A0 | RN1C 3 | 14 56 |
| DDR3_BA2 | RN1D 4 | 13 56 |
| DDR3_A6 | RN1E 5 | 12 56 |
| DDR3_A8 | RN1F 6 | 11 56 |
| DDR3_A1 | RN1G 7 | 10 56 |
| DDR3_A10 | RN1H 8 | 9 56 |

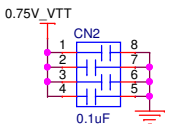
| Signal | Pin | Value |
|-------------|--------|-------|
| DDR3 RESETn | RN2A 1 | 16 56 |
| DDR3 RASn | RN2B 2 | 15 56 |
| DDR3 BA1 | RN2C 3 | 14 56 |
| DDR3 A9 | RN2D 4 | 13 56 |
| DDR3 A12 | RN2E 5 | 12 56 |
| DDR3 A11 | RN2F 6 | 11 56 |
| DDR3 A13 | RN2G 7 | 10 56 |
| DDR3 A2 | RN2H 8 | 9 56 |

| Signal | Pin | Value |
|-----------|--------|-------|
| DDR3 ODT | RN3A 1 | 16 56 |
| DDR3 A5 | RN3B 2 | 15 56 |
| DDR3 A7 | RN3C 3 | 14 56 |
| DDR3 WEn | RN3D 4 | 13 56 |
| DDR3 A3 | RN3E 5 | 12 56 |
| DDR3 CASn | RN3F 6 | 11 56 |
| DDR3 CSn | RN3G 7 | 10 56 |
| DDR3 BA0 | RN3H 8 | 9 56 |

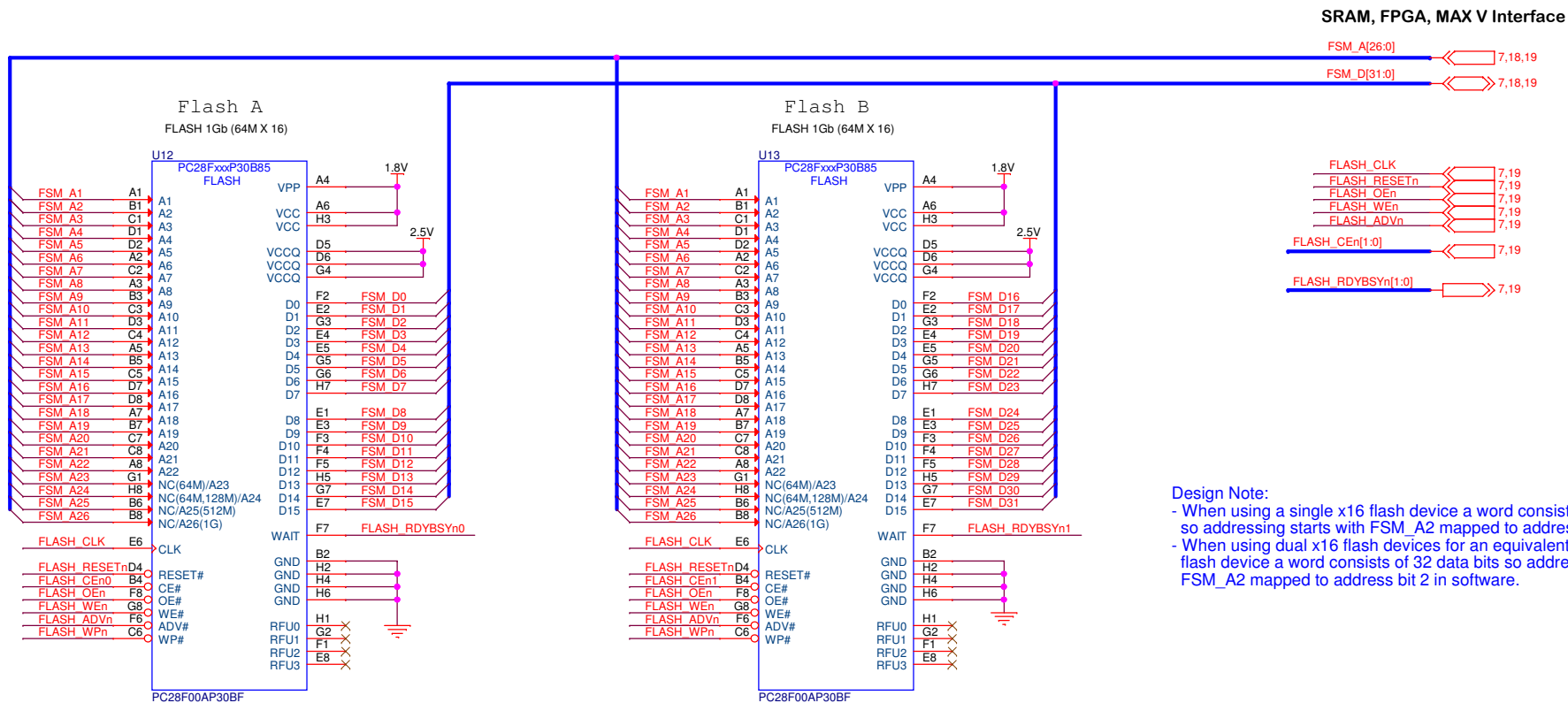
CAD Note:
Use tree-topology for termination signals
Use star via to branch out address/
command/control signals from FPGA
to memory devices and termination resistors



CAD Note:
Place cap arrays near
resistor packs and on
the same side of PCB



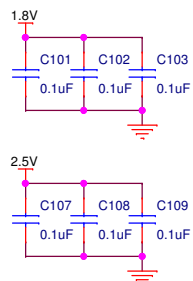
Flash



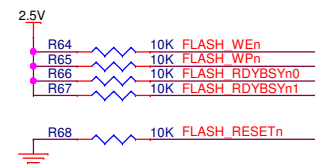
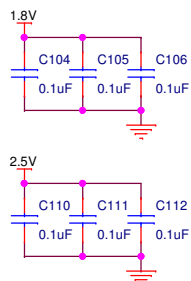
Design Note:

- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FSM_A2 mapped to address bit 1 in software.
- When using dual x16 flash devices for an equivalent x32 (x16||x16) flash device a word consists of 32 data bits so addressing starts with FSM_A2 mapped to address bit 2 in software.

Place capacitors near Flash A

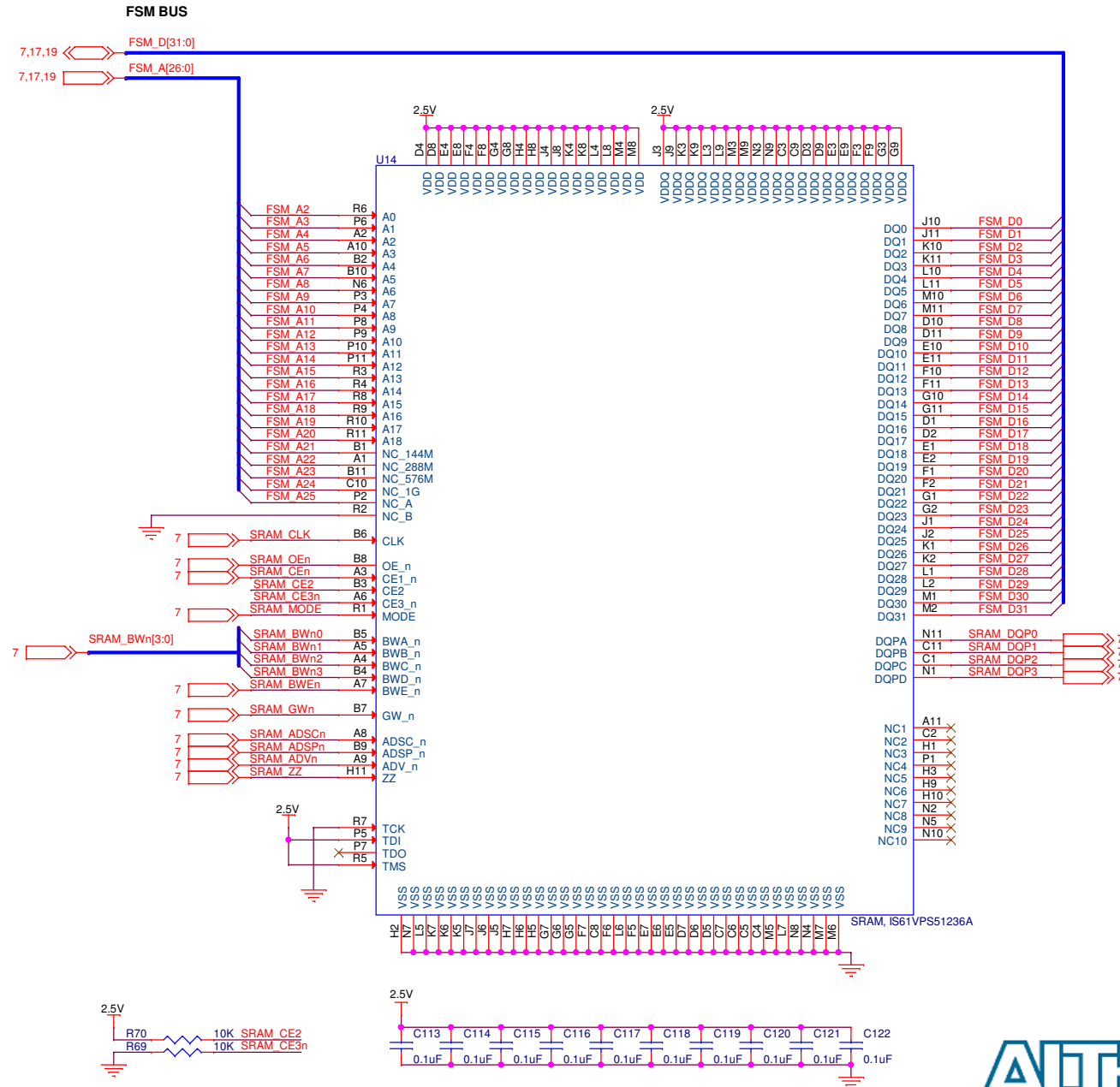


Place capacitors near Flash B

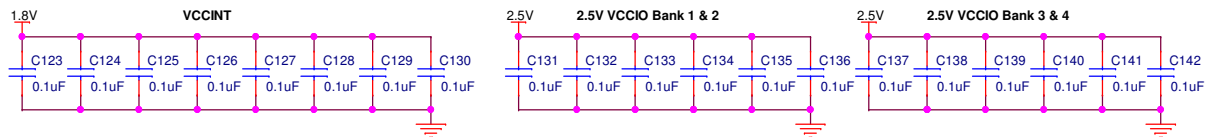
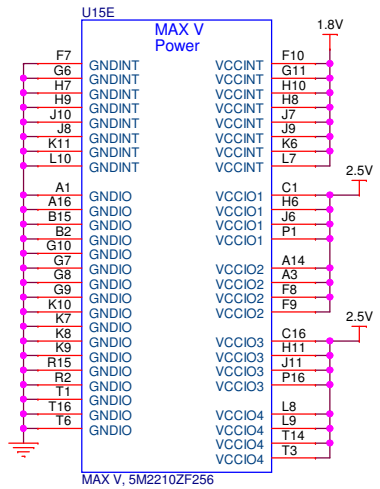
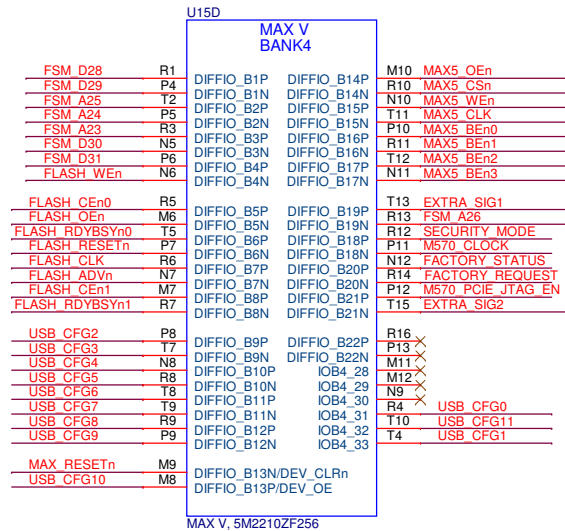
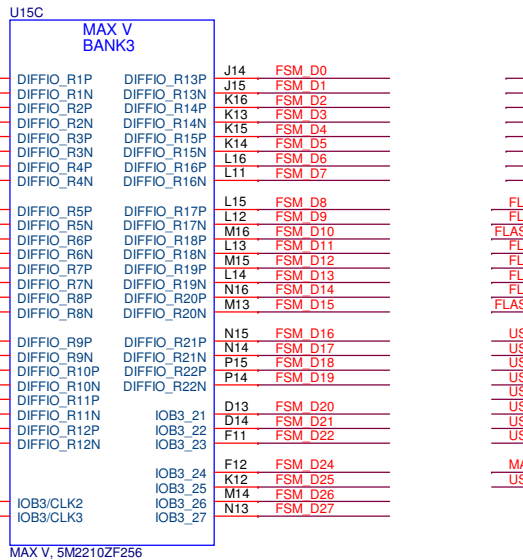
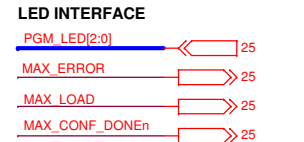
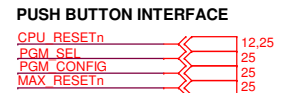
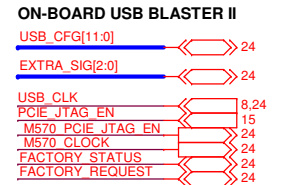
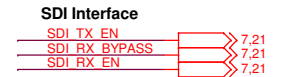
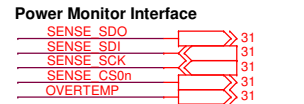
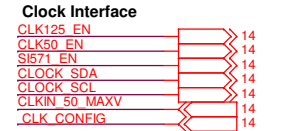
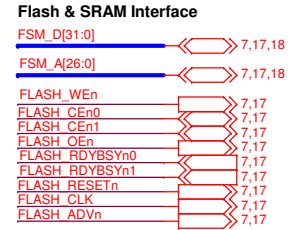
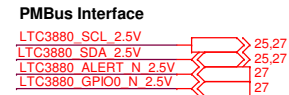
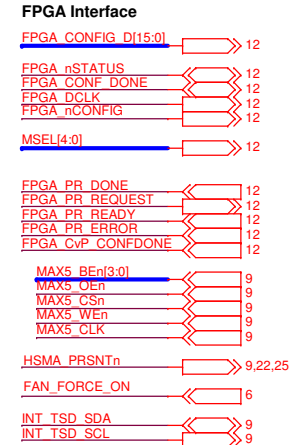
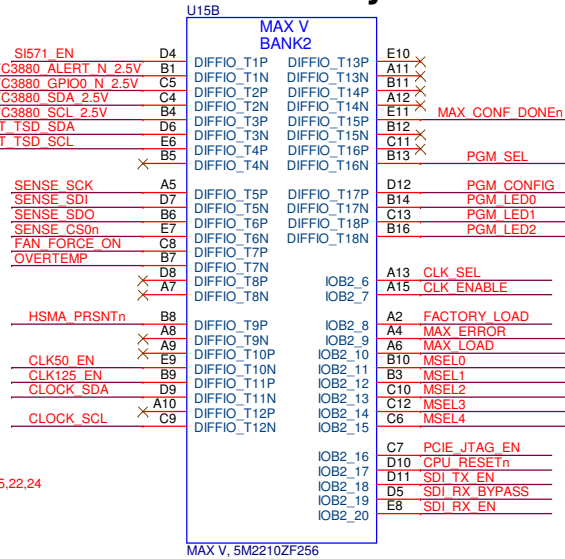
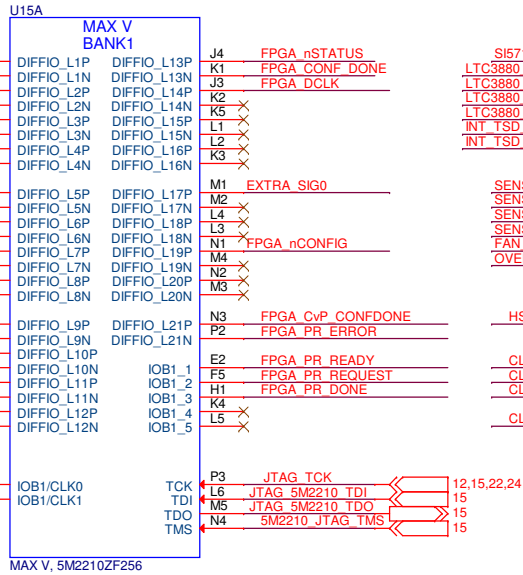


ALTERA

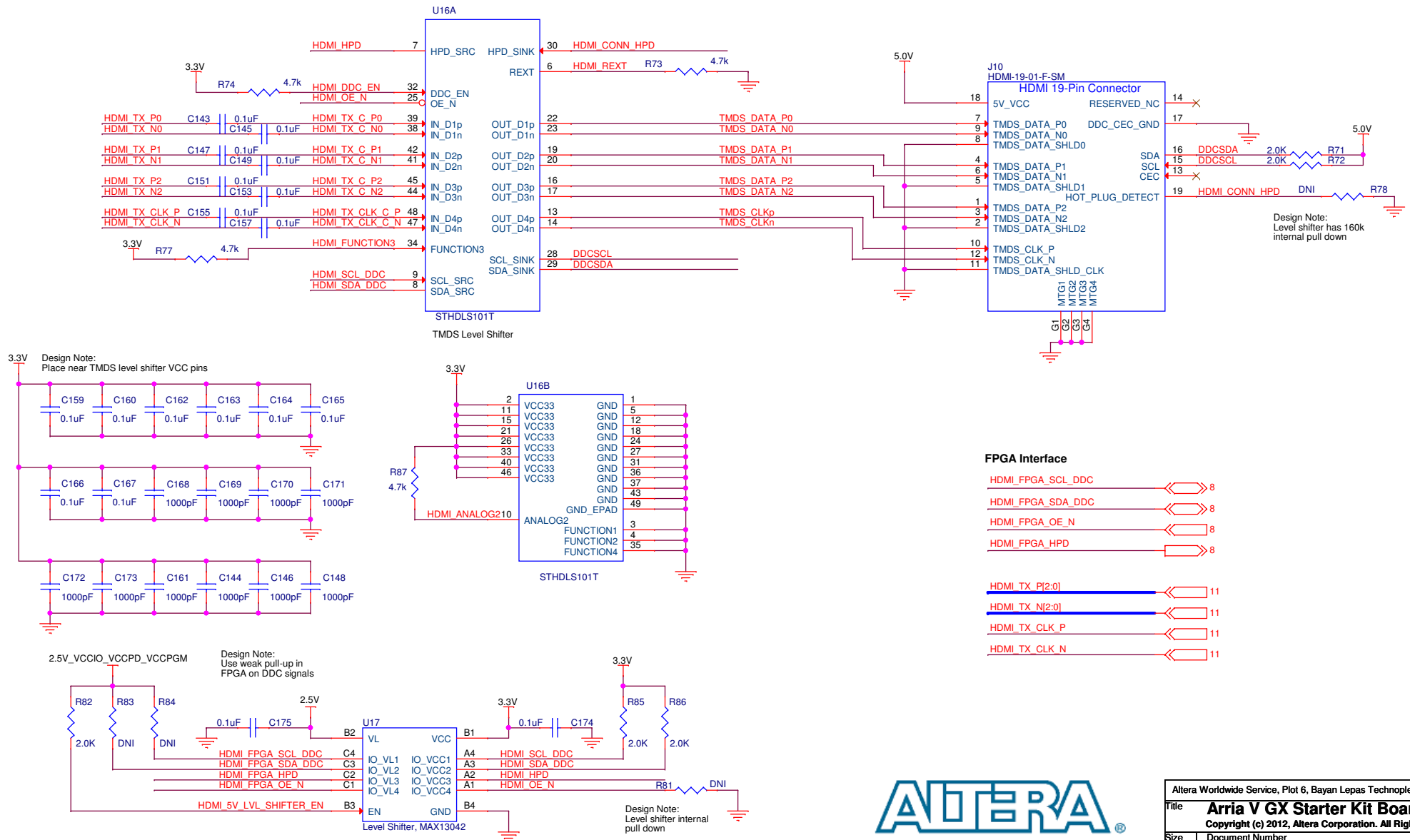
SRAM



5M2210 System Controller

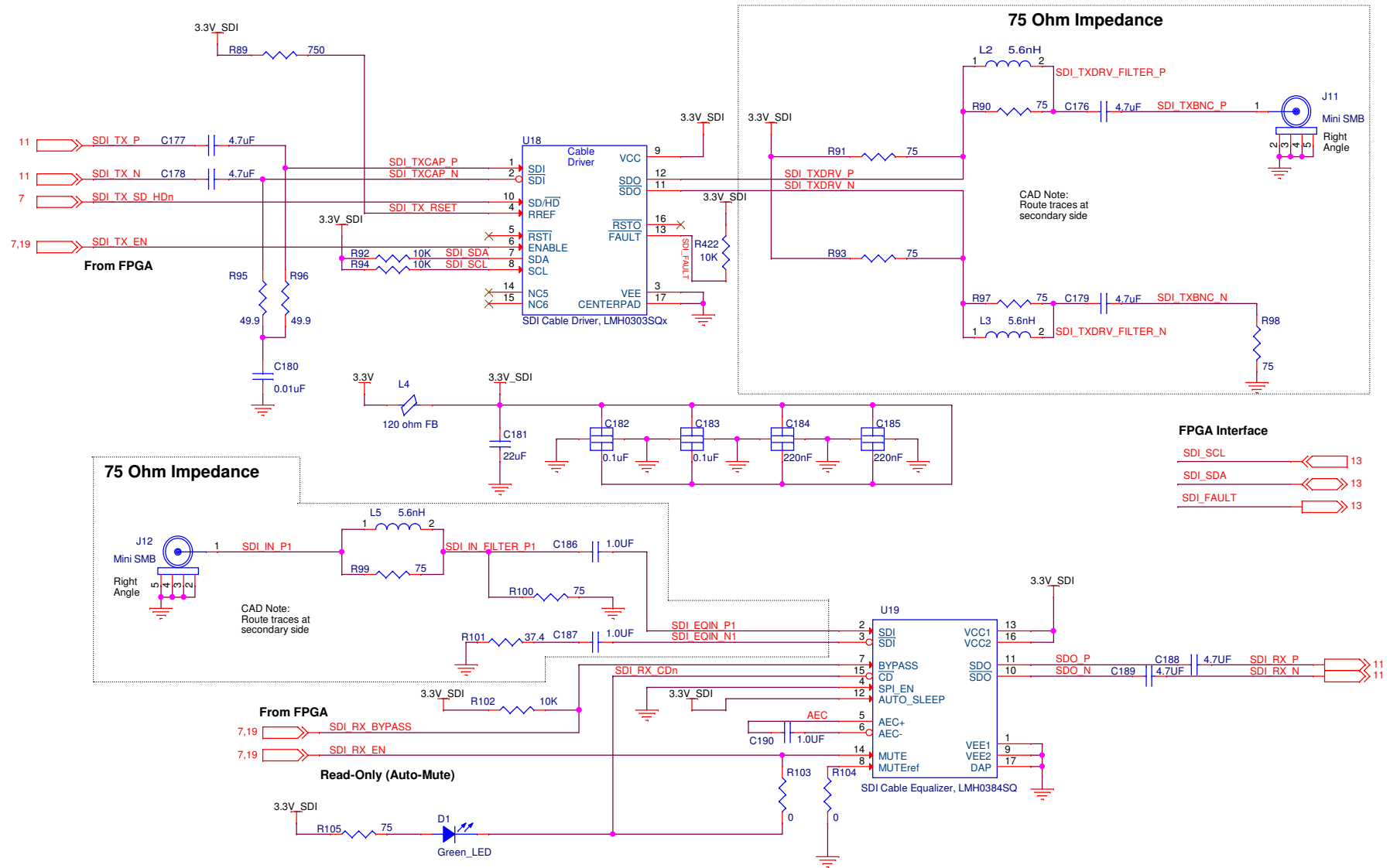


HDMI Video Output



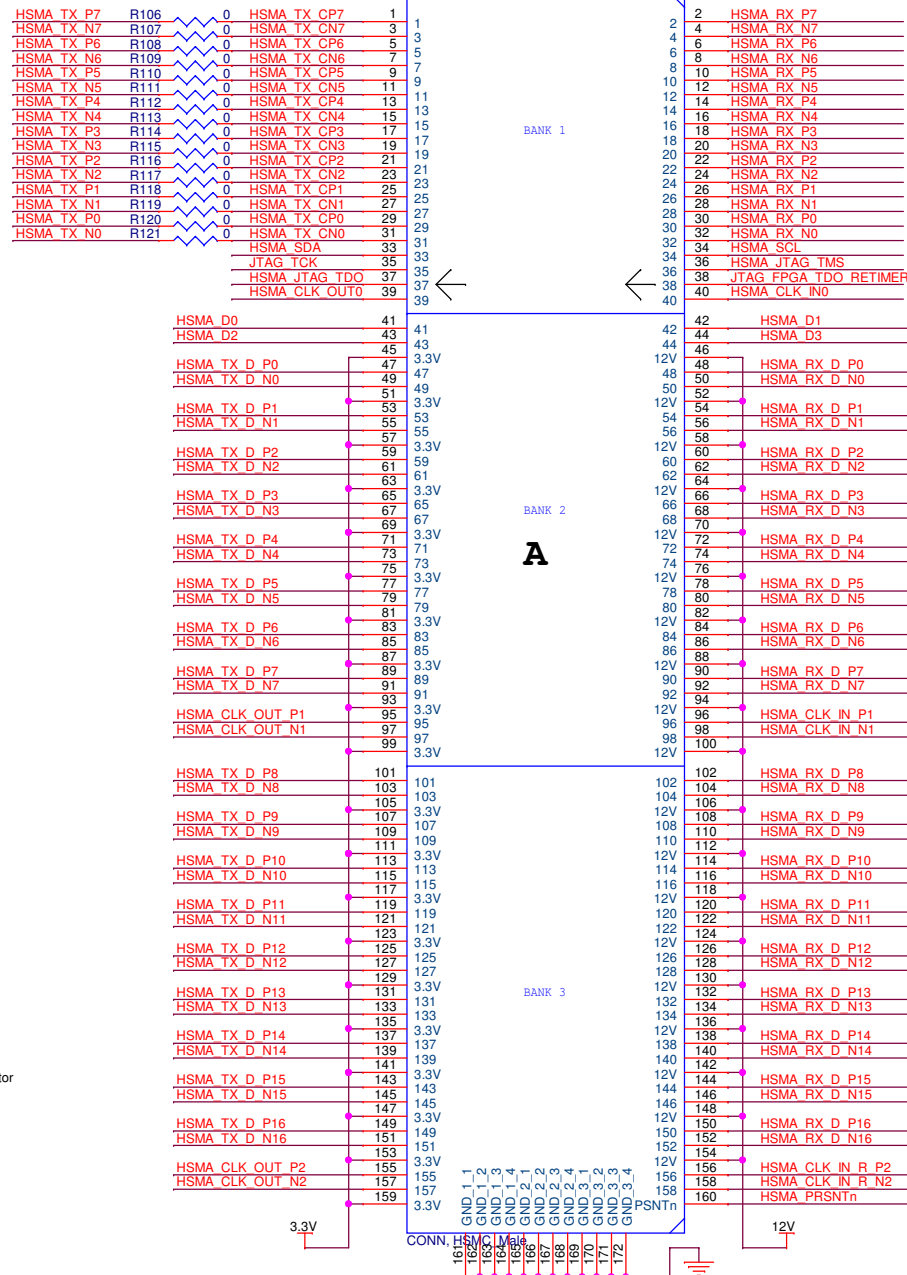
| | | |
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SDI Cable Driver, Equalizer, and SMB

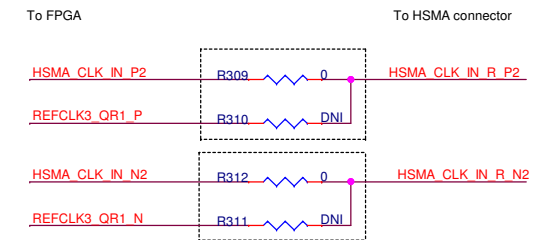
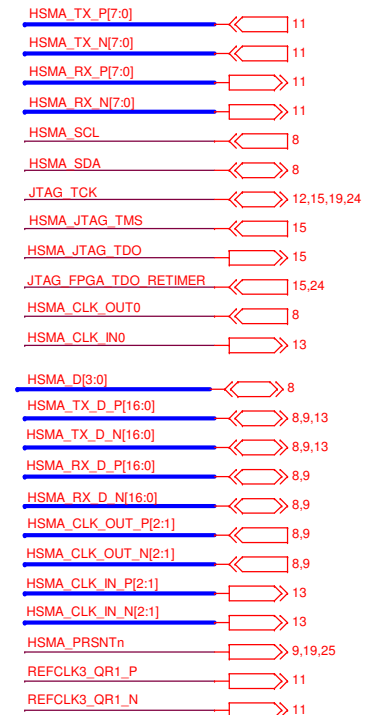


HSMC Port

Cad Note:
Place resistors near HSMC connector



FPGA Interface



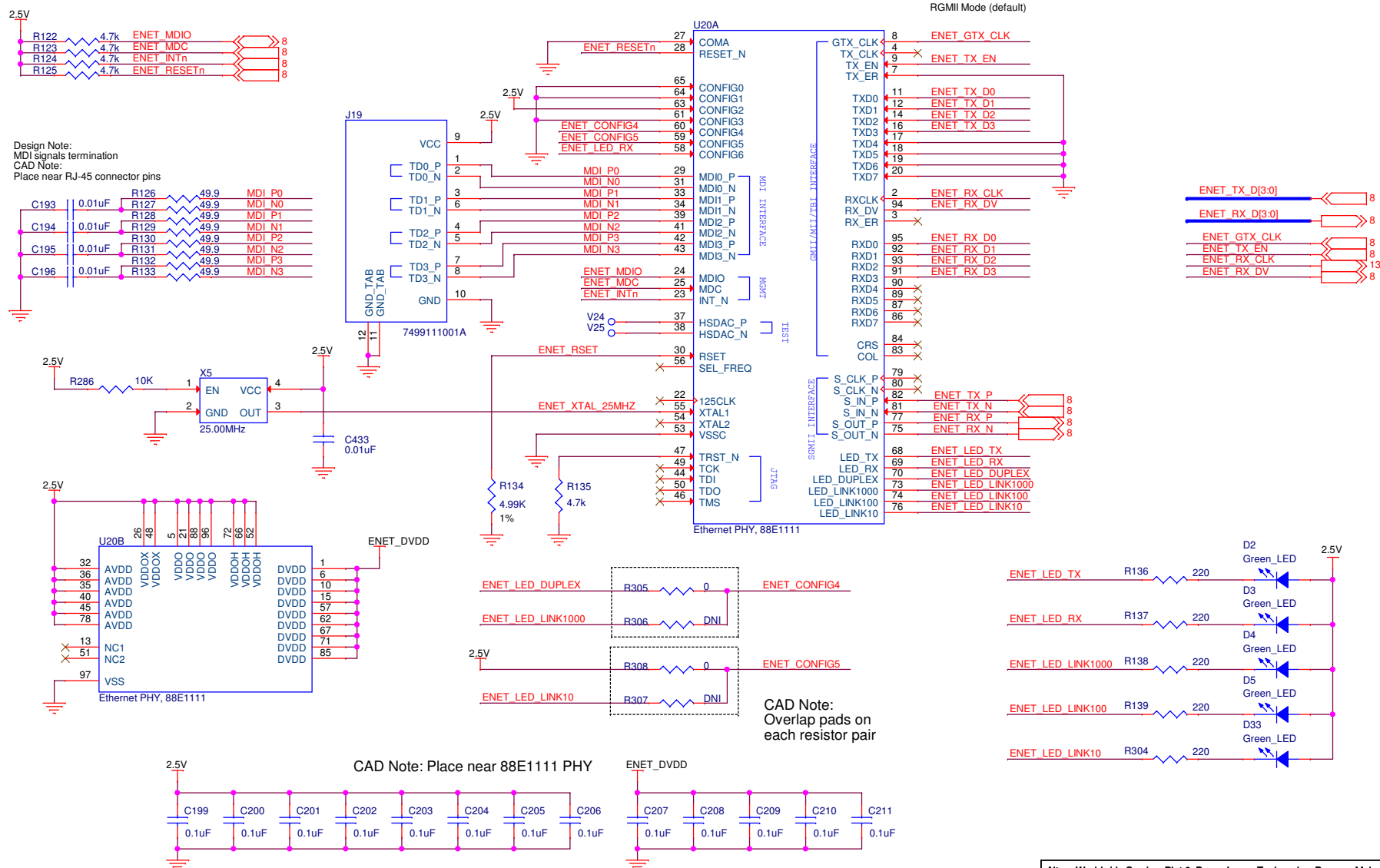
Design Note:
If HSMC-to-PCle adapter board is used and FPGA is configured as PCle root port, remove R309 & R312 and populate R310 & R311 with 0 ohm resistors

CAD Note:
Overlap pads on each resistor pair

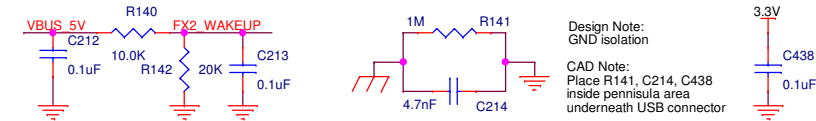


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|--|--|-------|----------|
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10/100/1000 Ethernet

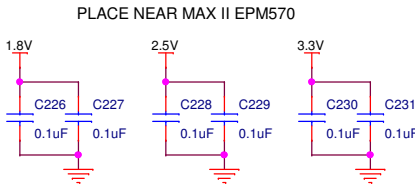
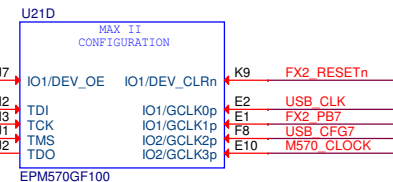
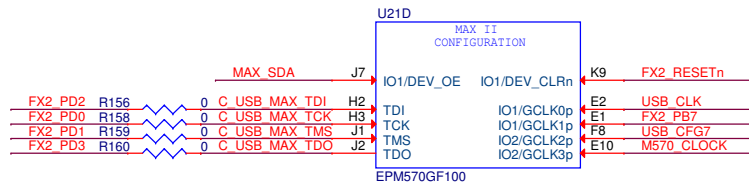
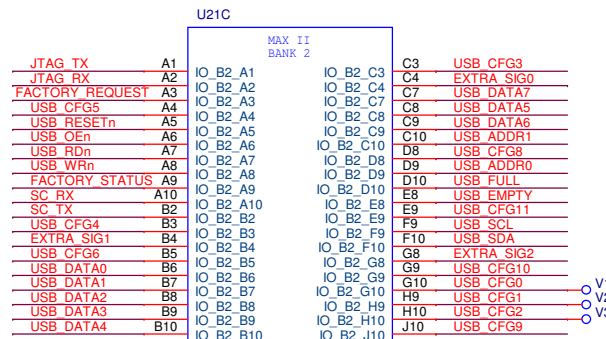
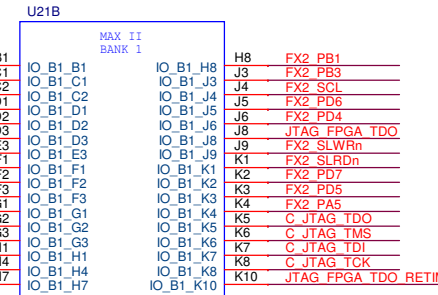
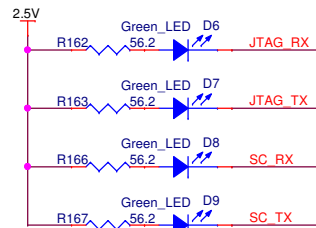
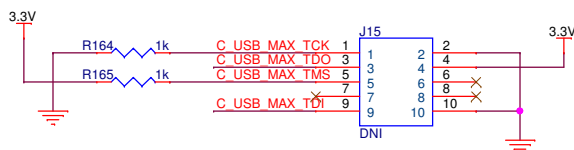
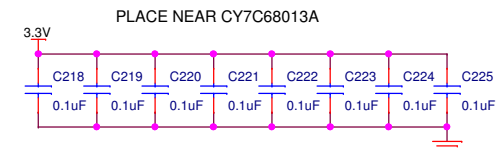
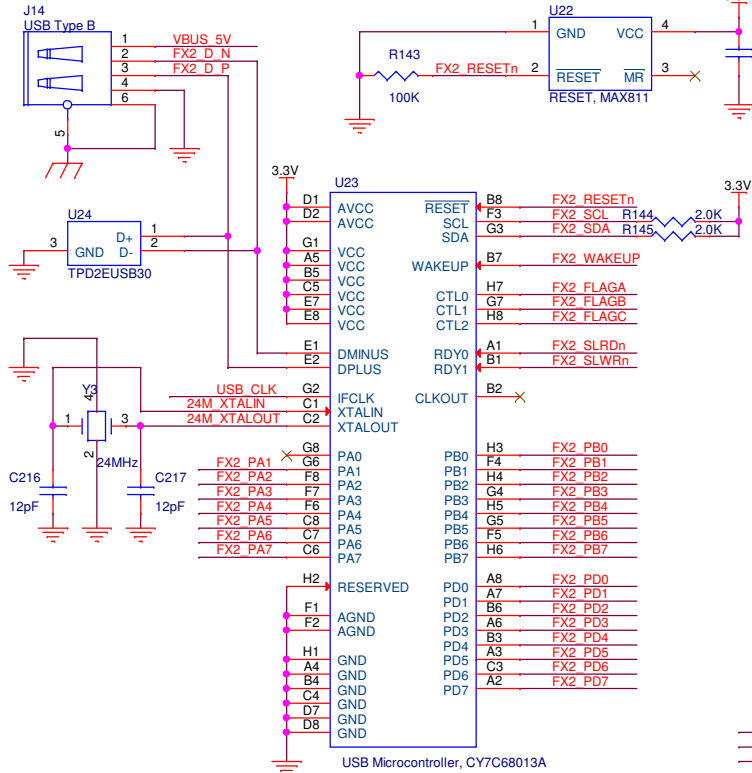


USB Blaster II



Design Note:
GND isolation

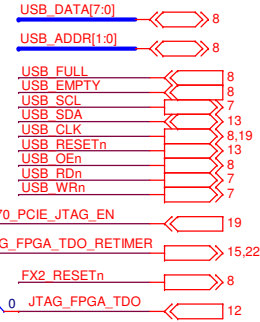
CAD Note:
Place R141, C214, C438
inside peninsula area
underneath USB connector



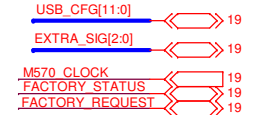
PLACE NEAR MAX II EPM570



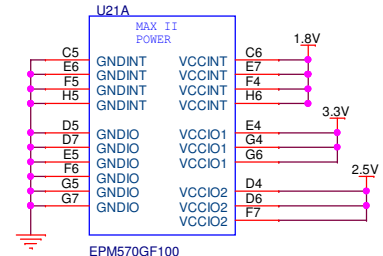
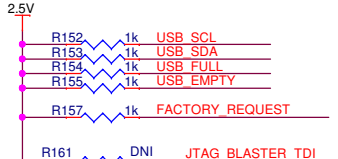
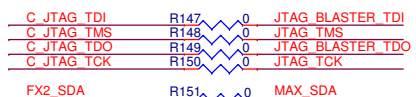
Arria V USB Interface



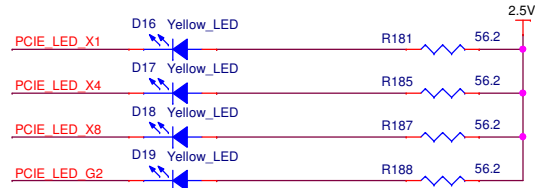
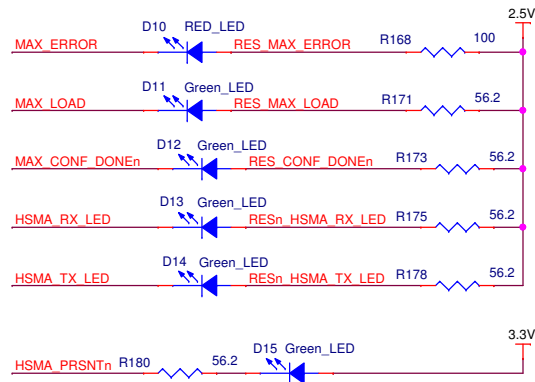
MAX V USB INTERFACE



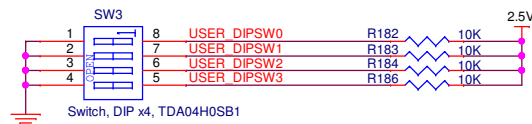
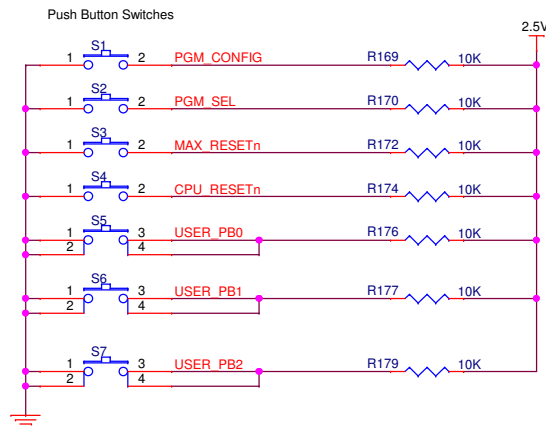
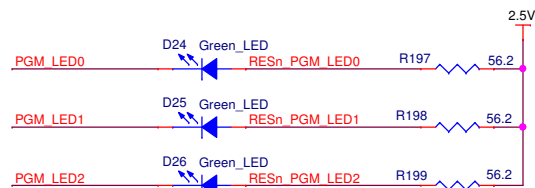
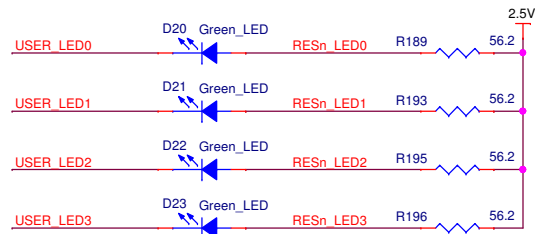
JTAG INTERFACE



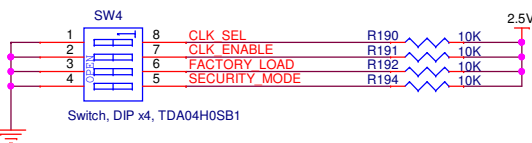
User IO & Connector



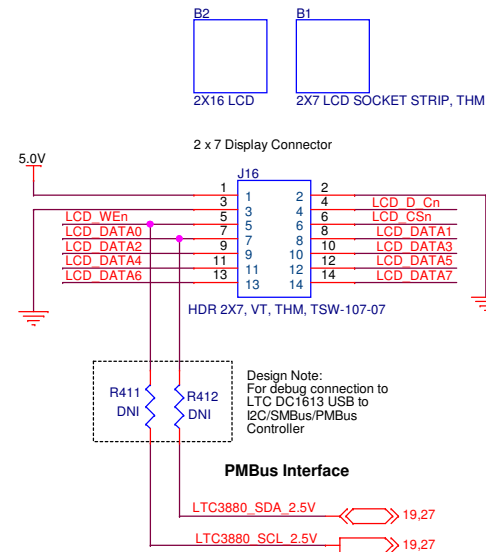
Design Note:
PCie GEN2 link indication



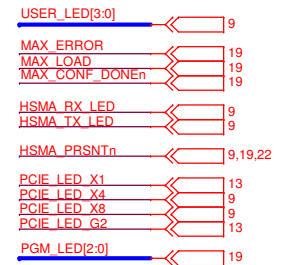
ON = 0
OFF = 1



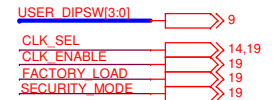
BOARD SETTINGS DIPSWITCH



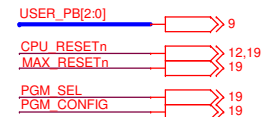
LED INTERFACE



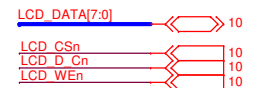
DIP SWITCH INTERFACE



PUSH BUTTON INTERFACE

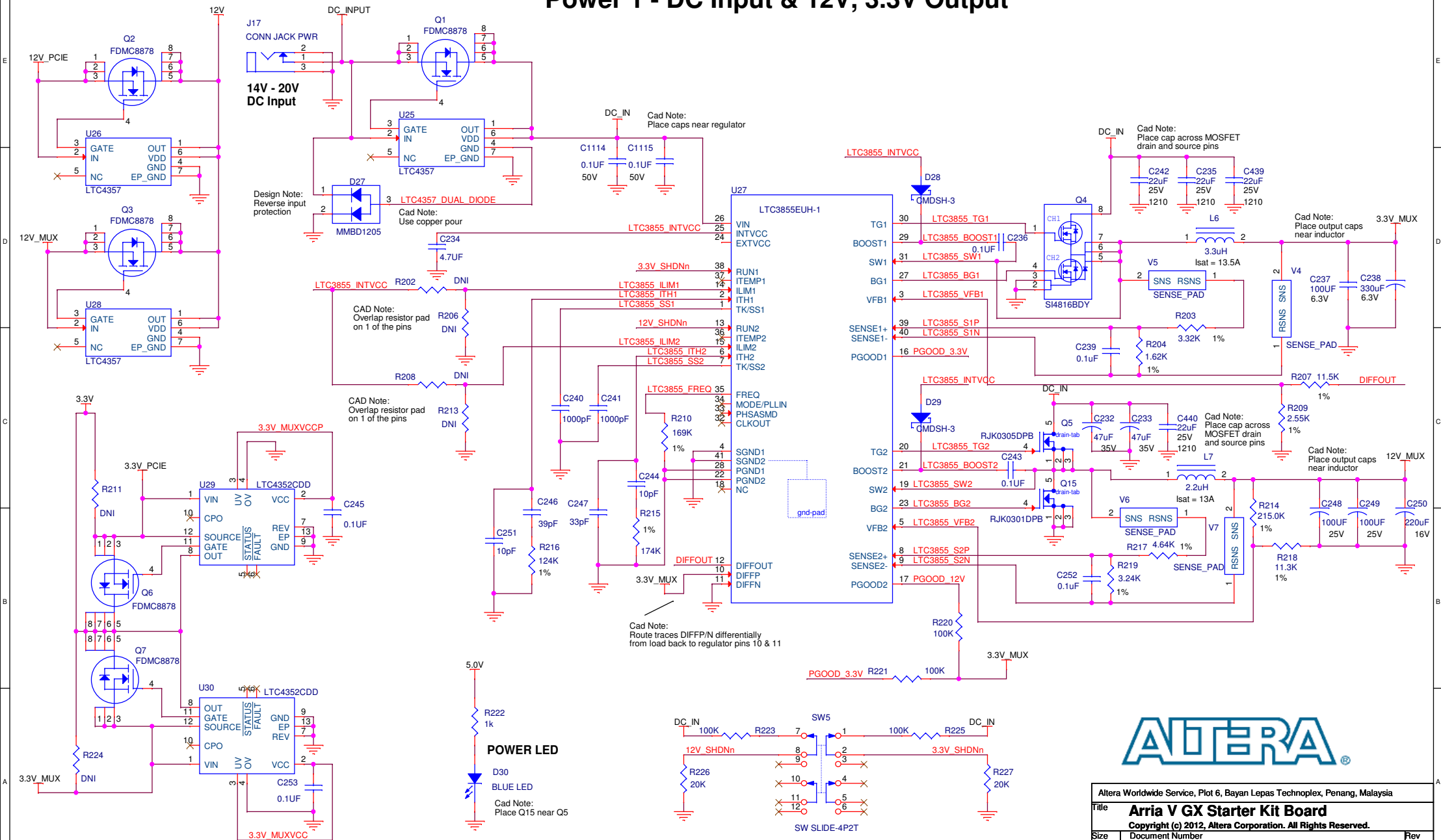


2x16 LCD DISPLAY INTERFACE



| | | | |
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| Date: | Wednesday, October 17, 2012 | Sheet | 25 of 35 |

Power 1 - DC Input & 12V, 3.3V Output



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| | |
|-------|-------------------------------------|
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|-------|-------------------------------------|

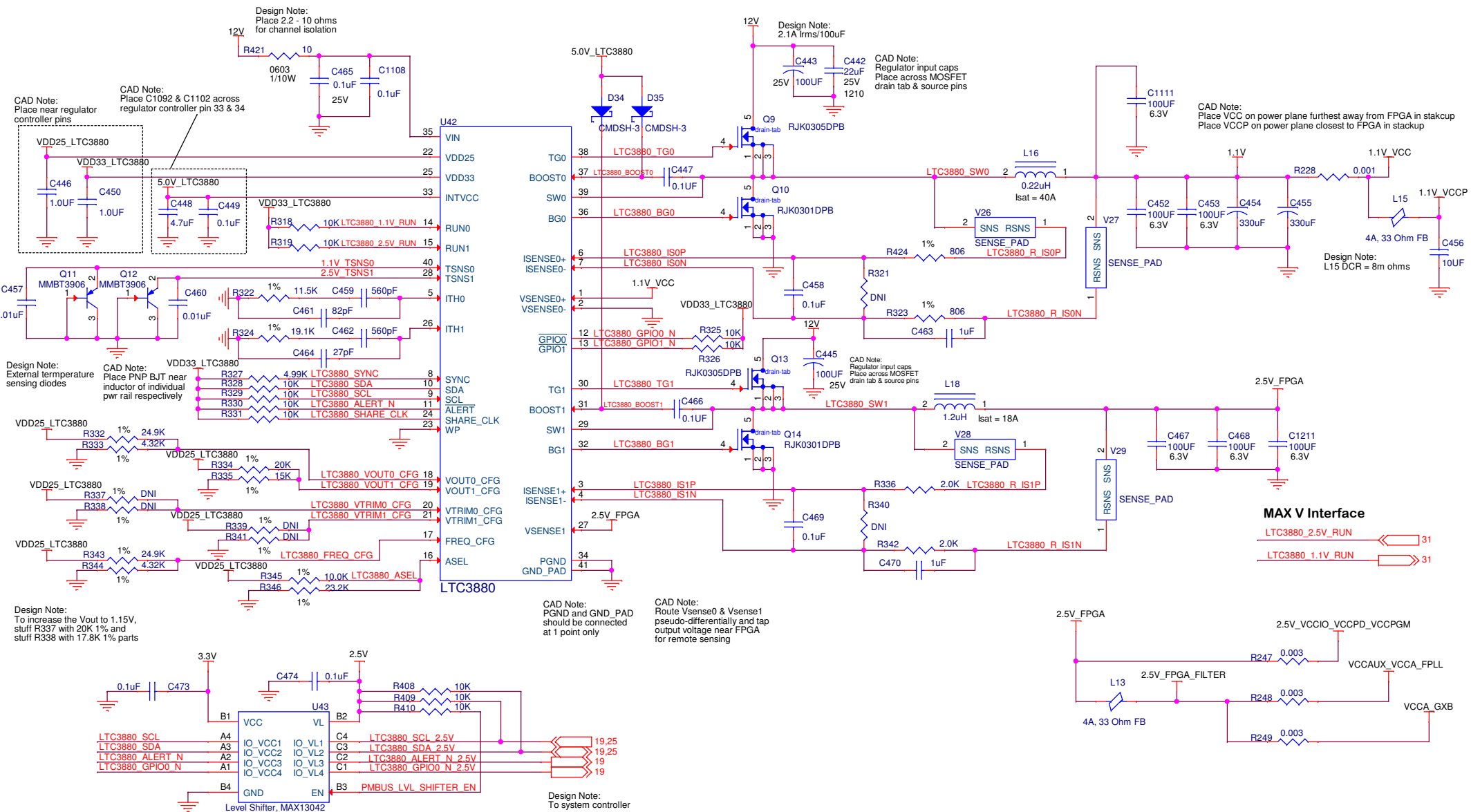
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| B | 150-0320806-C1 (6XX-44099R) |

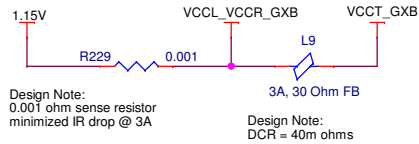
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|-------|----------------------------|-------|----|----|----|
| Date: | Friday, September 21, 2012 | Sheet | 26 | of | 35 |
|-------|----------------------------|-------|----|----|----|

| | | | | |
|----------------------------------|---------|----|---|----|
| Date: Friday, September 21, 2012 | Project | 20 | 9 | 50 |
| 2 | | 1 | | |

Power 2 - 1.1V & 2.5V FPGA

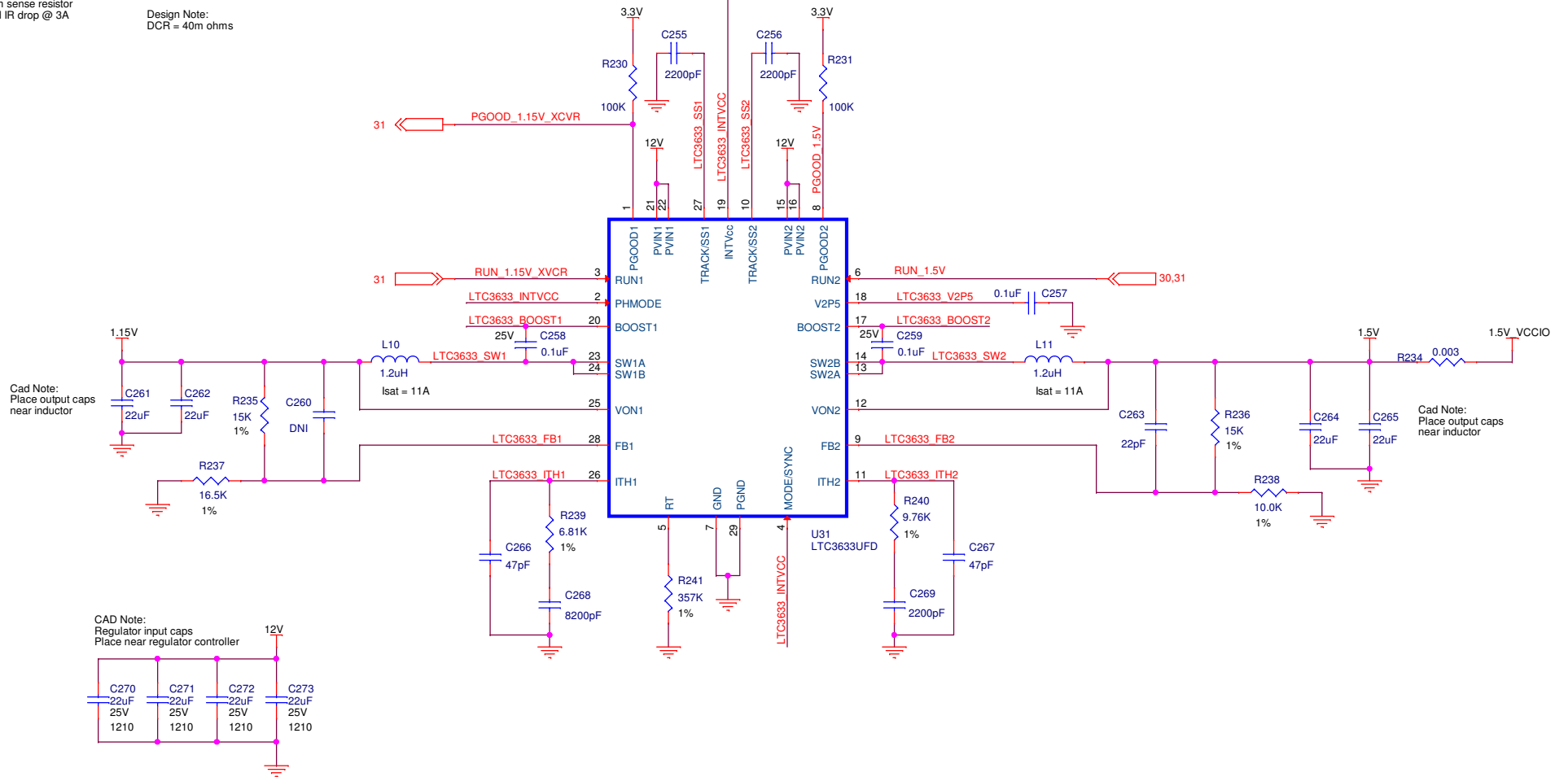


Power 3 - 1.15V & 1.5V FPGA



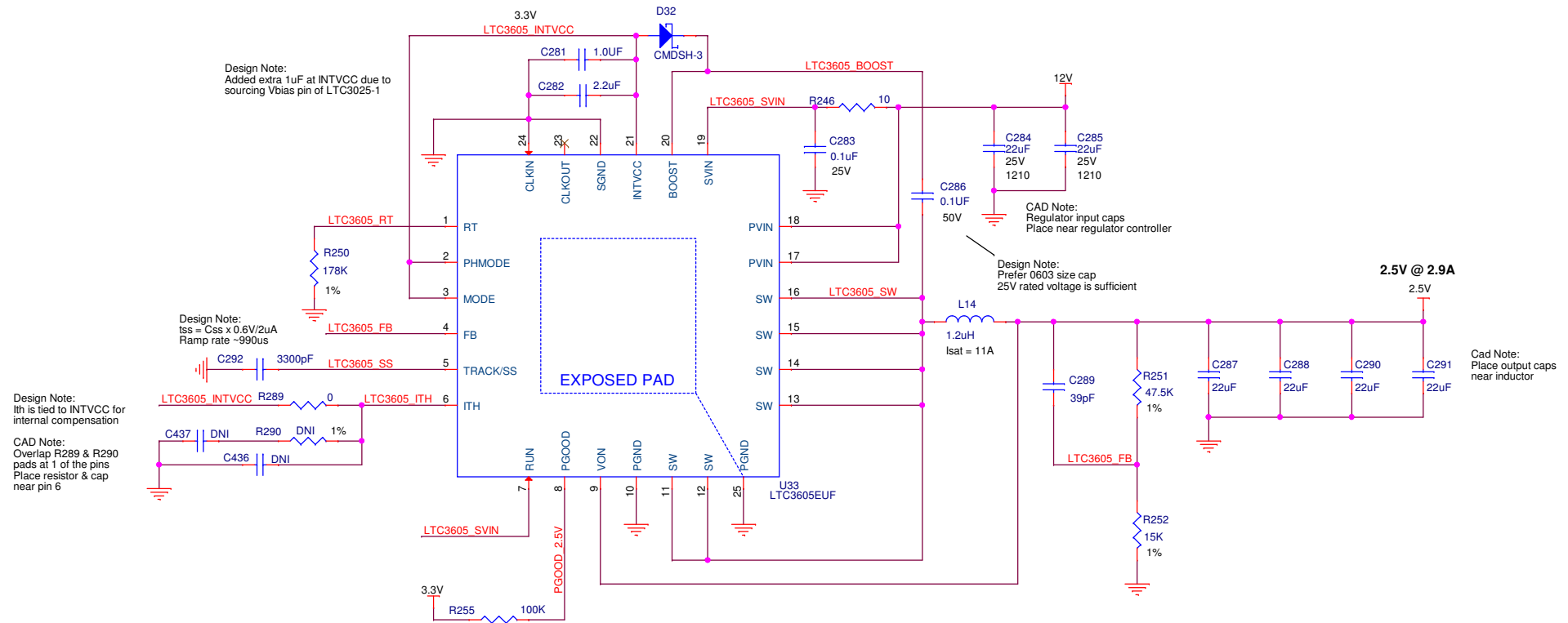
Design Note:
Soft-start, $t_{ss} = 430000 \text{ ohm} \times C_{ss}$
 $C_{ss} = 2.2\text{nF}$, ramp rate ~ 1ms

Cad Note:
Place near INTVCC pin



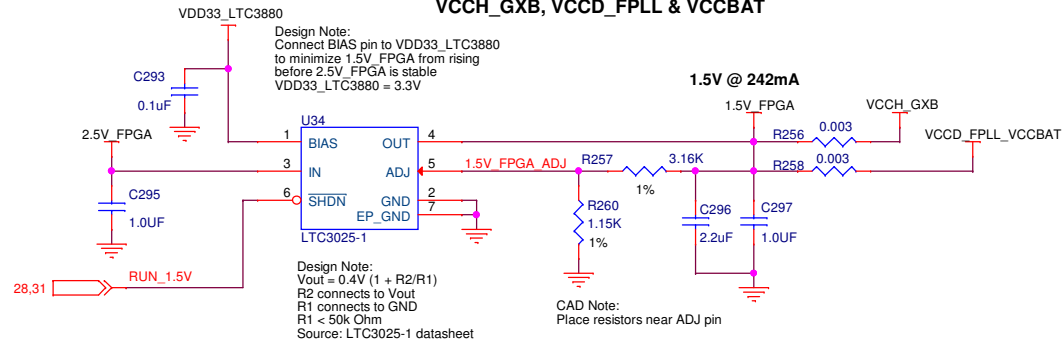
| | | |
|--|---|----------------|
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Power 3 - 2.5V Main

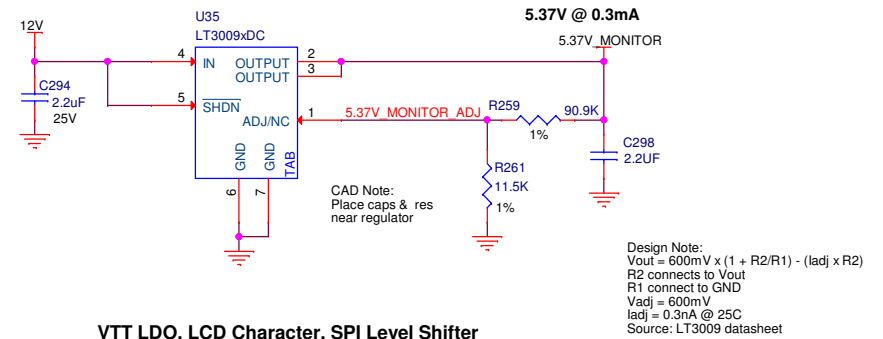


Power 4 - Linear Regulators

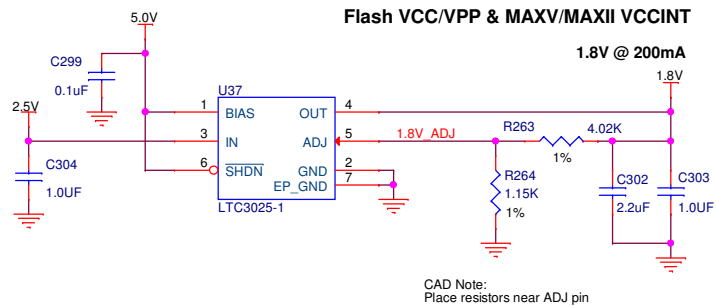
VCCH_GXB, VCCD_FPLL & VCCBAT



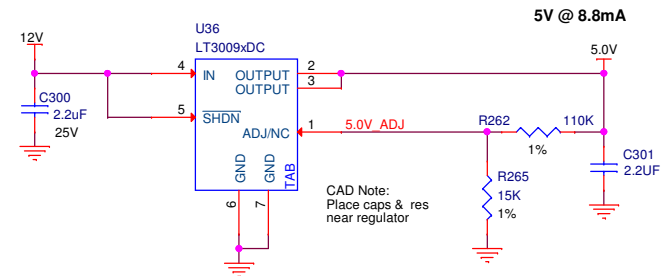
Power Monitor VIN



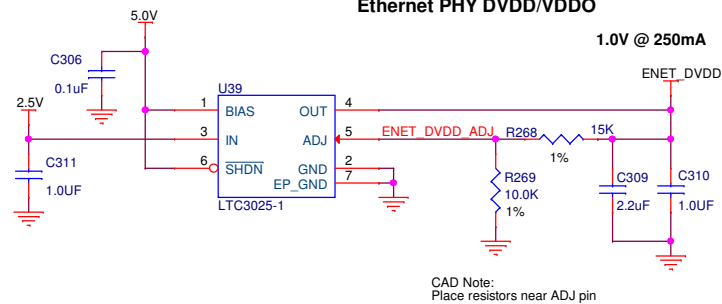
Flash VCC/VPP & MAXV/MAXII VCCINT



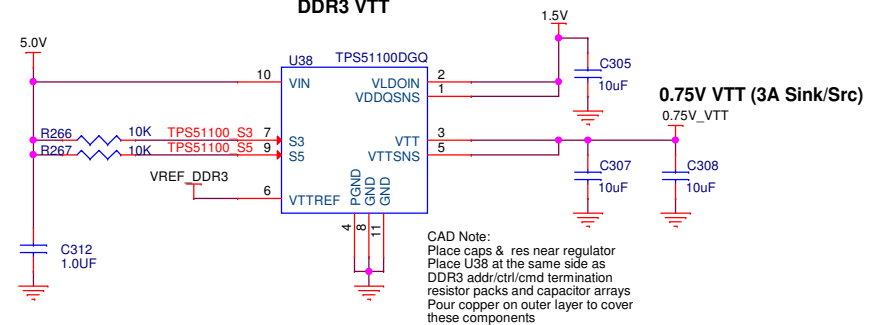
VTT LDO, LCD Character, SPI Level Shifter



Ethernet PHY DVDD/VDDO



DDR3 VTT



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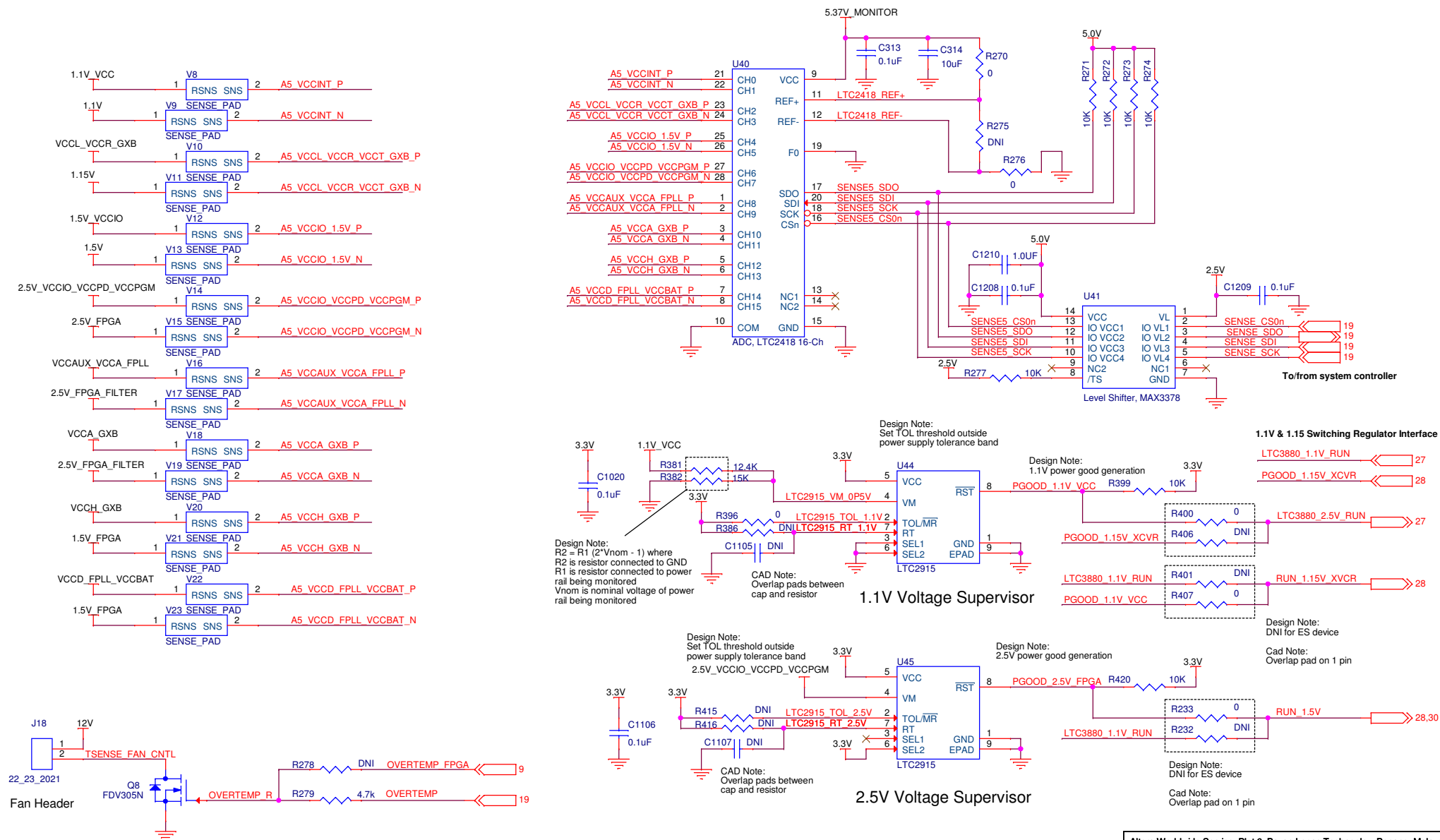
Title **Arria V GX Starter Kit Board**
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Size B Document Number 150-0320806-C1 (6XX-44099R)

Rev C1.1

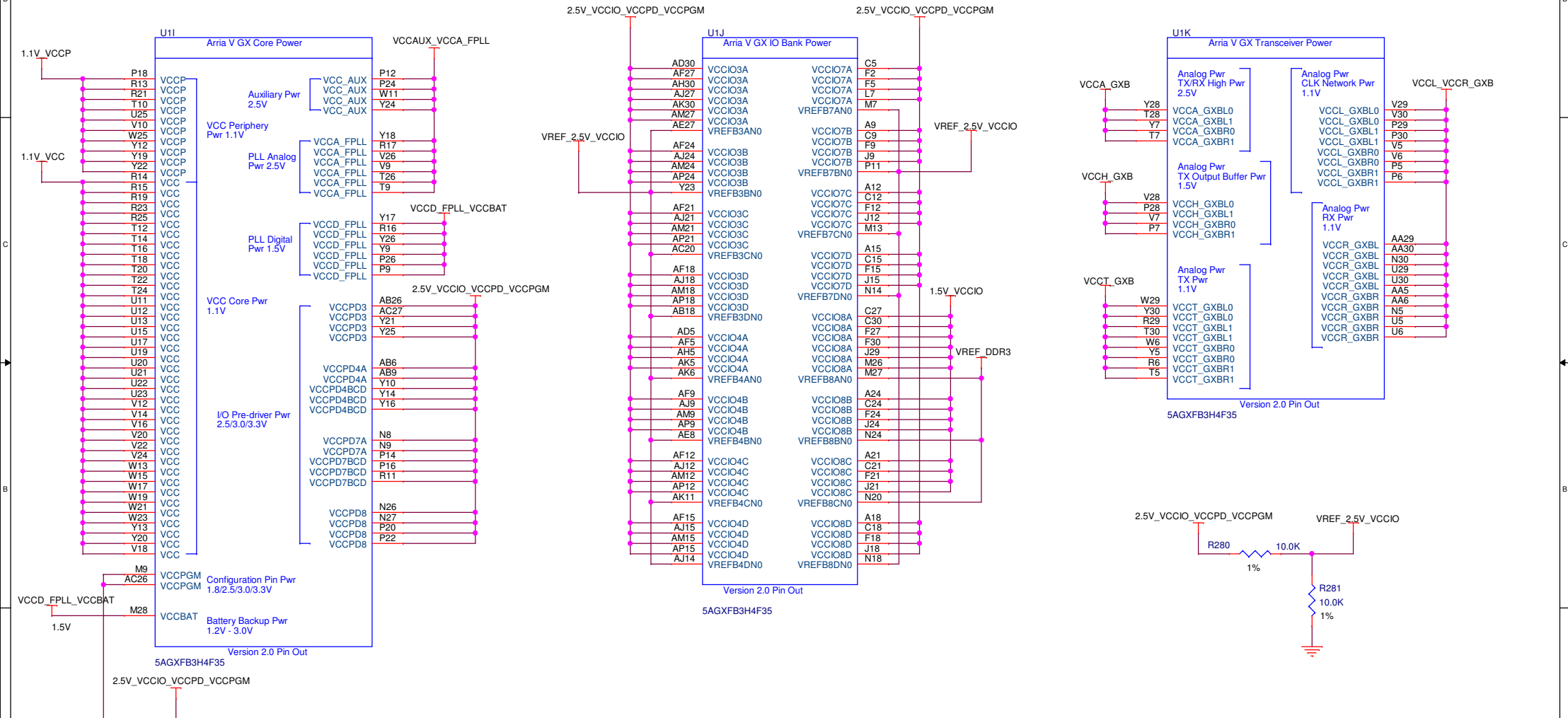
Date: Friday, September 21, 2012 Sheet 30 of 35

Power 5 - Power Monitor



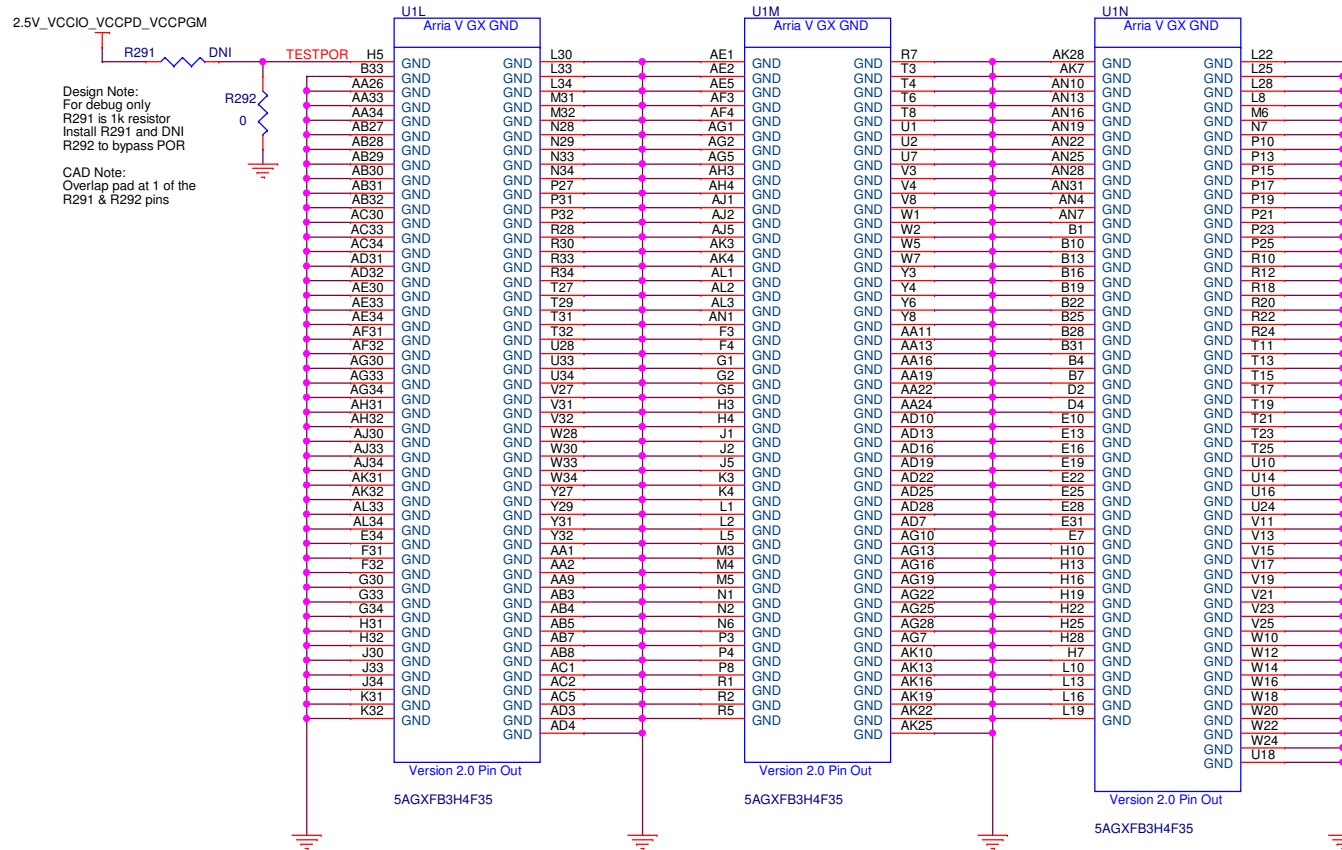
| | | |
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Power 6 - Arria V GX Power



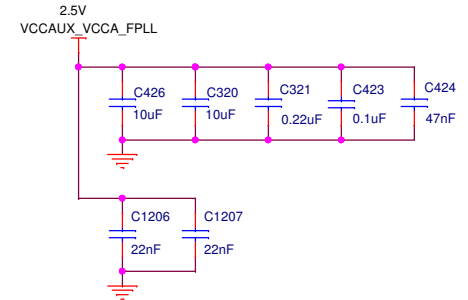
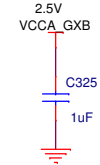
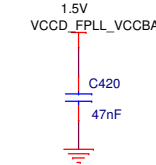
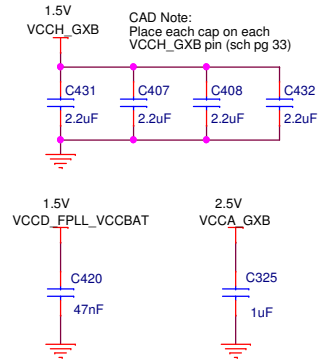
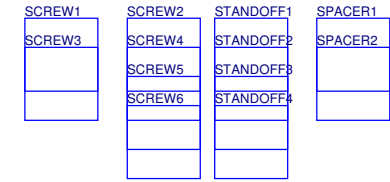
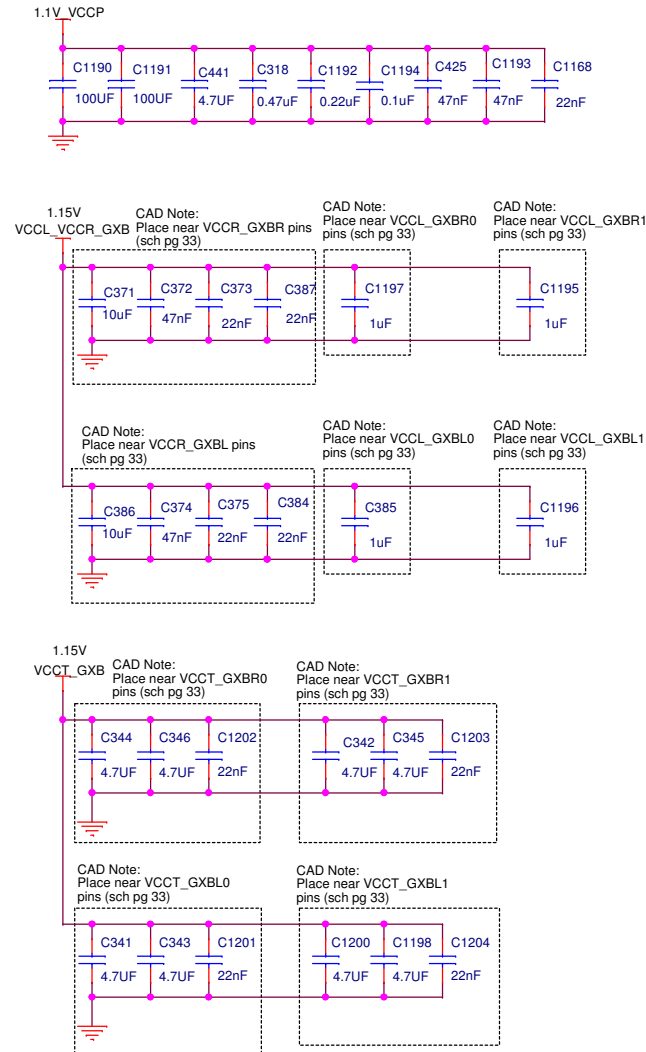
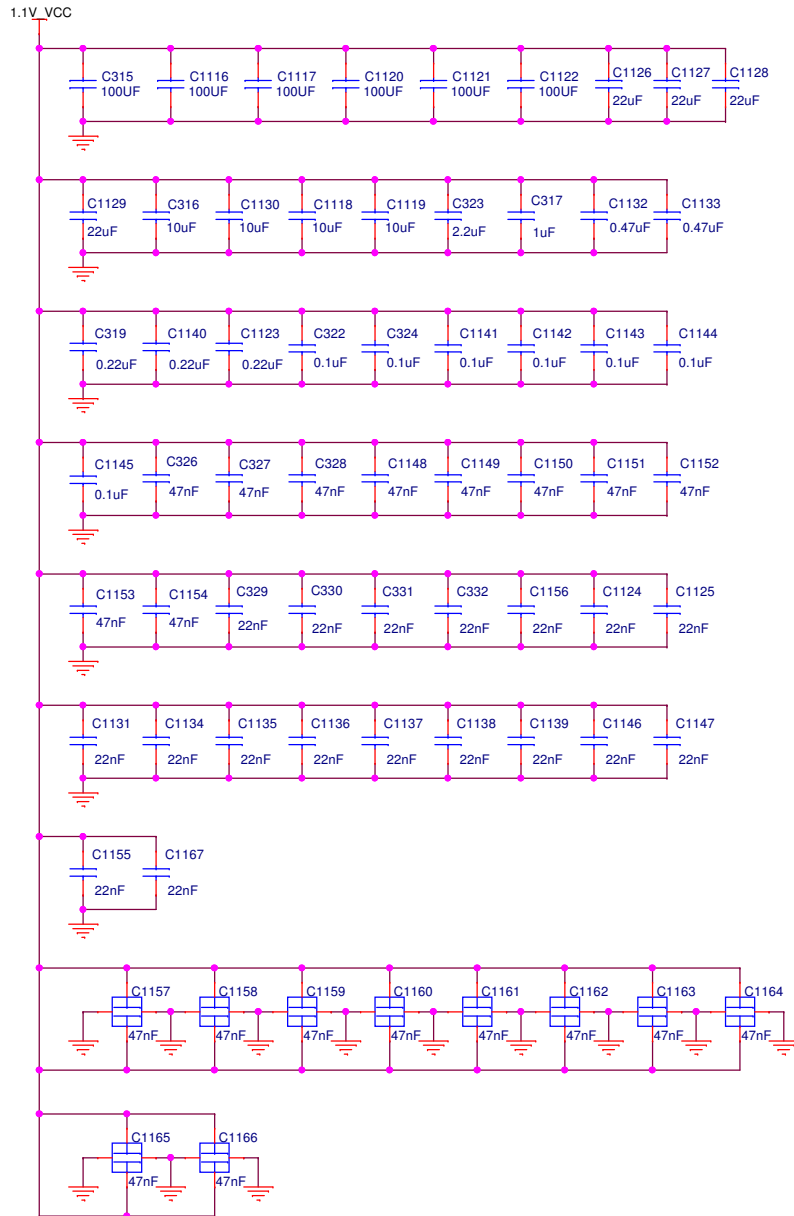
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| B | 150-0320806-C1 (6XX-44099R) | C1.1 | |
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Power 7 - Arria V GX Ground



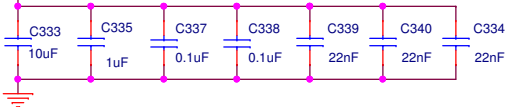
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|---|--|-------------|----------|
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Arria V GX Decoupling

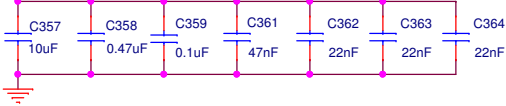


Arria V GX Decoupling

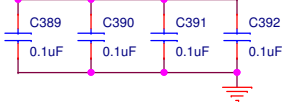
2.5V_VCCIO_VCCPD_VCCPGM



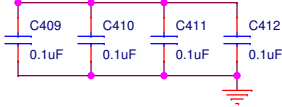
1.5V_VCCIO



VREF_2.5V_VCCIO



VREF_DDR3



| | | | |
|--|-----------------------------|--|----------|
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