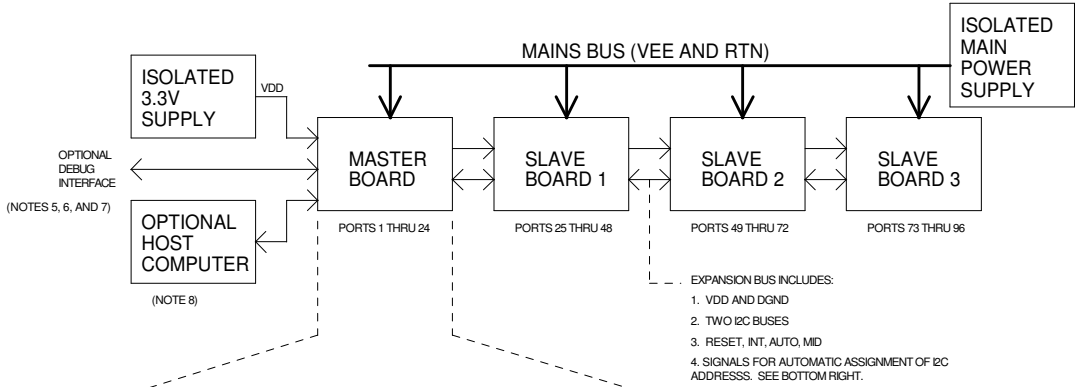


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**SYSTEM BLOCK DIAGRAM**

UP TO FOUR BOARDS CAN BE CONNECTED IN A CHAIN TO PROVIDE 96 PORTS.

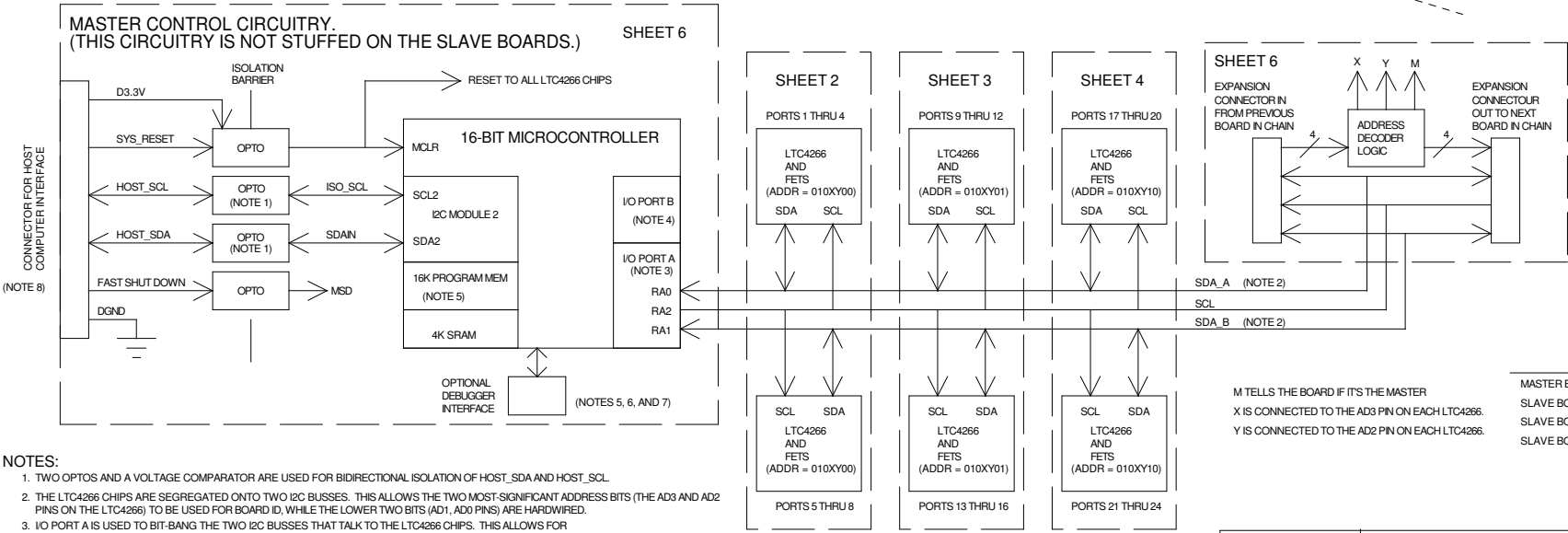
THE FIRST BOARD IN THE CHAIN MUST BE A MASTER (MICRO IS STUFFED). THE OTHER BOARDS CAN BE EITHER MASTERS OR SLAVES; IF THEY ARE MASTERS, THEIR MICROS WILL AUTOMATICALLY BE DISABLED AND THEY WILL BEHAVE AS SLAVES.

THE MAIN PS MUST BE CONNECTED TO EACH BOARD. THE VDD PS (3.3V NOM) MUST BE CONNECTED TO AT LEAST ONE BOARD IN THE CHAIN.

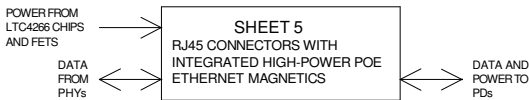
AN OPTIONAL HOST COMPUTER INTERFACE CAN BE USED TO:

1. SET THE SYSTEM POWER BUDGET
2. MONITOR STATUS
3. IMPLEMENT HIGH-LEVEL POWER MANAGEMENT FUNCTIONS SUCH AS PRIORITIZATION.

**BOARD BLOCK DIAGRAM**



- NOTES:**
1. TWO OPTOS AND A VOLTAGE COMPARATOR ARE USED FOR BIDIRECTIONAL ISOLATION OF HOST\_SDA AND HOST\_SCL.
  2. THE LTC4266 CHIPS ARE SEGREGATED ONTO TWO I2C BUSES. THIS ALLOWS THE TWO MOST-SIGNIFICANT ADDRESS BITS (THE AD3 AND AD2 PINS ON THE LTC4266) TO BE USED FOR BOARD ID, WHILE THE LOWER TWO BITS (AD1, AD0 PINS) ARE HARDWIRED.
  3. I/O PORT A IS USED TO BIT-BANG THE TWO I2C BUSES THAT TALK TO THE LTC4266 CHIPS. THIS ALLOWS FOR HIGH-SPEED OPERATION SINCE TWO CHIPS CAN BE READ SIMULTANEOUSLY.
  4. I/O PORT B IS USED FOR VARIOUS MISC STATUS AND CONTROL SIGNALS: MASTER, AUTO, MID, INT, AND MSD.
  5. THE FIRMWARE CAN BE REPROGRAMMED VIA THE HOST COMPUTER INTERFACE OR THE DEBUGGER INTERFACE.
  6. WHEN USING THE MPLAB ICD 2 FROM MICROCHIP INC., AN ISOLATED USB HUB IS RECOMMENDED.
  7. A UART INTERFACE IS ALSO PROVIDED FOR A TERMINAL PROGRAM TO SIMPLIFY DEBUGGING.
  8. THE HOST INTERFACE CONNECTOR IS COMPATIBLE WITH THE DC590B BOARD FROM LINEAR TECH.

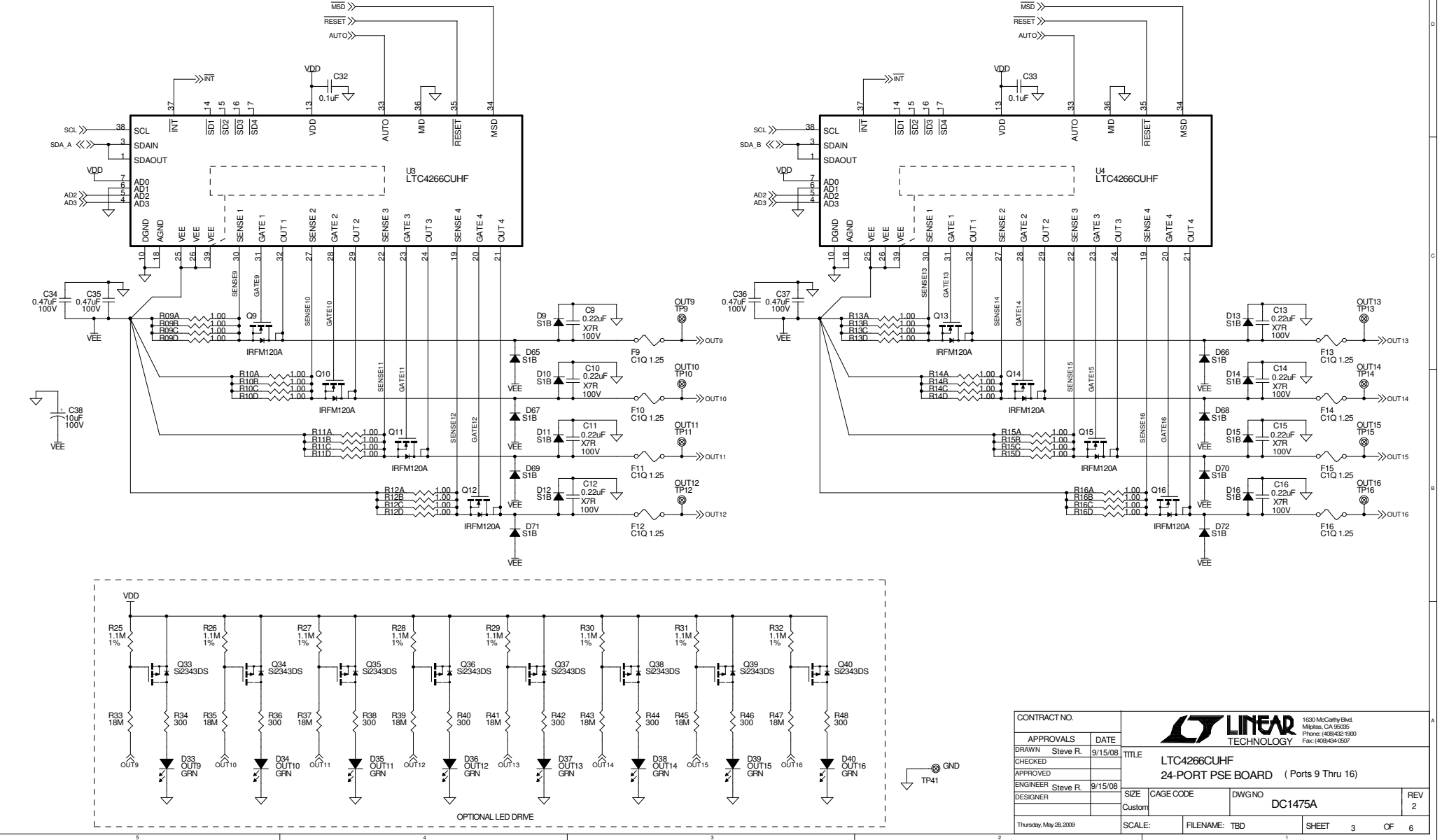



CONTRACT NO.		<b>LINEAR TECHNOLOGY</b> 1630 McCarthy Blvd Milpitas, CA 95035 Phone: (408)432-1900 Fax: (408)434-0907	
APPROVALS	DATE	TITLE	
DRAWN Steve R.	9/15/08	LTC4266CUHF 24-PORT PSE BOARD (Block diagram)	
CHECKED			
APPROVED			
ENGINEER Steve R.	9/15/08	SIZE Custom	CAGE CODE
DESIGNER		DWG NO DC1475A	REV 2
Thursday, May 28, 2009		SCALE:	FILENAME: TBD
		SHEET 1	OF 6



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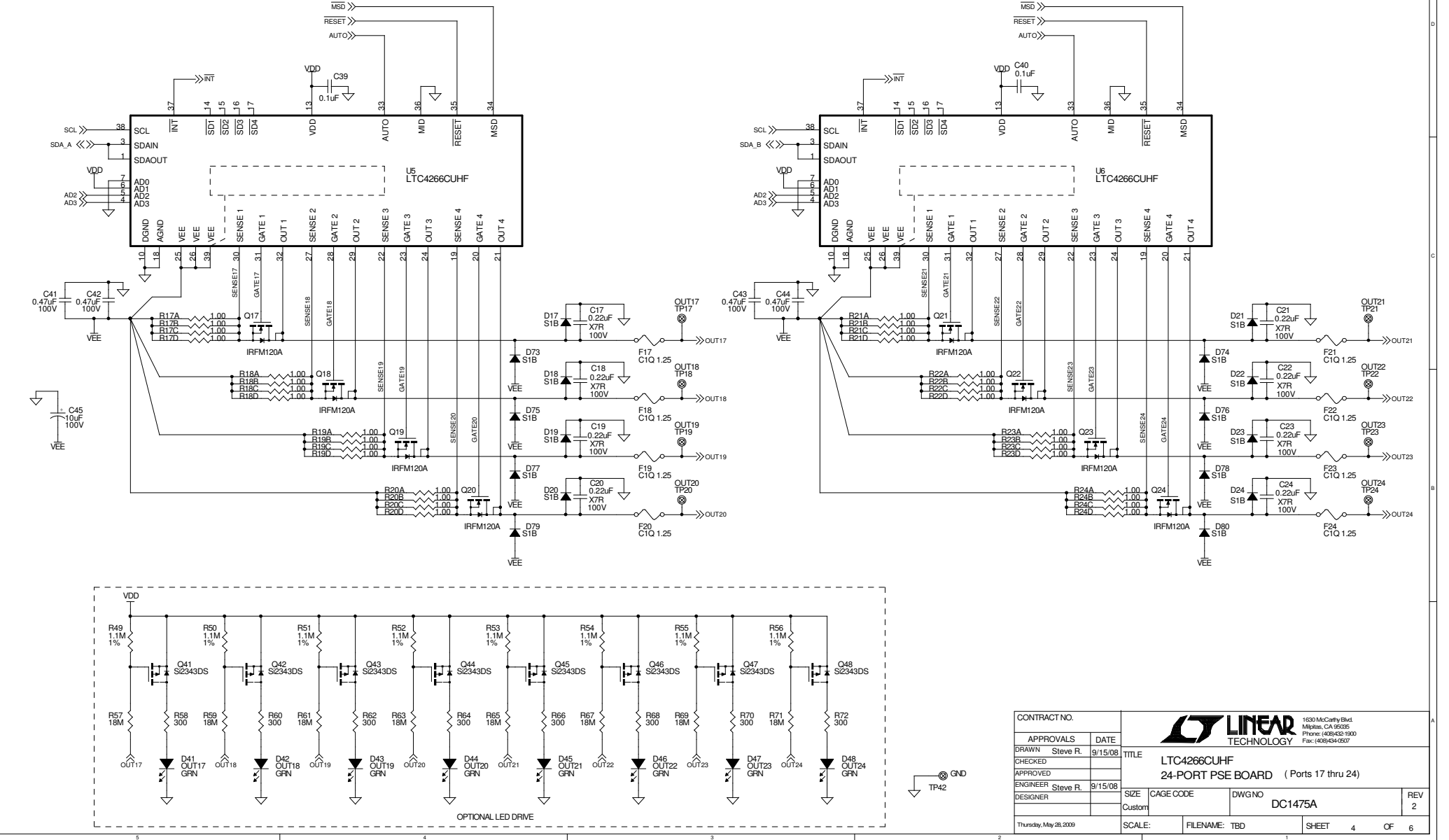
REVISION HISTORY			
ECO	REV	DESCRIPTION	DATE




CONTRACT NO.		 <div>1630 McCarthy Blvd. Milpitas, CA 95035 Phone: (408)432-1900 Fax: (408)434-0507</div>	
APPROVALS	DATE		
DRAWN Steve R.	9/15/08	TITLE	
CHECKED		LTC4266CUHF	
APPROVED		24-PORT PSE BOARD (Ports 9 Thru 16)	
ENGINEER Steve R.	9/15/08	SIZE	CAGE CODE
DESIGNER		Custom	DWG NO
Thursday, May 28, 2009		SCALE:	FILENAME: TBD
		SHEET	3 OF 6

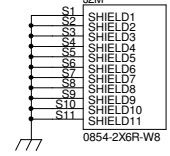
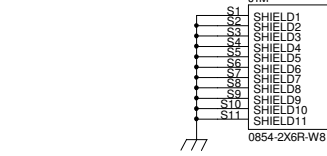
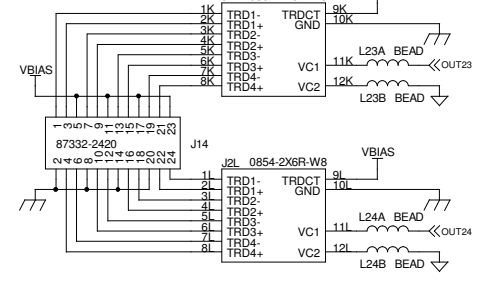
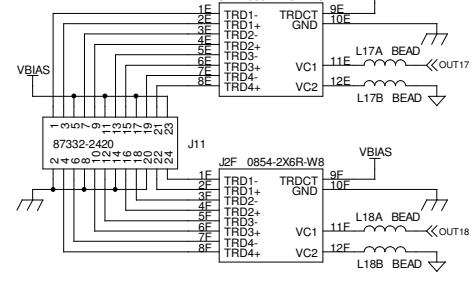
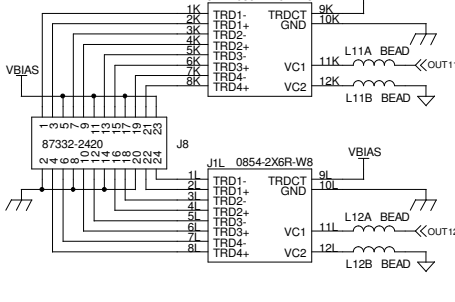
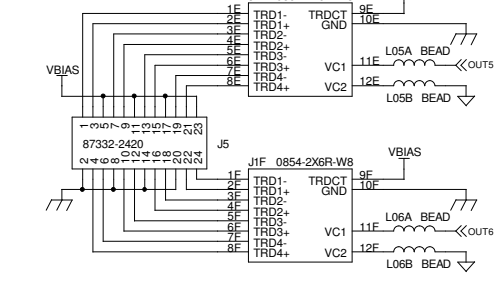
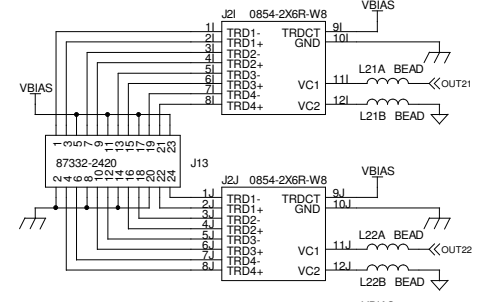
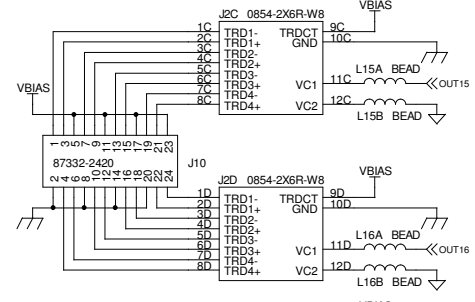
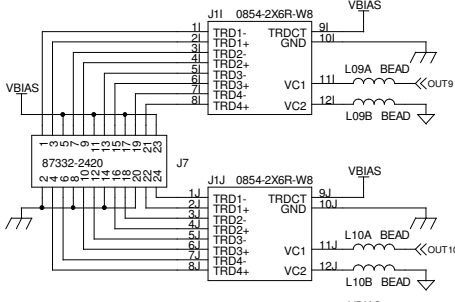
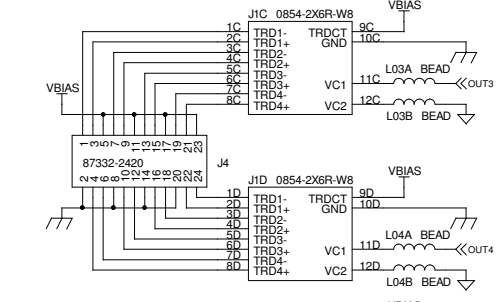
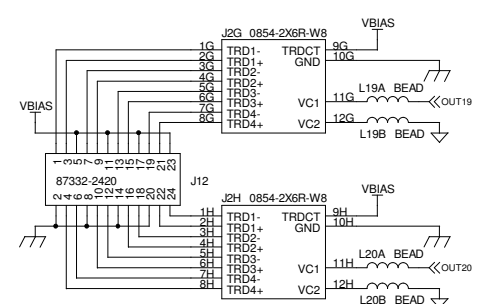
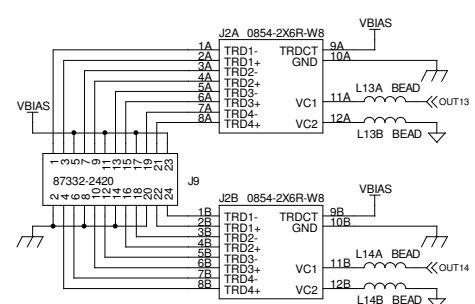
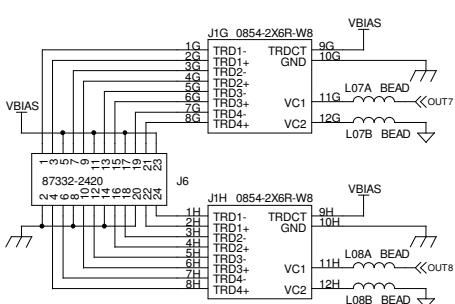
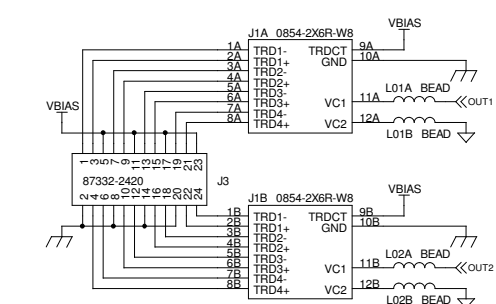
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REVISION HISTORY			
ECO	REV	DESCRIPTION	DATE



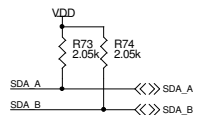
CONTRACT NO.		 <div>1630 McCarthy Blvd. Milpitas, CA 95035 Phone: (408) 432-1900 Fax: (408) 434-0507</div>	
APPROVALS	DATE		
DRAWN Steve R.	9/15/08	TITLE LTC4266CUHF 24-PORT PSE BOARD (Ports 17 thru 24)	
CHECKED			
APPROVED			
ENGINEER Steve R.	9/15/08		
DESIGNER		SIZE Custom	CAGE CODE
Thursday, May 28, 2009		SCALE:	FILENAME: TBD
		SHEET 4	OF 6

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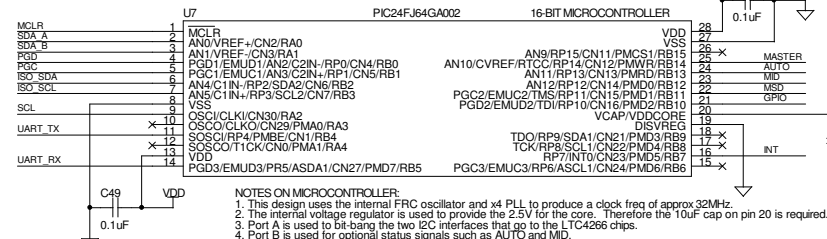
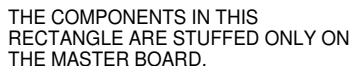
CONTRACT NO.		 1630 McCarthy Blvd. Milpitas, CA 95035 Phone: (408)432-1900 Fax: (408)434-0507	
APPROVALS	DATE		
DRAWN Steve R.	9/15/08	TITLE	
CHECKED		LTC4266CUHF	
APPROVED		24-PORT PSE BOARD ( Ethernet connectors )	
ENGINEER Steve R.	9/15/08	SIZE	
DESIGNER		Custom	
Thursday, May 28, 2009		DWG NO	
		DC1475A	
		REV	
		2	
		SCALE:	
		FILENAME: TBD	
		SHEET	
		5 OF 6	

CIRCUITRY ON THE LEFT SIDE OF THIS LINE IS NOT ESSENTIAL (EXCEPT WHERE NOTED); THESE COMPONENTS CAN BE DELETED IN MOST APPLICATIONS.



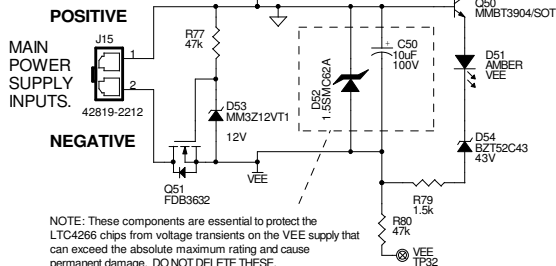
No pull up is needed for SCL since the PIC will drive it high as well as low. The LTC4266 chips don't use clock stretching, so SCL goes in one direction only.

REVISION HISTORY				
ECO	REV	DESCRIPTION	DATE	APPROVED



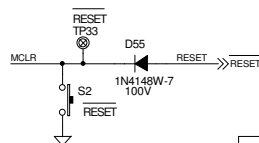
NOTES ON MICROCONTROL LIFE

1. This design uses the internal FRC oscillator and x4 PLL to produce a clock freq of approx 32MHz.
2. The internal voltage regulator is used to provide the 2.5V for the core. Therefore the 10uF cap on pin 20 is required
3. Port A is used to bit-bang the two I2C interfaces that go to the LTC4266 chips.
4. Port B is used for optional status signals such as ALTO and MID.



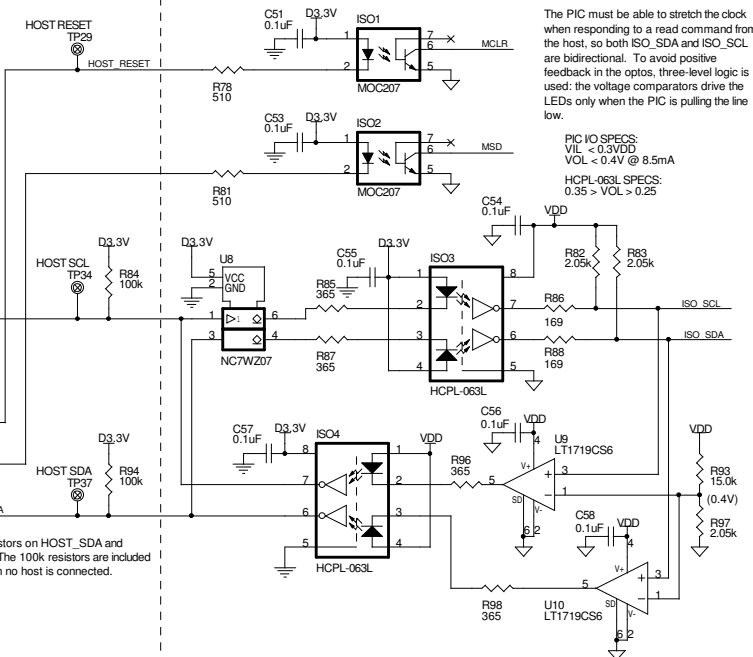
OPTIONAL  
INTERFACE FOR  
IN-CIRCUIT  
EMULATOR/  
DEBUGGER.

The +3.3V supply for this side of the isolation barrier can be supplied via this connector or through the D3.3V and DGND test points.



OPTIONAL INTERFACE TO  
HOST COMPUTER.

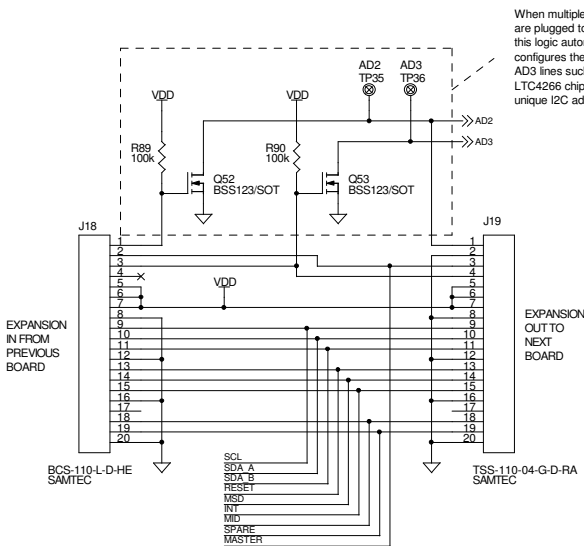
The user should provide pull-up resistors on HOST\_SDA and HOST\_SCL external to this board. The 100k resistors are included here so these inputs don't float when no host is connected.



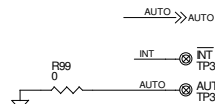
The PIC must be able to stretch the clock when responding to a read command from the host, so both `ISO_SDA` and `ISO_SCL` are bidirectional. To avoid positive feedback in the optos, three-level logic is used: the voltage comparators drive the LEDs only when the PIC is pulling the line low.


PIC I/O SPECS:  
VIL < 0.3VDD  
VOL < 0.4V @ 8.5mA

HCPL-063L SPECS:  
0.35 > VOL > 0.25



MASTER is high only on the first board in the chain. The other boards likely won't have the micro stuffed, but if they do, the MASTER signal mutes them so only one micro is the master.



CONTRACT NO.			1920 McCarthy Blvd. Milpitas, CA 95035 Phone: (408) 438-1930 Fax: (408) 434-0207			
APPROVALS	DATE		TITLE LTC4266CUHF 24-PORT PSE BOARD (Microcontroller)			
DRAWN Steve R.	9/15/08					
CHECKED						
APPROVED						
ENGINEER Steve R.	9/15/08					
DESIGNER		SIZE Custom	CAGE CODE	DWG NO DC1475A	REV 2	
Thursday, May 28, 2009		SCALE:	FILENAME: TBD		SHEET 6	OF 6