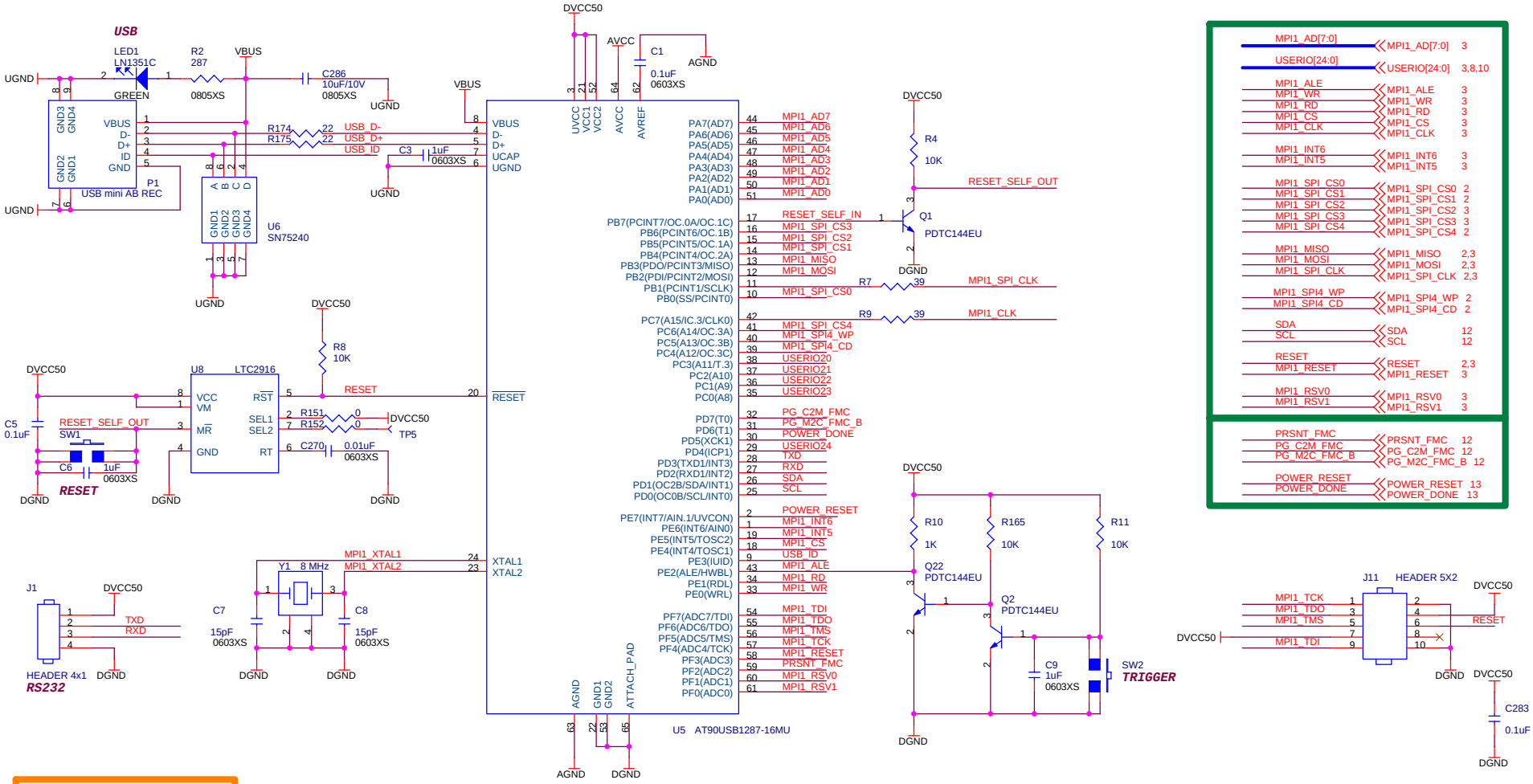

NOTES: UNLESS OTHERWISE SPECIFIED

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CONTRACT NO.

APPROVALS

PCB DES. KIM T.

ENG. GARY YU

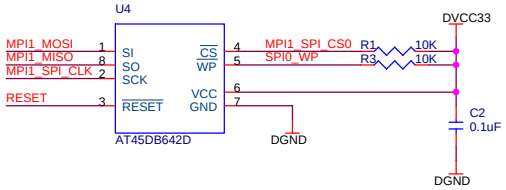
LINEAR TECHNOLOGY
1630 McCarthy Blvd.
Milpitas, CA 95035
Phone: (408)432-1900
Fax: (408)434-0507
LTC Confidential-For Customer Use Only

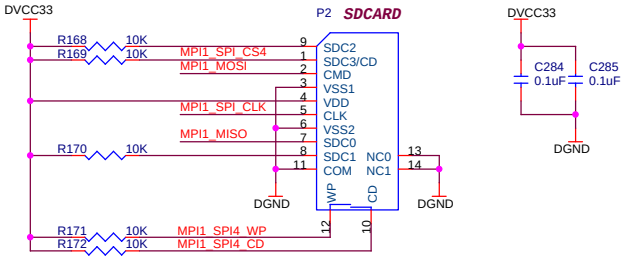
TITLE: SCHEMATIC

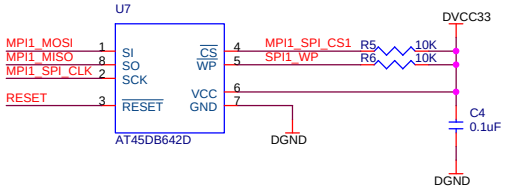
PSTACHE

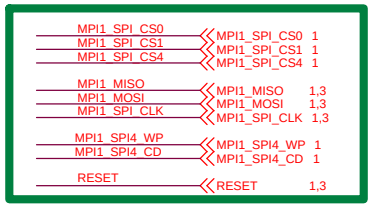
SIZE B | IC NO. DC1371A - HSDAACS | REV 2

DATE: Tuesday, November 24, 2009 | SHEET 1 OF 16









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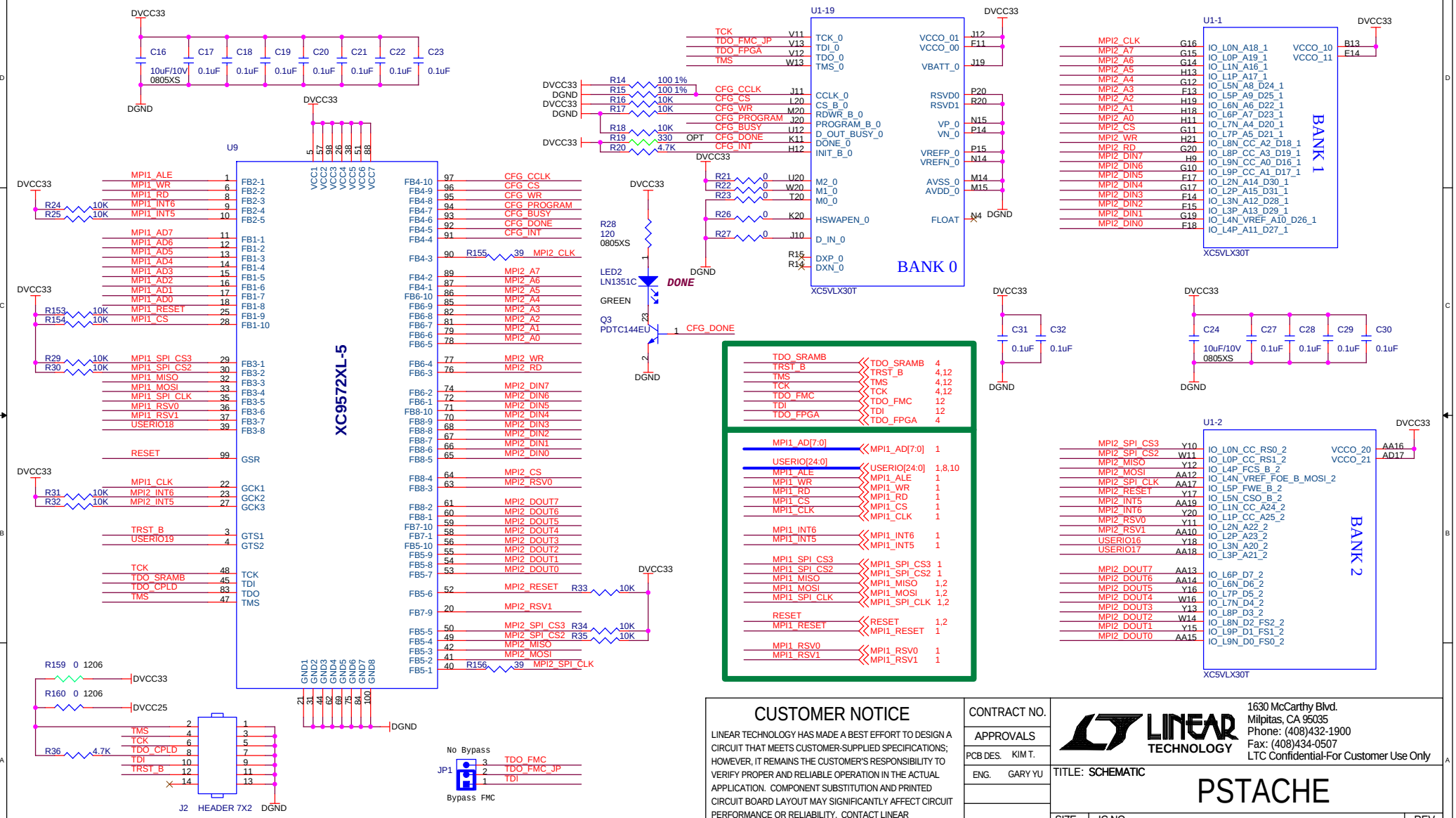
SIZE	IC NO.	REV
B	DC1371A - HSDAACS	2

DATE: Tuesday, November 24, 2009



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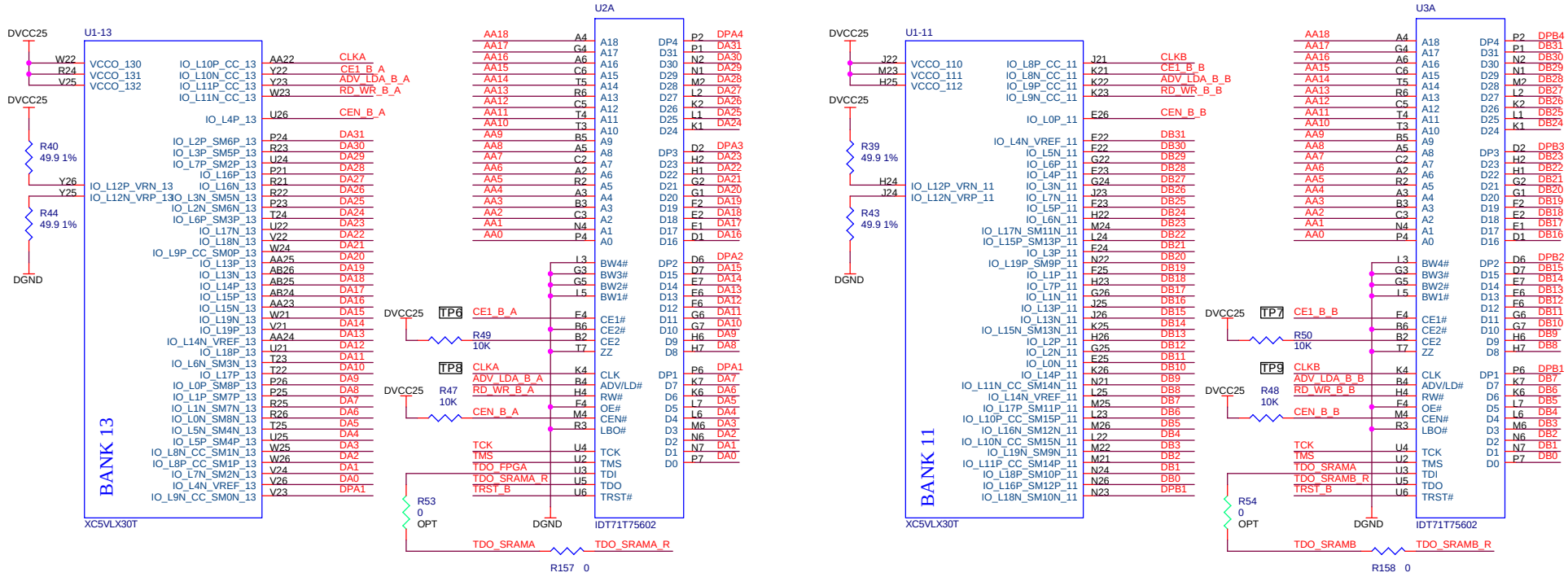

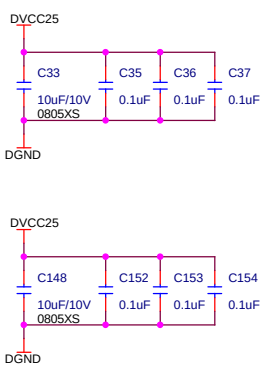

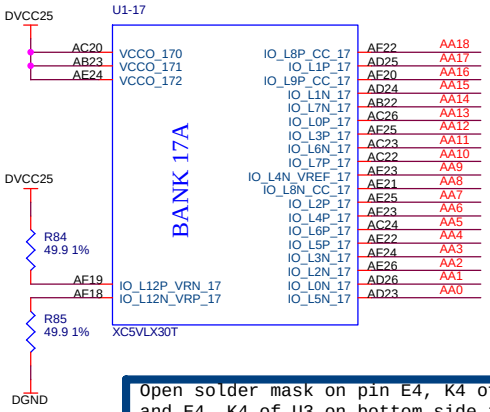

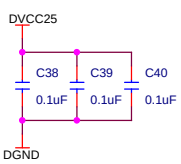

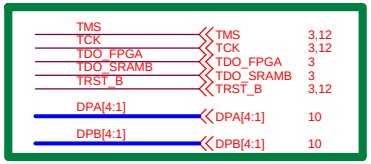

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Open solder mask on pin E4, K4 of U2 and E4, K4 of U3 on bottom side to make test points

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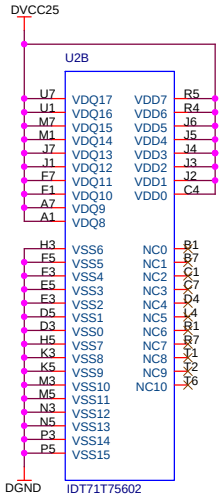

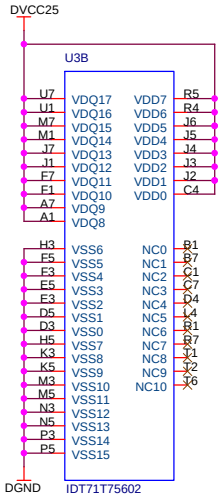

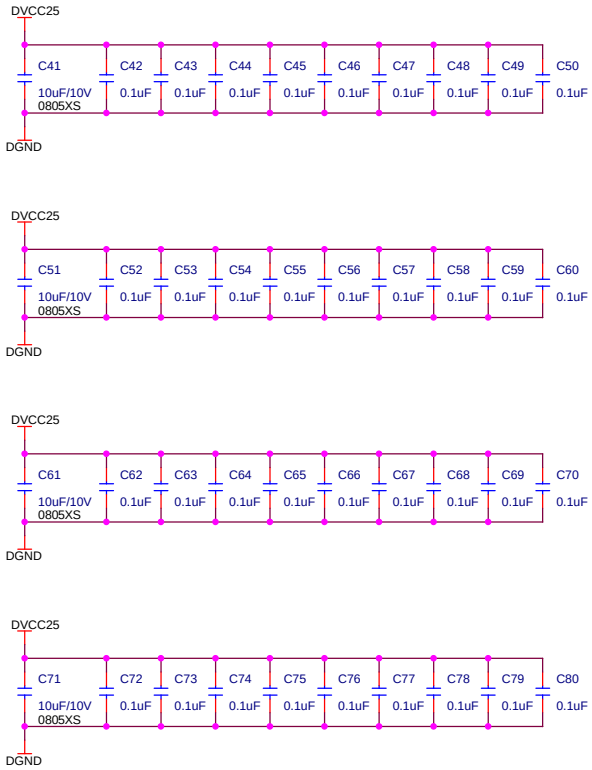

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SIZE	IC NO.	REV
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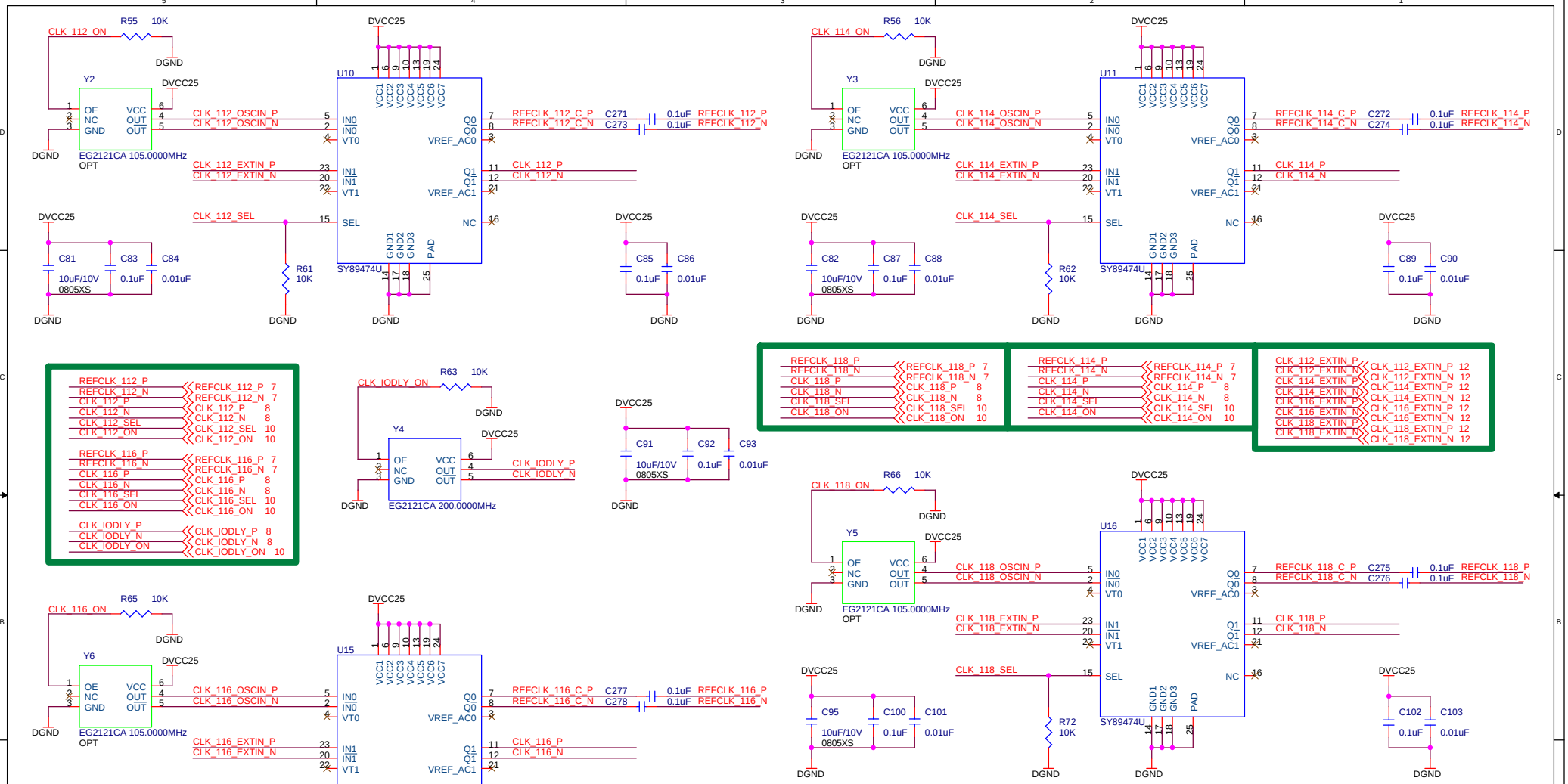
DATE: Tuesday, November 24, 2009

SHEET 5 OF 16



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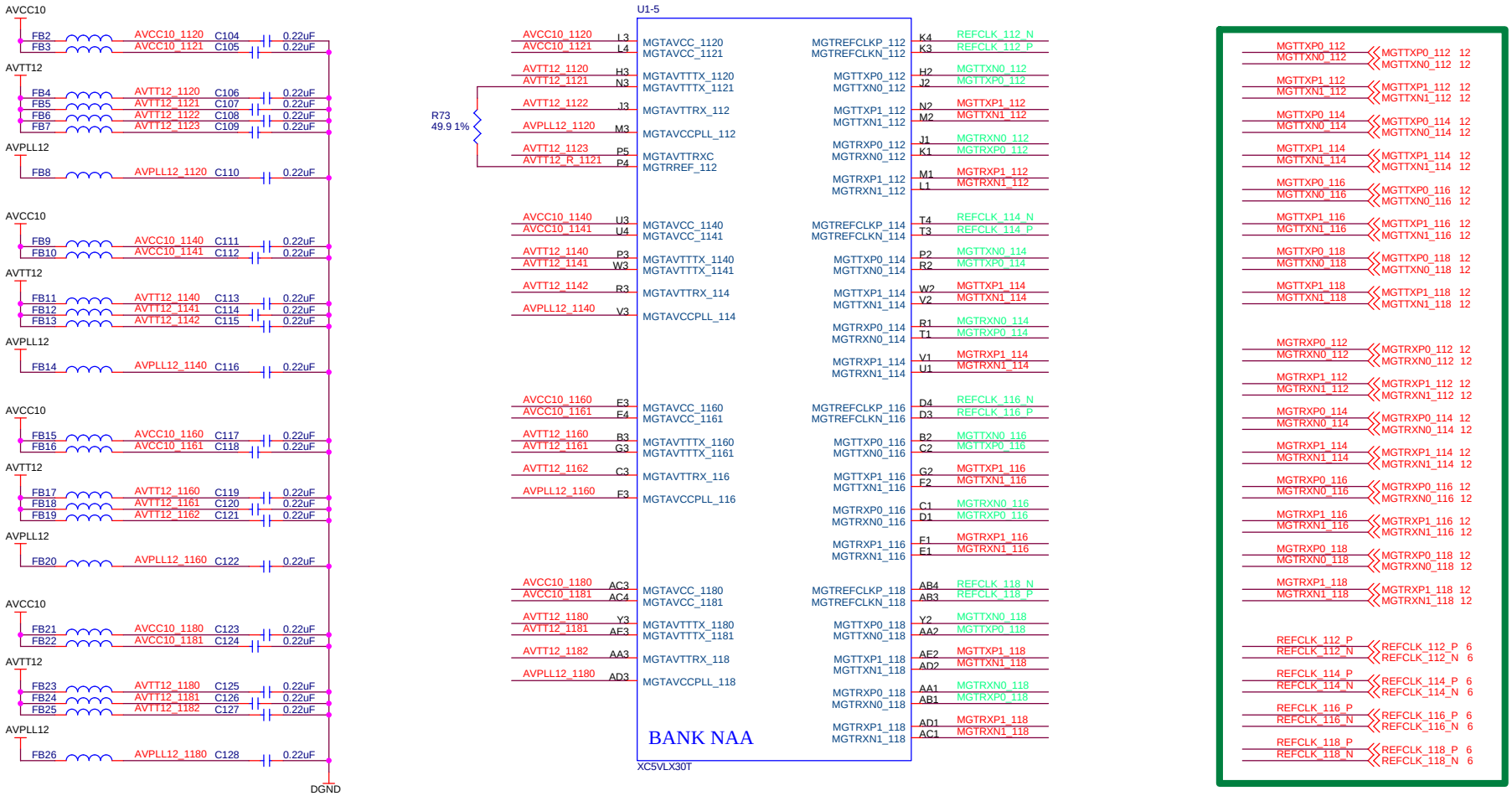
SIZE B | IC NO. DC1371A - HSDAACS | REV 2

DATE: Tuesday, November 24, 2009 | SHEET 6 OF 16



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3. ALL FERRITE BEADS ARE MPZ1608S221A

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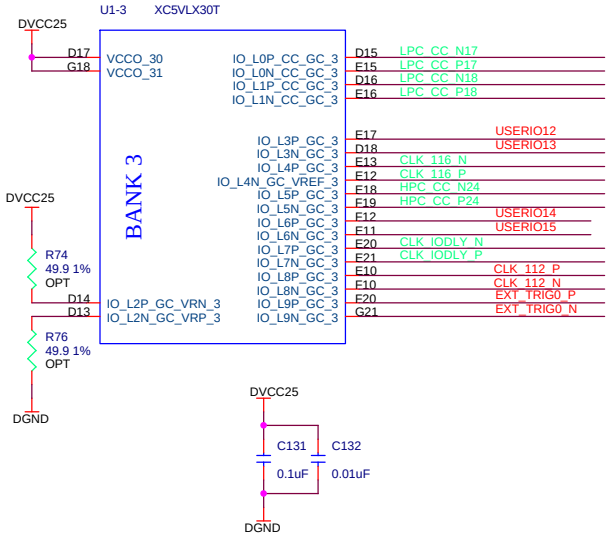

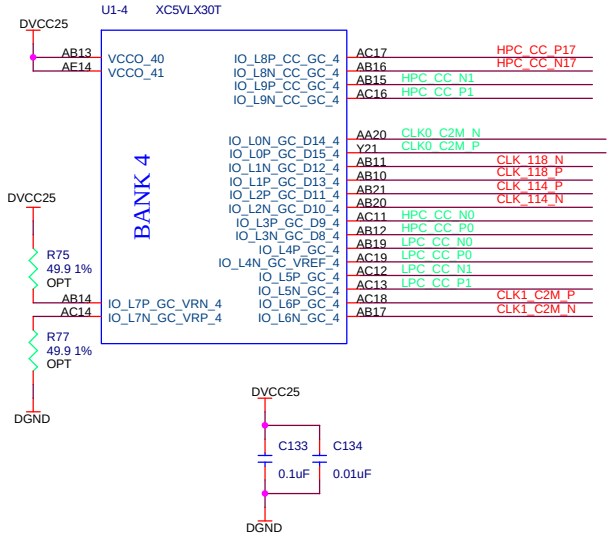

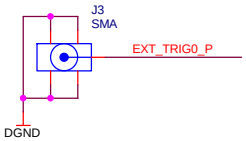

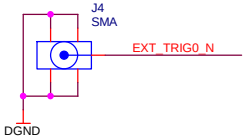

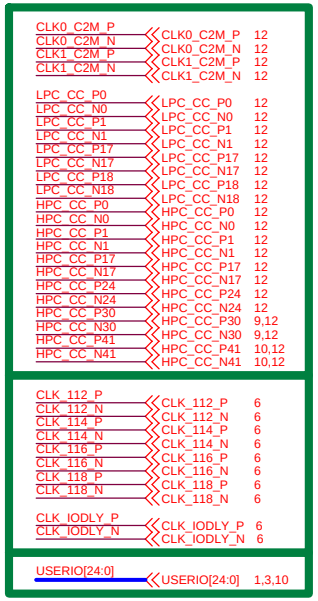

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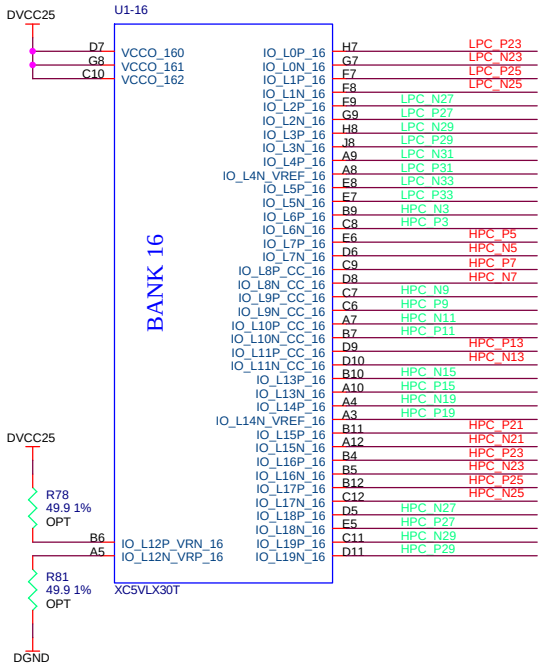

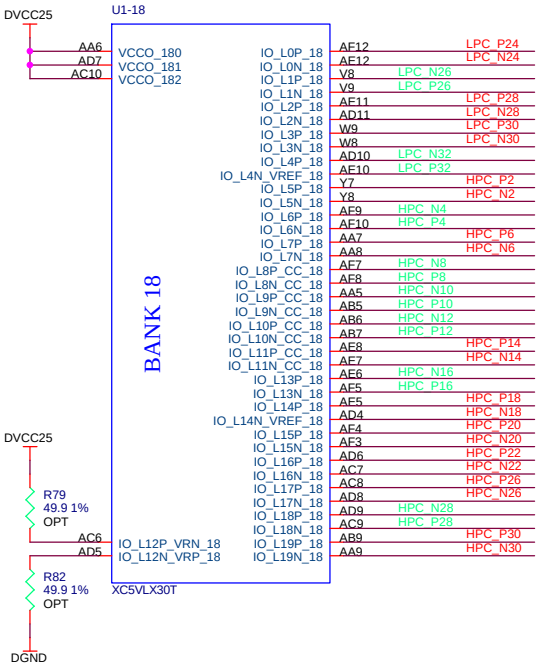

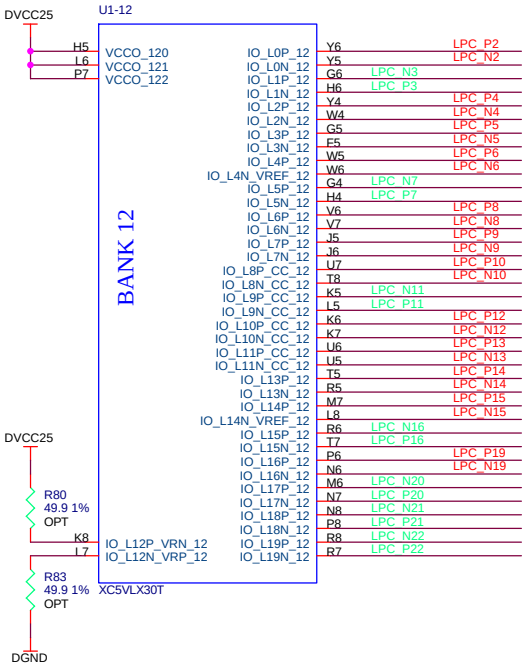

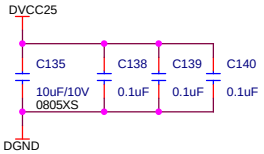

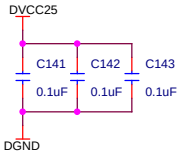

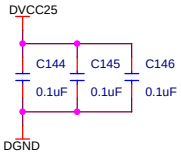

LPC_P[33:0]	LPC_P[33:0]	8,12
LPC_N[33:0]	LPC_N[33:0]	8,12
HPC_P[45:0]	HPC_P[45:0]	8,10,12
HPC_N[45:0]	HPC_N[45:0]	8,10,12

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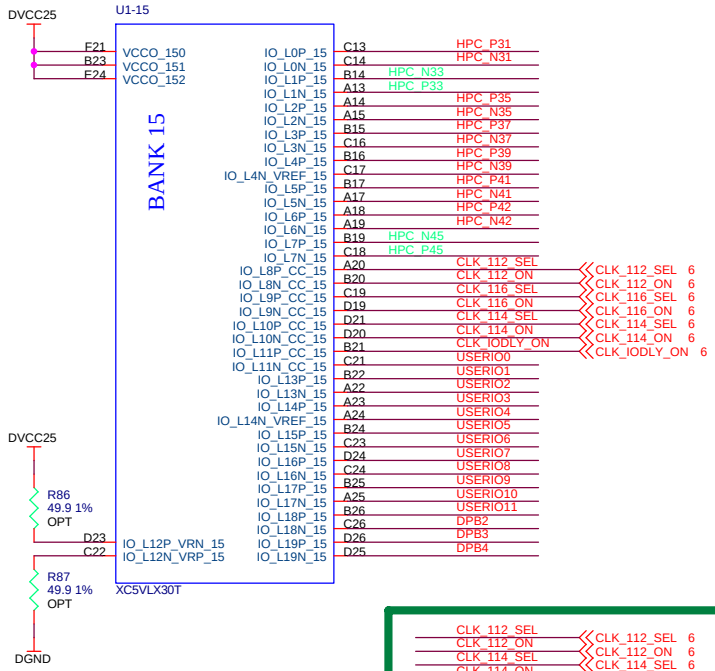
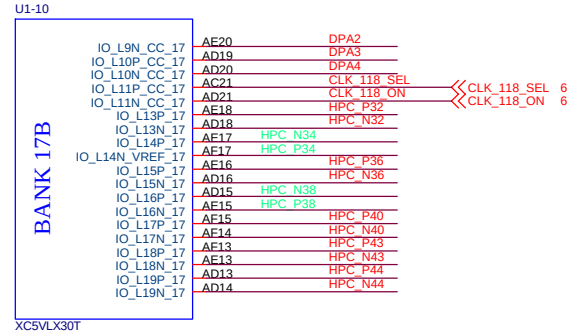
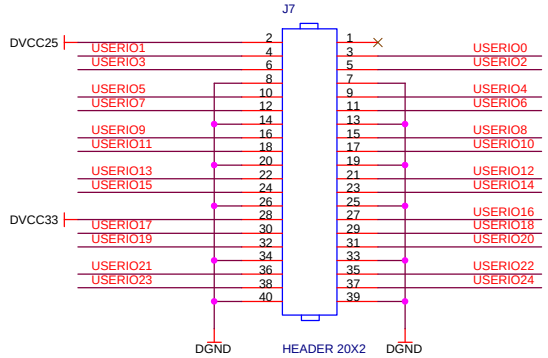
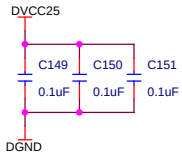
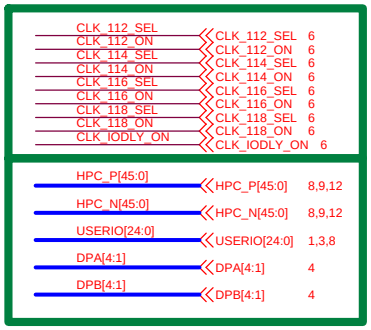
SHEET 9 OF 16











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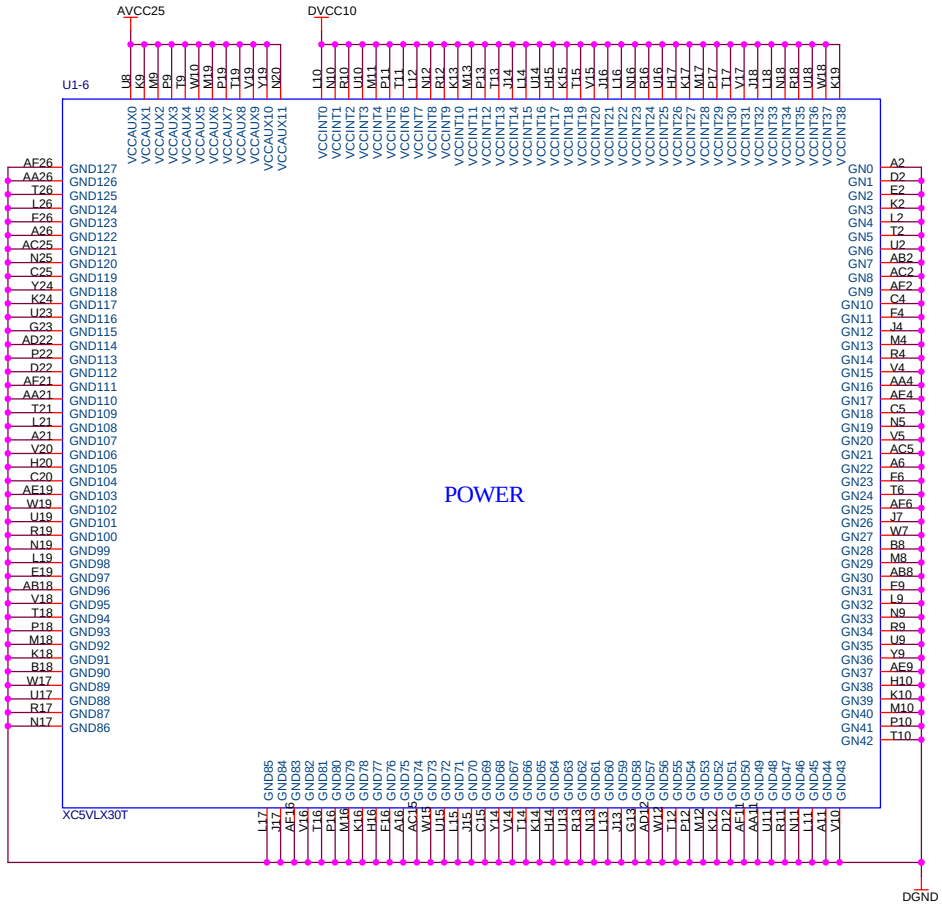
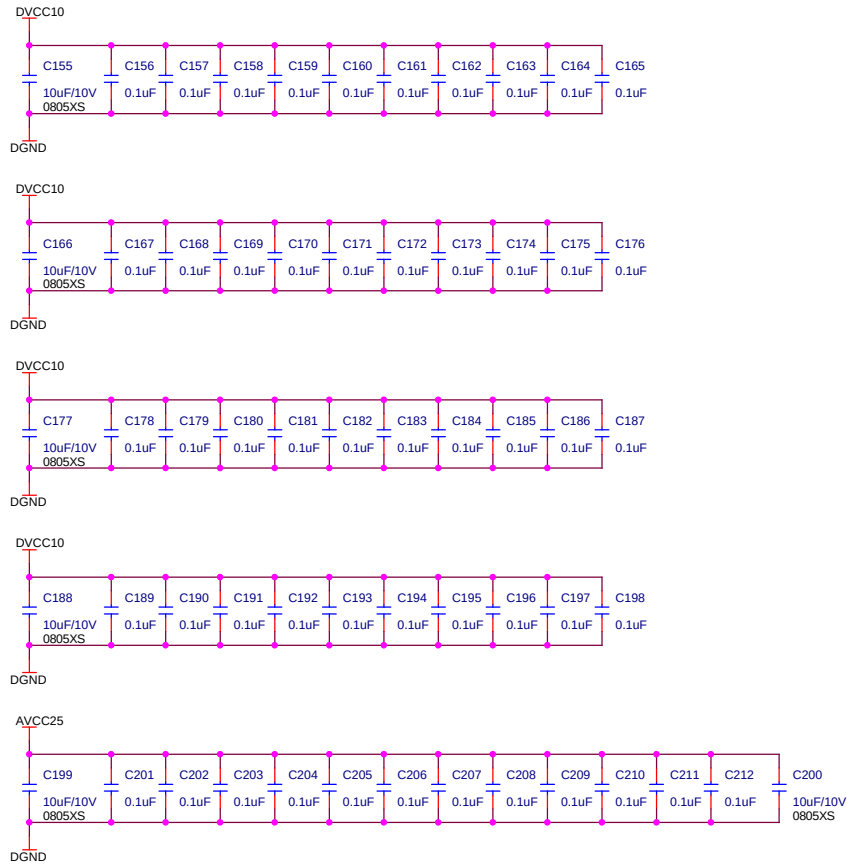
TITLE: SCHEMATIC

PSTACHE

SIZE B | IC NO. DC1371A - HSDAACS | REV 2

DATE: Tuesday, November 24, 2009





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CONTRACT NO.

APPROVALS

PCB DES. KIM T.

ENG. GARY YU

LINEAR TECHNOLOGY
1630 McCarthy Blvd.
Milpitas, CA 95035
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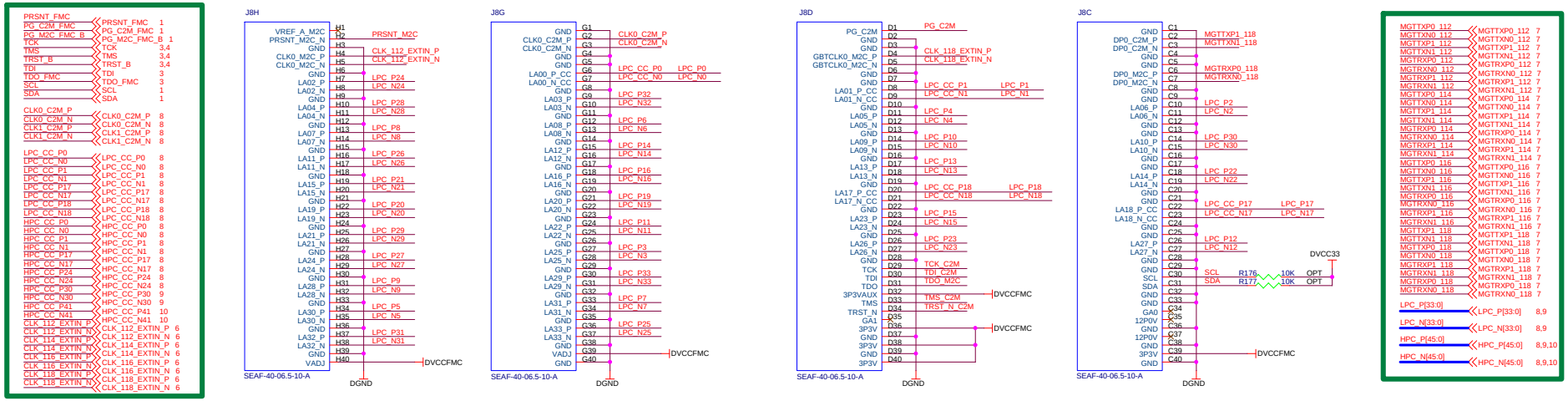
DATE: Tuesday, November 24, 2009

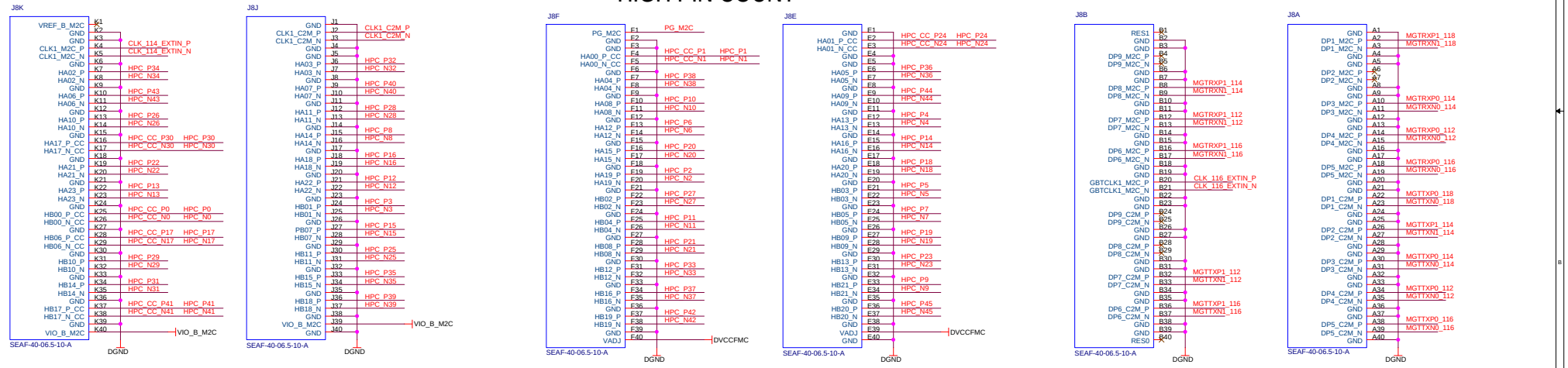
NOTES: UNLESS OTHERWISE SPECIFIED

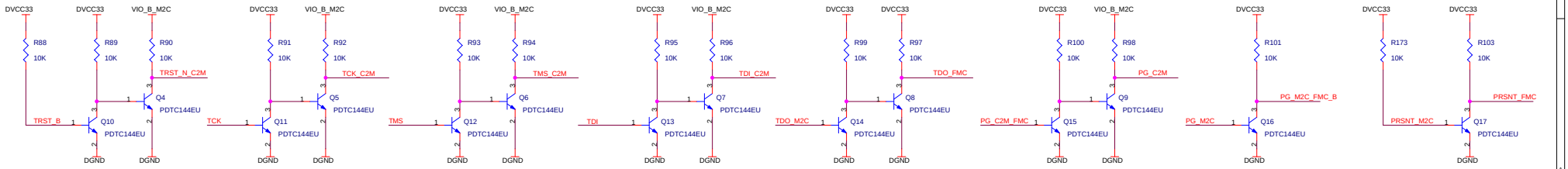
ALL CAPACITORS ARE 0402

LOW PIN COUNT



HIGH PIN COUNT





NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 0603.
2. ALL CAPACITORS ARE 0402

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SIZE	IC NO.	REV
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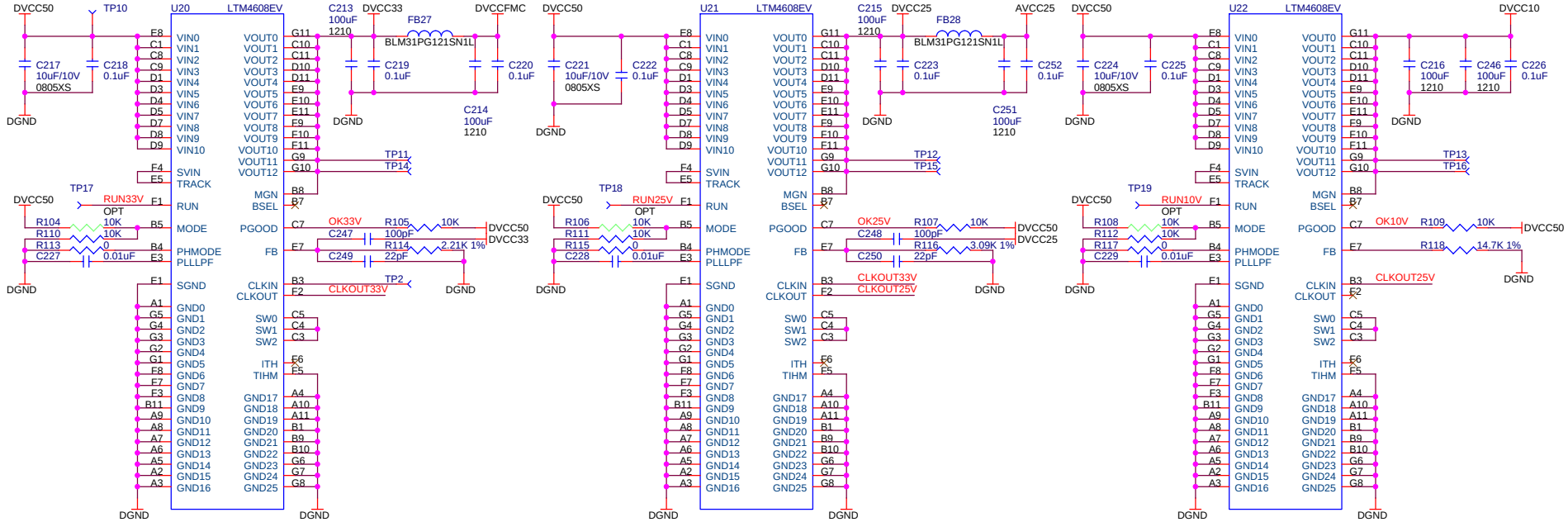
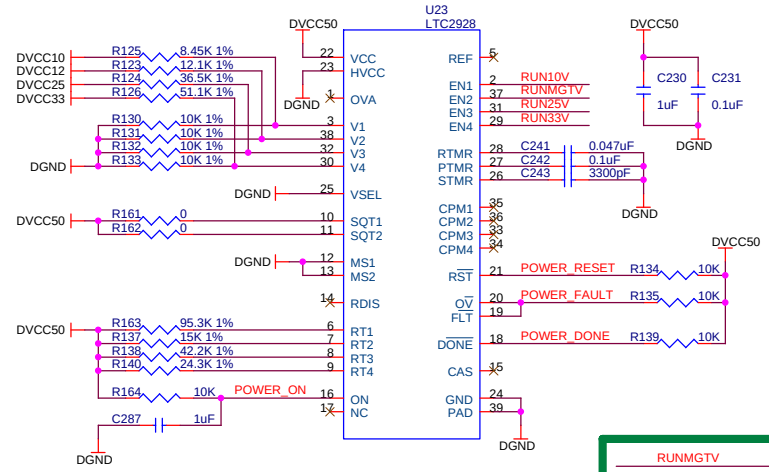
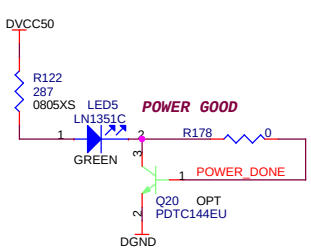
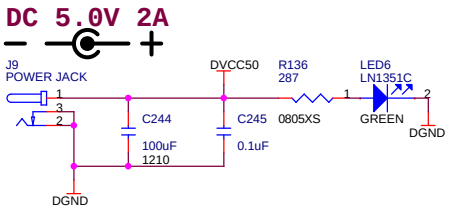
DATE: Tuesday, November 24, 2009

SHEET 12 OF 16









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1. ALL RESISTORS ARE IN OHMS, 0603.
2. ALL CAPACITORS ARE 0603

RUNMGTV — RUNMGTV 14
POWER_RESET — POWER_RESET 1
POWER_DONE — POWER_DONE 1

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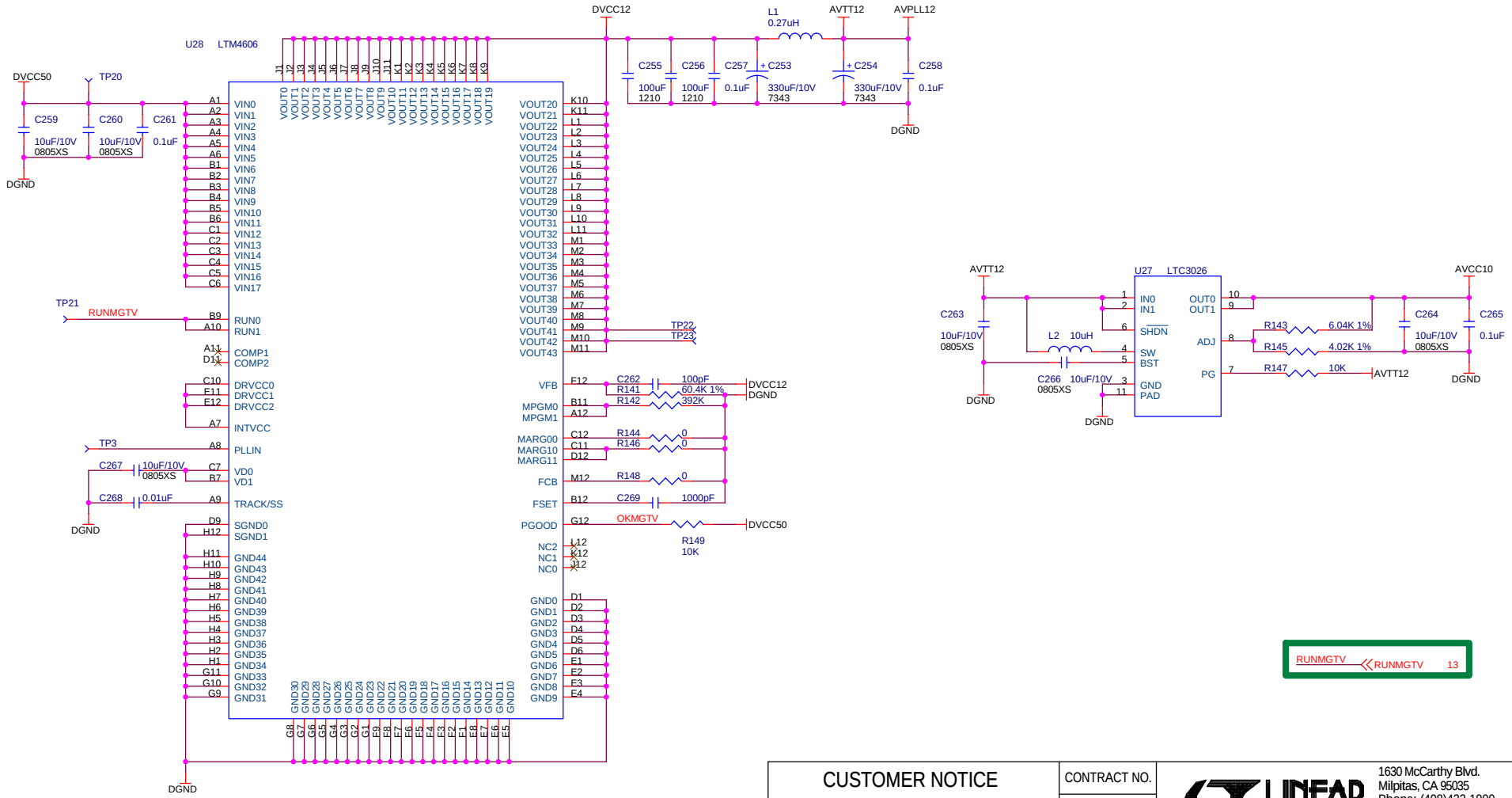
SHEET 13 OF 16



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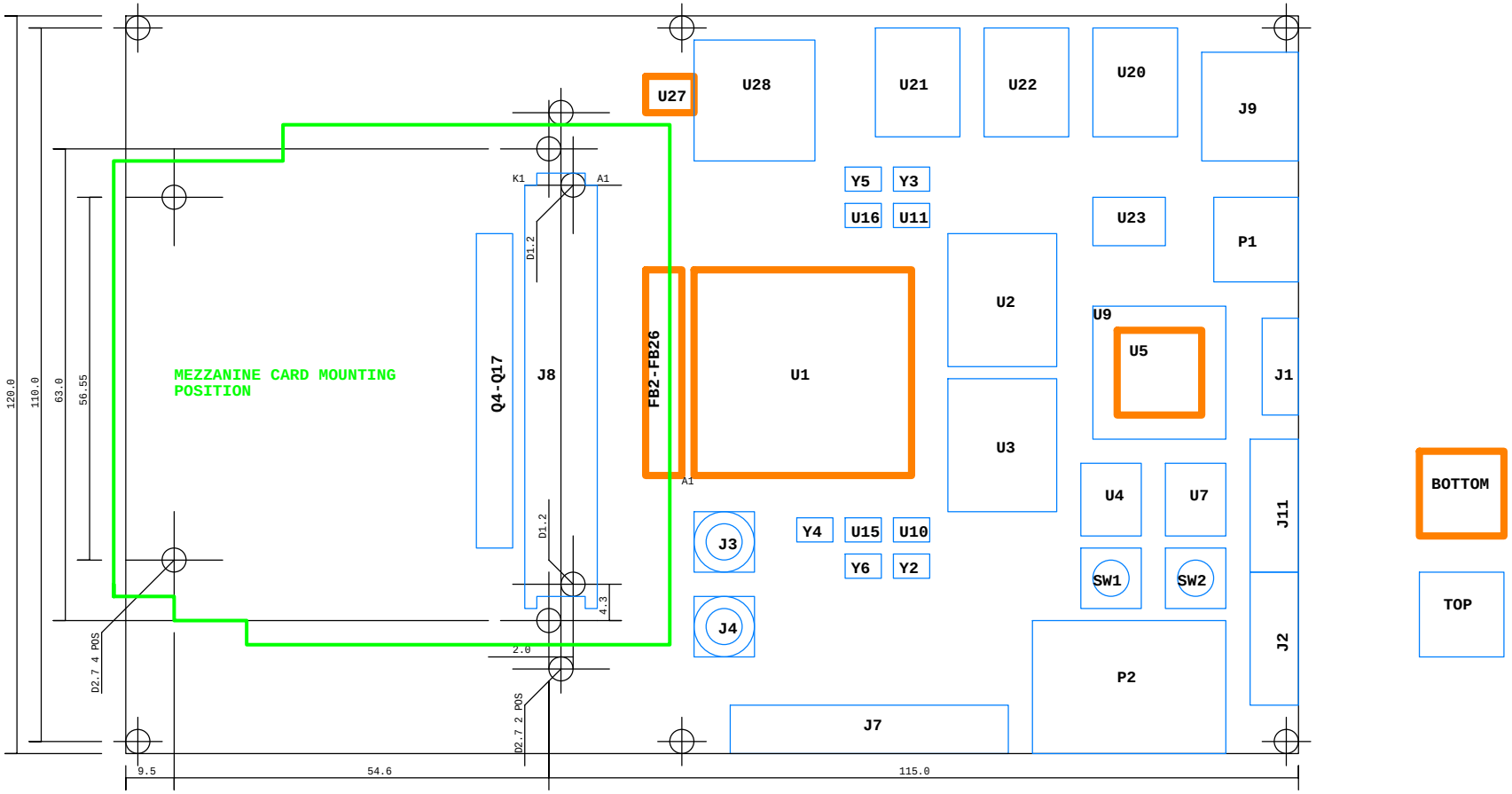
SHEET 14 OF 16



NOTES:

UNIT: mm

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Revison History

Revison A:

Initial version

Revison A - 1:

1) Added SDCARD for a flash memory option(P2).
2) Removed standby power mode.
3) Moved "MGTRXP/N0_118 to FMC low pin count.
4) Enabled CPU auto detecting USB cable plugging feature.
5) Expanded 4M bits SRAM space.
6) Fixed P1 pin assignment layout error.
7) Tied U1.V10 to ground.
8) Re-assigned HPC32, 34, 36, 38, 40, 43, 44.
9) Re-assigned CLK_118_SEL, CLK_118_ON, CLK_114_SEL, CLK_114_ON, CLK_IODLY_ON.
10) Re-assigned USERIO[23:0]. Two of them has been connected to CPLD.
11) Removed USERIO[36:24].
12) Added dedicated JTAG interface for CPU.
13) Fixed DCI issues.
14) Fixed FPGA configuration pin issues.
15) Added pullup resistors option for I2C.
16) Swapped CLK_112_EXTIN_P/N and CLK_118_EXTIN_P/N on FMC connector.

Revison 2:

1) Added Two tool mounting holes for J8 installation issue.
2) Added test points TP10-TP23.
3) Removed Test points TP6-TP9. Open solder mask on pin E4, K4 of U2 and E4, K4 of U3 on bottom side for probing.
4) Do not install Q20 and added R178.

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