**FEATURES**

- Pulse Width Modulation (PWM) Controlled by Simple 0V to 1V Analog Input
- Four Available Options Define Duty Cycle Limits
  - Minimum Duty Cycle at 0% or 5%
  - Maximum Duty Cycle at 95% or 100%
- Frequency Range: 3.81Hz to 1MHz
- Configured with 1 to 3 Resistors
- <1.7% Maximum Frequency Error
- PWM Duty Cycle Error <3.7% Maximum
- Frequency Modulation (VCO) Capability
- 2.25V to 5.5V Single Supply Operation
- 115μA Supply Current at 100kHz
- 500μs Start-Up Time
- CMOS Output Driver Sources/Sinks 20mA
- –55°C to 125°C Operating Temperature Range
- Available in Low Profile (1mm) SOT-23 (ThinSOT™) and 2mm × 3mm DFN

**APPLICATIONS**

- PWM Servo Loops
- Heater Control
- LED Dimming Control
- High Vibration, High Acceleration Environments
- Portable and Battery-Powered Equipment

**DESCRIPTION**

The LTC®6992 is a silicon oscillator with an easy-to-use analog voltage-controlled pulse width modulation (PWM) capability. The LTC6992 is part of the TimerBlox® family of versatile silicon timing devices.

A single resistor, $R_{SET}$, programs the LTC6992’s internal master oscillator frequency. The output frequency is determined by this master oscillator and an internal frequency divider, $N_{DIV}$, programmable to eight settings from 1 to 16384.

$$f_{OUT} = \frac{1MHz}{N_{DIV} \cdot \frac{50k\Omega}{R_{SET}}}, N_{DIV} = 1, 4, 16 \ldots 16384$$

Applying a voltage between 0V and 1V on the MOD pin sets the duty cycle.

The four versions differ in their minimum/maximum duty cycle. Note that a minimum duty cycle limit of 0% or maximum duty cycle limit of 100% allows oscillations to stop at the extreme duty cycle settings.

<table>
<thead>
<tr>
<th>DEVICE NAME</th>
<th>PWM DUTY CYCLE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC6992-1</td>
<td>0% to 100%</td>
</tr>
<tr>
<td>LTC6992-2</td>
<td>5% to 95%</td>
</tr>
<tr>
<td>LTC6992-3</td>
<td>0% to 95%</td>
</tr>
<tr>
<td>LTC6992-4</td>
<td>5% to 100%</td>
</tr>
</tbody>
</table>

For easy configuration of the LTC6992, download the TimerBlox Designer tool at [www.linear.com/timerblox](http://www.linear.com/timerblox).

**TYPICAL APPLICATION**

1MHz Pulse Width Modulator

- **ANALOG PWM DUTY CYCLE CONTROL (0V TO 1V)**
- **MOD**
- **OUT**
- **GND**
- **V+**
- **SET**
- **DIV**
- **RSET 50kΩ**
- **C1 0.1µF**
- **3.3V**

Graph showing MOD 0.5V/DIV and OUT 1V/DIV

2μs/DIV
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V+) to GND ........................................... 6V
Maximum Voltage On Any Pin .......................................................... (GND – 0.3V) ≤ V\text{PIN} ≤ (V+ + 0.3V)
Operating Temperature Range (Note 2)
LTC6992C ........................................... –40°C to 85°C
LTC6992I ........................................... –40°C to 85°C
LTC6992H ........................................... –40°C to 125°C
LTC6992MP ....................................... –55°C to 125°C

Specified Temperature Range (Note 3)
LTC6992C ........................................... 0°C to 70°C
LTC6992I ........................................... –40°C to 85°C
LTC6992H ........................................... –40°C to 125°C
LTC6992MP ....................................... –55°C to 125°C
Junction Temperature ........................................... 150°C
Storage Temperature Range ........................................... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) S6 Package ......................... 300°C

PIN CONFIGURATION

ORDER INFORMATION

Lead Free Finish

<table>
<thead>
<tr>
<th>TAPE AND REEL (MINI)</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>SPECIFIED TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC6992DCB-1#TRMPBF</td>
<td>LTC6992DCB-1#TRPBF</td>
<td>LDXC</td>
<td>6-Lead (2mm × 3mm) Plastic DFN</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC6992DCB-1#TRMPBF</td>
<td>LTC6992DCB-1#TRPBF</td>
<td>LDXC</td>
<td>6-Lead (2mm × 3mm) Plastic DFN</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LTC6992DCB-1#TRMPBF</td>
<td>LTC6992DCB-1#TRPBF</td>
<td>LDXC</td>
<td>6-Lead (2mm × 3mm) Plastic DFN</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LTC6992DCB-2#TRMPBF</td>
<td>LTC6992DCB-2#TRPBF</td>
<td>LDXF</td>
<td>6-Lead (2mm × 3mm) Plastic DFN</td>
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</tr>
<tr>
<td>LTC6992DCB-2#TRMPBF</td>
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<td>LDXF</td>
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<tr>
<td>LTC6992DCB-3#TRMPBF</td>
<td>LTC6992DCB-3#TRPBF</td>
<td>LFPC</td>
<td>6-Lead (2mm × 3mm) Plastic DFN</td>
<td>0°C to 70°C</td>
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<td>LTC6992DCB-3#TRPBF</td>
<td>LFPC</td>
<td>6-Lead (2mm × 3mm) Plastic DFN</td>
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<tr>
<td>LTC6992DCB-1#TRMPBF</td>
<td>LTC6992DCB-1#TRPBF</td>
<td>LTDX</td>
<td>6-Lead Plastic TSOT-23</td>
<td>0°C to 70°C</td>
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<tr>
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<td>LTC6992DCB-1#TRPBF</td>
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<td>6-Lead Plastic TSOT-23</td>
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<tr>
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<tr>
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</tr>
<tr>
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<td>LTC6992DCB-3#TRPBF</td>
<td>LTDX</td>
<td>6-Lead Plastic TSOT-23</td>
<td>–40°C to 125°C</td>
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Lead Free Finish

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<tr>
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<th>PACKAGE DESCRIPTION</th>
<th>SPECIFIED TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC6992CDCB-4#TRMPBF</td>
<td>LTC6992CDCB-4#TRMPBF</td>
<td>LFCR</td>
<td>6-Lead (2mm × 3mm) Plastic DFN</td>
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<tr>
<td>LTC6992SDBB-4#TRMPBF</td>
<td>LTC6992SDBB-4#TRMPBF</td>
<td>LFCR</td>
<td>6-Lead (2mm × 3mm) Plastic DFN</td>
<td>−40°C to 85°C</td>
</tr>
<tr>
<td>LTC6992G6-4#TRMPBF</td>
<td>LTC6992G6-4#TRMPBF</td>
<td>LFCR</td>
<td>6-Lead Plastic TSOT-23</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC6992H6-4#TRMPBF</td>
<td>LTC6992H6-4#TRMPBF</td>
<td>LFCR</td>
<td>6-Lead Plastic TSOT-23</td>
<td>−40°C to 125°C</td>
</tr>
<tr>
<td>LTC6992K6-4#TRMPBF</td>
<td>LTC6992K6-4#TRMPBF</td>
<td>LFCR</td>
<td>6-Lead Plastic TSOT-23</td>
<td>−55°C to 125°C</td>
</tr>
<tr>
<td>LTC6992CS6-4#TRMPBF</td>
<td>LTC6992CS6-4#TRMPBF</td>
<td>LFCR</td>
<td>6-Lead Plastic TSOT-23</td>
<td>−55°C to 125°C</td>
</tr>
</tbody>
</table>

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.
Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.
For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)
For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C. Test conditions are V+ = 2.25V to 5.5V, VMOD = 0V to VSET, DIVCODE = 0 to 15 (NDIV = 1 to 16,384), RSET = 50k to 800k, RLOAD = 5k, CLOAD = 5pF unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>fOUT</td>
<td>Output Frequency</td>
<td>3.81</td>
<td>1000000 Hz</td>
</tr>
<tr>
<td>ΔfOUT</td>
<td>Frequency Accuracy (Note 4)</td>
<td>3.81Hz ≤ fOUT ≤ 1MHz</td>
<td>±0.8</td>
</tr>
<tr>
<td>ΔfOUT/ΔT</td>
<td>Frequency Drift Over Temperature</td>
<td>●</td>
<td>±0.005</td>
</tr>
<tr>
<td>ΔfOUT/ΔV+</td>
<td>Frequency Drift Over Supply</td>
<td>V+ = 4.5V to 5.5V</td>
<td>0.25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V+ = 2.25V to 4.5V</td>
<td>0.08</td>
</tr>
<tr>
<td>Long-Term Frequency Stability</td>
<td>(Note 10)</td>
<td>90 ppm/√kHz</td>
<td></td>
</tr>
<tr>
<td>Period Jitter (Note 9)</td>
<td>NDIV = 1</td>
<td>1.2</td>
<td>%p-p</td>
</tr>
<tr>
<td></td>
<td>NDIV = 4</td>
<td>0.4</td>
<td>%p-p</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.07</td>
<td>%p-p</td>
</tr>
<tr>
<td></td>
<td>NDIV = 16</td>
<td>0.15</td>
<td>%p-p</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.022</td>
<td>%p-p</td>
</tr>
<tr>
<td>Pulse Width Modulation</td>
<td>D</td>
<td>PWM Duty Cycle Accuracy</td>
<td>VMOD = 0.2•VSET to 0.8•VSET</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VMOD = 0.2•VSET to 0.8•VSET</td>
<td>●</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VMOD &lt; 0.2•VSET or VMOD &gt; 0.8•VSET</td>
<td>●</td>
</tr>
<tr>
<td>DMAX</td>
<td>Maximum Duty Cycle Limit</td>
<td>LTC6992-1/LTC6992-4, POL = 0, VMOD = 1V</td>
<td>●</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LTC6992-2/LTC6992-3, POL = 0, VMOD = 1V</td>
<td>●</td>
</tr>
<tr>
<td>DMIN</td>
<td>Minimum Duty Cycle Limit</td>
<td>LTC6992-1/LTC6992-3, POL = 0, VMOD = 0V</td>
<td>●</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LTC6992-2/LTC6992-4, POL = 0, VMOD = 0V</td>
<td>●</td>
</tr>
<tr>
<td>tS,PWM</td>
<td>Duty Cycle Settling Time (Note 6)</td>
<td>tMASTER = tOUT/NDIV</td>
<td>8•tMASTER</td>
</tr>
</tbody>
</table>

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)
For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)
The electrical characteristics of the LTC6992-1/LTC6992-2/LTC6992-3/LTC6992-4 denote the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. Test conditions are $V^+ = 2.25V$ to $5.5V$, $V_{MOD} = 0V$ to $V_{SET}$, $DIVCODE = 0$ to $15$ ($N_{DIV} = 1$ to $16,384$), $R_{SET} = 50k$ to $800k$, $R_{LOAD} = 5k$, $C_{LOAD} = 5pF$ unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply</td>
<td>$V^+$</td>
<td>Operating Supply Voltage Range</td>
<td>●</td>
<td>2.25</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power-On Reset Voltage</td>
<td>●</td>
<td>1.95</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td>$R_L = \infty$, $R_{SET} = 50k$, $N_{DIV} = 1$</td>
<td>$V^+ = 5.5V$</td>
<td>●</td>
<td>365</td>
<td>450</td>
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<td></td>
<td></td>
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<td>$V^+ = 2.25V$</td>
<td>●</td>
<td>225</td>
<td>285</td>
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<td>$R_L = \infty$, $R_{SET} = 50k$, $N_{DIV} = 4$</td>
<td>$V^+ = 5.5V$</td>
<td>●</td>
<td>350</td>
<td>420</td>
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<td>$V^+ = 2.25V$</td>
<td>●</td>
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<td>280</td>
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<tr>
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<td>$R_L = \infty$, $R_{SET} = 800k$, $N_{DIV} = 1$ to $16,384$</td>
<td>$V^+ = 5.5V$</td>
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<td>120</td>
<td>170</td>
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<td>$V^+ = 2.25V$</td>
<td>●</td>
<td>105</td>
<td>150</td>
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<tr>
<td>Analog Inputs</td>
<td>$V_{SET}$</td>
<td>Voltage at SET Pin</td>
<td>●</td>
<td>0.97</td>
<td>1.00</td>
<td>1.03</td>
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<tr>
<td></td>
<td>$\Delta V_{SET}/\Delta T$</td>
<td>$V_{SET}$ Drift Over Temperature</td>
<td>●</td>
<td>±75</td>
<td></td>
<td>V/°C</td>
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<td>$R_{SET}$</td>
<td>Frequency-Setting Resistor</td>
<td>●</td>
<td>50</td>
<td>800</td>
<td>kΩ</td>
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<td>MOD Pin Input Capacitance</td>
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<td></td>
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<td>pF</td>
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<td>MOD Pin Input Current</td>
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<td></td>
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<td>±10 nA</td>
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<td></td>
<td>$V_{MOD,HI}$</td>
<td>$V_{MOD}$ Voltage for Maximum Duty Cycle</td>
<td></td>
<td>0.90$\cdot V_{SET}$</td>
<td>0.936$\cdot V_{SET}$</td>
<td>V</td>
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<tr>
<td></td>
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<td>LTC6992-1/LTC6992-4, POL = 0, D = 100%</td>
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<td>0.90$\cdot V_{SET}$</td>
<td>0.936$\cdot V_{SET}$</td>
<td>V</td>
</tr>
<tr>
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<td></td>
<td>LTC6992-2/LTC6992-3, POL = 0, D = 95%</td>
<td></td>
<td>0.86$\cdot V_{SET}$</td>
<td>0.936$\cdot V_{SET}$</td>
<td>V</td>
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<tr>
<td></td>
<td>$V_{MOD,LO}$</td>
<td>$V_{MOD}$ Voltage for Minimum Duty Cycle</td>
<td></td>
<td>0.064$\cdot V_{SET}$</td>
<td>0.10$\cdot V_{SET}$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LTC6992-1/LTC6992-3, POL = 0, D = 0%</td>
<td></td>
<td>0.064$\cdot V_{SET}$</td>
<td>0.10$\cdot V_{SET}$</td>
<td>V</td>
</tr>
<tr>
<td></td>
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<td>LTC6992-2/LTC6992-4, POL = 0, D = 5%</td>
<td></td>
<td>0.14$\cdot V_{SET}$</td>
<td>0.16$\cdot V_{SET}$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{DIV}$</td>
<td>DIV Pin Voltage</td>
<td>●</td>
<td>0</td>
<td>$V^+$</td>
<td>V</td>
</tr>
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<td></td>
<td>$\Delta V_{DIV}/\Delta V^+$</td>
<td>DIV Pin Valid Code Range (Note 5) Deviation from Ideal</td>
<td></td>
<td>$V_{DIV}/V^+$ = (DIVCODE + 0.5)/16</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>DIV Pin Input Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±10 nA</td>
</tr>
<tr>
<td>Digital Output</td>
<td>$I_{OUT(MAX)}$</td>
<td>Output Current</td>
<td>$V^+ = 2.7V$ to $5.5V$</td>
<td></td>
<td>±20</td>
<td>mA</td>
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<tr>
<td></td>
<td>$V_{DH}$</td>
<td>High Level Output Voltage (Note 7)</td>
<td>$V^+ = 5.5V$</td>
<td>$I_{OUT} = -1mA$</td>
<td>5.45</td>
<td>5.48</td>
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<td></td>
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<td>$I_{OUT} = -16mA$</td>
<td>●</td>
<td>4.84</td>
<td>5.15</td>
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<td></td>
<td>$V^+ = 3.3V$</td>
<td>$I_{OUT} = -1mA$</td>
<td>3.24</td>
<td>3.27</td>
<td>V</td>
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<td>$I_{OUT} = -10mA$</td>
<td>●</td>
<td>2.75</td>
<td>2.99</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^+ = 2.25V$</td>
<td>$I_{OUT} = -1mA$</td>
<td>2.17</td>
<td>2.21</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$I_{OUT} = -8mA$</td>
<td>●</td>
<td>1.58</td>
<td>1.88</td>
</tr>
<tr>
<td></td>
<td>$V_{DL}$</td>
<td>Low Level Output Voltage (Note 7)</td>
<td>$V^+ = 5.5V$</td>
<td>$I_{OUT} = 1mA$</td>
<td>0.02</td>
<td>0.04</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$I_{OUT} = 16mA$</td>
<td>●</td>
<td>0.26</td>
<td>0.54</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^+ = 3.3V$</td>
<td>$I_{OUT} = 1mA$</td>
<td>0.03</td>
<td>0.05</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$I_{OUT} = 10mA$</td>
<td>●</td>
<td>0.22</td>
<td>0.46</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^+ = 2.25V$</td>
<td>$I_{OUT} = 1mA$</td>
<td>0.03</td>
<td>0.07</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$I_{OUT} = 8mA$</td>
<td>●</td>
<td>0.26</td>
<td>0.54</td>
</tr>
<tr>
<td></td>
<td>$t_r$</td>
<td>Output Rise Time (Note 8)</td>
<td>$V^+ = 5.5V$, $R_{LOAD} = \infty$</td>
<td></td>
<td>1.1</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V^+ = 3.3V$, $R_{LOAD} = \infty$</td>
<td></td>
<td>1.7</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V^+ = 2.25V$, $R_{LOAD} = \infty$</td>
<td></td>
<td>2.7</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>$t_f$</td>
<td>Output Fall Time (Note 8)</td>
<td>$V^+ = 5.5V$, $R_{LOAD} = \infty$</td>
<td></td>
<td>1.0</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V^+ = 3.3V$, $R_{LOAD} = \infty$</td>
<td></td>
<td>1.6</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V^+ = 2.25V$, $R_{LOAD} = \infty$</td>
<td></td>
<td>2.4</td>
<td>ns</td>
</tr>
</tbody>
</table>
ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6992C is guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 3: The LTC6992C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6992C is designed, characterized and expected to meet specified performance from –40°C to 85°C but it is not tested or QA sampled at these temperatures. The LTC6992C is guaranteed to meet specified performance from –40°C to 85°C. The LTC6992H is guaranteed to meet specified performance from –40°C to 125°C. The LTC6992MP is guaranteed to meet specified performance from –55°C to 125°C.

Note 4: Frequency accuracy is defined as the deviation from the f_{OUT} equation, assuming R_{SET} is used to program the frequency.

Note 5: See Operation section, Table 1 and Figure 2 for a full explanation of how the DIV pin voltage selects the value of DIVCODE.

Note 6: Duty cycle settling time is the amount of time required for the output to settle within ±1% of the final duty cycle after a ±10% change in the setting (±80mV step in V_{MOD}).

Note 7: To conform to the Logic IC Standard, current out of a pin is arbitrarily given a negative value.

Note 8: Output rise and fall times are measured between the 10% and the 90% power supply levels with 5pF output load. These specifications are based on characterization.

Note 9: Jitter is the ratio of the peak-to-peak deviation of the period to the mean of the period. This specification is based on characterization and is not 100% tested.

Note 10: Long-term drift of silicon oscillators is primarily due to the movement of ions and impurities within the silicon and is tested at 30°C under otherwise nominal operating conditions. Long-term drift is specified as ppm/√kHr due to the typically nonlinear nature of the drift. To calculate drift for a set time period, translate that time into thousands of hours, take the square root and multiply by the typical drift number. For instance, a year is 8.77kHr and would yield a drift of 266ppm at 90ppm/√kHr. Drift without power applied to the device may be approximated as 1/10th of the drift with power, or 9ppm/√kHr for a 90ppm/√kHr device.

TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

Frequency Error vs Temperature

Guaranteed Max Over Temperature

Guaranteed Min Over Temperature

R_{SET} = 50k

3 PARTS

R_{SET} = 200k

3 PARTS

R_{SET} = 800k

3 PARTS
Typical Performance Characteristics

- **Frequency Error vs RSET**
- **Frequency Drift vs Supply Voltage**
- **Typical VSET Distribution**
- **VSET Drift vs ISET**
- **VSET Drift vs Supply**
- **VSET vs Temperature**

**Note:** V+ = 3.3V, RSET = 200k, and TA = 25°C, unless otherwise noted.
Typical Performance Characteristics

V+ = 3.3V, RSET = 200k, and TA = 25°C, unless otherwise noted.

N_{DIV} > 1 Duty Cycle Error vs RSET

N_{DIV} = 1 Duty Cycle Error vs RSET

N_{DIV} = 1 Duty Cycle Clamps vs RSET

N_{DIV} = 1 Duty Cycle Error vs Temperature

N_{DIV} > 1 Duty Cycle Error vs Temperature
Typical Performance Characteristics

V+ = 3.3V, RSET = 200k, and TA = 25°C, unless otherwise noted.

**NDIV > 1 Duty Cycle Error vs Temperature**

![Graph showing Duty Cycle Error vs Temperature for NDIV > 1 with different DIVCODE settings.](image1)

**NDIV > 1 Duty Cycle Error vs Temperature**

![Graph showing Duty Cycle Error vs Temperature for NDIV > 1 with different DIVCODE settings.](image2)

**NDIV > 1 Duty Cycle Clamps vs Temperature**

![Graph showing Duty Cycle Clamps vs Temperature for NDIV > 1 with different DIVCODE settings.](image3)

**NDIV > 1 Duty Cycle Clamps vs Temperature**

![Graph showing Duty Cycle Clamps vs Temperature for NDIV > 1 with different DIVCODE settings.](image4)

**Duty Cycle Error vs DIVCODE**

![Graph showing Duty Cycle Error vs DIVCODE.](image5)

**Duty Cycle Error vs DIVCODE**

![Graph showing Duty Cycle Error vs DIVCODE.](image6)

**NDIV > 1 Duty Cycle vs VMOD/VSET**

![Graph showing Duty Cycle vs VMOD/VSET for NDIV > 1 with different DIVCODE settings.](image7)

**NDIV > 1 Duty Cycle vs VMOD/VSET**

![Graph showing Duty Cycle vs VMOD/VSET for NDIV > 1 with different DIVCODE settings.](image8)

**NDIV > 1 Duty Cycle Clamps vs VMOD/VSET**

![Graph showing Duty Cycle Clamps vs VMOD/VSET for NDIV > 1 with different DIVCODE settings.](image9)

**NDIV > 1 Duty Cycle Clamps vs VMOD/VSET**

![Graph showing Duty Cycle Clamps vs VMOD/VSET for NDIV > 1 with different DIVCODE settings.](image10)

**NDIV = 1 Duty Cycle Clamps vs VMOD/VSET**

![Graph showing Duty Cycle Clamps vs VMOD/VSET for NDIV = 1 with different DIVCODE settings.](image11)

**NDIV = 1 Duty Cycle Clamps vs VMOD/VSET**

![Graph showing Duty Cycle Clamps vs VMOD/VSET for NDIV = 1 with different DIVCODE settings.](image12)
TYPICAL PERFORMANCE CHARACTERISTICS

\( V^* = 3.3\text{V}, \, R_{\text{SET}} = 200\text{k}, \, \text{and} \, T_A = 25^\circ\text{C}, \) unless otherwise noted.

### Linearity Near 100% Duty Cycle

- **VMOD/VSET (V/V)**: 0.836, 0.804, 0.9
- **DUTY CYCLE (%)**: 100

### Linearity Near 95% Duty Cycle

- **VMOD/VSET (V/V)**: 0.836, 0.804, 0.9
- **DUTY CYCLE (%)**: 95

### Linearity Near 67% Duty Cycle

- **VMOD/VSET (V/V)**: 0.612, 0.628, 0.644, 0.596, 0.676
- **DUTY CYCLE (%)**: 67

### Linearity Near 0% Duty Cycle

- **VMOD/VSET (V/V)**: 0.116, 0.148, 0.084
- **DUTY CYCLE (%)**: 0

### Linearity Near 5% Duty Cycle

- **VMOD/VSET (V/V)**: 0.116, 0.148, 0.084
- **DUTY CYCLE (%)**: 5
**Typical Performance Characteristics**

- **Linearity Near 31% Duty Cycle**
  - DIVCODE = 4
  - 3 Parts

- **N\textsubscript{DIV} = 1 Duty Cycle Drift vs Supply**
  - DIVCODE = 0
  - 5% CLAMP, 95% CLAMP
  - V\textsubscript{MOD}/V\textsubscript{SET} = 0.8
  - V\textsubscript{MOD}/V\textsubscript{SET} = 0.2
  - V\textsubscript{MOD}/V\textsubscript{SET} = 0.5
  - Referenced to V\textsuperscript{+} = 4V

- **N\textsubscript{DIV} > 1 Duty Cycle Drift vs Supply**
  - DIVCODE = 4
  - 5% CLAMP, 95% CLAMP
  - V\textsubscript{MOD}/V\textsubscript{SET} = 0.2
  - V\textsubscript{MOD}/V\textsubscript{SET} = 0.5
  - Referenced to V\textsuperscript{+} = 4V

- **Supply Current vs VMOD**
  - LTC6992-2
  - R\textsubscript{SET} = 50k, +1
  - R\textsubscript{SET} = 50k, +16
  - R\textsubscript{SET} = 100k, +4
  - R\textsubscript{SET} = 800k, +1

- **Supply Current vs Supply Voltage**
  - Supply Current vs Frequency
  - 5V Supply Current vs Frequency
  - 2.5V Supply Current vs Frequency

- **Supply Current vs Temperature**
  - 5.0V, R\textsubscript{SET} = 50k, +1
  - 5.0V, R\textsubscript{SET} = 50k, +16
  - 2.5V, R\textsubscript{SET} = 50k, +1
  - 2.5V, R\textsubscript{SET} = 800k, +1

- **Jitter vs Frequency**
  - 5V
  - 2.5V

- **Other Characteristics**
  - V\textsuperscript{+} = 3.3V, R\textsubscript{SET} = 200k, and T\textsubscript{A} = 25°C, unless otherwise noted.
TYPICAL PERFORMANCE CHARACTERISTICS

Typical Frequency Error vs Time (Long-Term Drift)

Typical Output Resistance vs Supply Voltage

Rise and Fall Time vs Supply Voltage

Typical I_SET Current Limit vs V^+

Typical Start-Up, POL = 0

Typical Start-Up, POL = 1

125kHz Full Modulation

V^+ = 3.3V, R_SET = 200k, and T_A = 25°C, unless otherwise noted.

V^+ = 2.3V
DIVCODE = 3 (-64)
R_SET = 50k
V_MOD = 0.3V (~25% DUTY CYCLE)

V^+ = 3.3V
DIVCODE = 1
R_SET = 100k

V^+ = 2.5V
DIVCODE = 12 (~64, POL = 1)
R_SET = 50k
V_MOD = 0.2V (~87.5% DUTY CYCLE)
PIN FUNCTIONS (DCB/S6)

V+ (Pin 1/Pin 5): Supply Voltage (2.25V to 5.5V). This supply should be kept free from noise and ripple. It should be bypassed directly to the GND pin with a 0.1µF capacitor.

DIV (Pin 2/Pin 4): Programmable Divider and Polarity Input. The DIV pin voltage (V_DIV) is internally converted into a 4-bit result (DIVCODE). V_DIV may be generated by a resistor divider between V+ and GND. Use 1% resistors to ensure an accurate result. The DIV pin and resistors should be shielded from the OUT pin or any other traces that have fast edges. Limit the capacitance on the DIV pin to less than 100pF so that V_DIV settles quickly. The MSB of DIVCODE (POL) determines if the PWM signal is inverted before driving the output. When POL = 1 the transfer function is inverted (duty cycle decreasing as V_MOD increases).

SET (Pin 3/Pin 3): Frequency-Setting Input. The voltage on the SET pin (V_SET) is regulated to 1V above GND. The amount of current sourced from the SET pin (I_SET) programs the master oscillator frequency. The I_SET current range is 1.25µA to 20µA. The output oscillation will stop if I_SET drops below approximately 500nA. A resistor connected between SET and GND is the most accurate way to set the frequency. For best performance, use a precision metal or thin film resistor of 0.5% or better tolerance and 50ppm/°C or better temperature coefficient. For lower accuracy applications an inexpensive 1% thick film resistor may be used.

OUT (Pin 6/Pin 6): Oscillator Output. The OUT pin swings from GND to V+ with an output resistance of approximately 30Ω. The duty cycle is determined by the voltage on the MOD pin. When driving an LED or other low-impedance load a series output resistor should be used to limit the source/sink current to 20mA.

Limit the capacitance on the SET pin to less than 10pF to minimize jitter and ensure stability. Capacitance less than 100pF maintains the stability of the feedback circuit regulating the V_SET voltage.

MOD (Pin 4/Pin 1): Pulse-Width Modulation Input. The voltage on the MOD pin controls the output duty cycle. The linear control range is between 0.1 • V_SET and 0.9 • V_SET (approximately 100mV to 900mV). Beyond those limits, the output will either clamp at 5% or 95%, or stop oscillating (0% or 100% duty cycle), depending on the version.

GND (Pin 5/Pin 2): Ground. Tie to a low inductance ground plane for best performance.
**LTC6992-1/LTC6992-2/
LTC6992-3/LTC6992-4**

** BLOCK DIAGRAM **
(S6 Package Pin Numbers Shown)

**Diagram Details:**
- **4-Bit A/D Converter**
- **Digital Filter**
- **Master Oscillator**
  - $f_{osc} = 1$ MHz $\times 50k\Omega$ $\times \frac{I_{set}}{V_{set}}$
- **Programmable Divider**
  - +1, 4, 16, 64, 256, 1024, 4096, 16384
- **Pulse Width Modulator**
  - Duty Cycle: $\frac{V_{mod(lim)} - 0.1 \times V_{set}}{0.8 \times V_{set}}$
- **Voltage Limiter**
- **Output Polarity**

**Connections:**
- $V^+$
- $S$
- $R1$ (DIV)
- $R2$
- $4$ (4-Bit A/D Converter)
- $DOUT$
- $DIN$
- $SET$
- $ISET$
- $RSET$
- $VSET = 1V$
- $V_{REF} = 1V$
- $GND$
- $MOD$
- $MCLK$
- $POR$
The LTC6992 is built around a master oscillator with a 1MHz maximum frequency. The oscillator is controlled by the SET pin current (I_SET) and voltage (V_SET), with a 1MHz • 50k conversion factor that is accurate to ±0.8% under typical conditions.

\[ f_{\text{MASTER}} = \frac{1}{t_{\text{MASTER}}} = 1\text{MHz} \times 50k \times \frac{I_{\text{SET}}}{V_{\text{SET}}} \]

A feedback loop maintains V_SET at 1V ±30mV, leaving I_SET as the primary means of controlling the output frequency. The simplest way to generate I_SET is to connect a resistor (R_SET) between SET and GND, such that I_SET = V_SET/R_SET.

The master oscillator equation reduces to:

\[ f_{\text{MASTER}} = \frac{1}{t_{\text{MASTER}}} = 1\text{MHz} \times 50k \times \frac{R_{\text{SET}}}{R_{\text{SET}}} \]

From this equation, it is clear that V_SET drift will not affect the output frequency when using a single program resistor (R_SET). Error sources are limited to R_SET tolerance and the inherent frequency accuracy \( \Delta f_{\text{OUT}} \) of the LTC6992.

R_SET may range from 50k to 800k (equivalent to I_SET between 1.25μA and 20μA).

The LTC6992 includes a programmable frequency divider which can further divide the frequency by 1, 4, 16, 64, 256, 1024, 4096 or 16384 before driving the OUT pin. The divider ratio N_DIV is set by a resistor divider attached to the DIV pin.

\[ f_{\text{OUT}} = \frac{1}{t_{\text{OUT}}} = 1\text{MHz} \times 50k \times \frac{I_{\text{SET}}}{V_{\text{SET}}} \]

With R_SET in place of V_SET/I_SET the equation reduces to:

\[ f_{\text{OUT}} = \frac{1}{t_{\text{OUT}}} = 1\text{MHz} \times 50k \times \frac{N_{\text{DIV}}}{R_{\text{SET}}} \]

DIVCODE

The DIV pin connects to an internal, V^+ referenced 4-bit A/D converter that determines the DIVCODE value. DIVCODE programs two settings on the LTC6992:

1. DIVCODE determines the output frequency divider setting, N_DIV.
2. DIVCODE determines the output polarity, via the POL bit.

V_DIV may be generated by a resistor divider between V^+ and GND as shown in Figure 1.

![Figure 1. Simple Technique for Setting DIVCODE](image)
Table 1 offers recommended 1% resistor values that accurately produce the correct voltage division as well as the corresponding NDIV and POL values for the recommended resistor pairs. Other values may be used as long as:

1. The $V_{DIV}/V^+$ ratio is accurate to ±1.5% (including resistor tolerances and temperature effects).
2. The driving impedance ($R_1||R_2$) does not exceed 500kΩ.

If the voltage is generated by other means (i.e., the output of a DAC) it must track the $V^+$ supply voltage. The last column in Table 1 shows the ideal ratio of $V_{DIV}$ to the supply voltage, which can also be calculated as:

$$\frac{V_{DIV}}{V^+} = \frac{\text{DIVCODE} + 0.5}{16} \pm 1.5\%$$

For example, if the supply is 3.3V and the desired DIVCODE is 4, $V_{DIV} = 0.281 \cdot 3.3V = 928mV \pm 50mV$.

Figure 2 illustrates the information in Table 1, showing that $N_{DIV}$ is symmetric around the DIVCODE midpoint.
**Pulse Width (Duty Cycle) Modulation**

The MOD pin is a high impedance analog input providing direct control of the output duty cycle. The duty cycle is proportional to the voltage applied to the MOD pin, $V_{MOD}$.

$$\text{Duty Cycle} = D = \frac{V_{MOD}}{0.8 \cdot V_{SET}} - \frac{1}{8}$$

The PWM duty cycle accuracy $\Delta D$ specifies that the above equation is valid to within ±4.5% for $V_{MOD}$ between $0.2 \cdot V_{SET}$ and $0.8 \cdot V_{SET}$ (12.5% to 87.5% duty cycle).

Since $V_{SET} = 1V \pm 30mV$, the duty cycle equation may be approximated by the following equation.

$$\text{Duty Cycle} \approx D = \frac{V_{MOD} - 100mV}{800mV}$$

The $V_{MOD}$ control range is approximately 0.1V to 0.9V. Driving $V_{MOD}$ beyond that range (towards GND or $V^*$) will have no further affect on the duty cycle.

**Duty Cycle Limits**

The only difference between the four versions of the LTC6992 is the limits, or clamps, placed on the output duty cycle. The LTC6992-1 generates output duty cycles ranging from 0% to 100%. At 0% or 100% the output will stop oscillating and rest at GND or $V^*$, respectively.

The LTC6992-2 will never stop oscillating, regardless of the $V_{MOD}$ level. Internal clamping circuits limit its duty cycle to a 5% to 95% range (1% to 99% guaranteed). Therefore, its $V_{MOD}$ control range is $0.14 \cdot V_{SET}$ to $0.86 \cdot V_{SET}$ (approximately 0.14V to 0.86V).

The LTC6992-3 and LTC6992-4 complete the family by providing one-sided clamping. The LTC6992-3 allows 0% to 95% duty cycle, and the LTC6992-4 allows 5% to 100% duty cycle.

**Output Polarity (POL Bit)**

The duty cycle equation describes a proportional transfer function, where duty cycle increases as $V_{MOD}$ increases. The LTC6992 includes a POL bit (determined by the DIVCODE as described earlier) that inverts the output signal. This makes the duty cycle gain negative, reducing duty cycle as $V_{MOD}$ increases.
OPERATION

POL = 1 forces a simple logic inversion, so it changes the duty cycle range of the LTC6992-3 (making it 100% to 5%) and LTC6992-4 (making it 95% to 0%). These transfer functions are detailed in Figure 4.

Table 2. Duty Cycle Ranges

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DUTY CYCLE RANGE vs ( V_{MOD} = 0V \rightarrow 1V )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>POL = 0</td>
</tr>
<tr>
<td>LTC6992-1</td>
<td>0% to 100%</td>
</tr>
<tr>
<td>LTC6992-2</td>
<td>5% to 95%</td>
</tr>
<tr>
<td>LTC6992-3</td>
<td>0% to 95%</td>
</tr>
<tr>
<td>LTC6992-4</td>
<td>5% to 100%</td>
</tr>
</tbody>
</table>

Figure 4. PWM Transfer Functions for All LTC6992 Family Parts
Changing DIVCODE After Start-Up

Following start-up, the A/D converter will continue monitoring $V_{\text{DIV}}$ for changes. Changes to DIVCODE will be recognized slowly, as the LTC6992 places a priority on eliminating any “wandering” in the DIVCODE. The typical delay depends on the difference between the old and new DIVCODE settings and is proportional to the master oscillator period.

$$t_{\text{DIVCODE}} = 16 \times (\Delta \text{DIVCODE} + 6) \times t_{\text{MASTER}}$$

A change in DIVCODE will not be recognized until it is stable, and will not pass through intermediate codes. A digital filter is used to guarantee the DIVCODE has settled to a new value before making changes to the output. Then the output will make a clean (glitchless) transition to the new divider setting.

Start-Up Time

When power is first applied, the power-on reset (POR) circuit will initiate the start-up time, $t_{\text{START}}$. The OUT pin is held low during this time. The typical value for $t_{\text{START}}$ ranges from 0.5ms to 8ms depending on the master oscillator frequency (independent of $N_{\text{DIV}}$):

$$t_{\text{START(TYP)}} = 500 \times t_{\text{MASTER}}$$

The output will begin oscillating after $t_{\text{START}}$. If POL = 0 the first pulse has the correct width. If POL = 1 (DIVCODE ≥ 8), the first pulse width can be shorter or longer than expected, depending on the duty cycle setting, and will never be less than 25% of $t_{\text{OUT}}$.

During start-up, the DIV pin A/D converter must determine the correct DIVCODE before the output is enabled. The start-up time may increase if the supply or DIV pin voltages are not stable. For this reason, it is recommended to minimize the capacitance on the DIV pin so it will properly track $V^\text{+}$. Less than 100pF will not affect performance.
Basic Operation

The simplest and most accurate method to program the LTC6992 is to use a single resistor, $R_{\text{SET}}$, between the SET and GND pins. The design procedure is a four step process. After choosing the proper LTC6992 version and POL bit setting, select the $N_{\text{DIV}}$ value and then calculate the value for the $R_{\text{SET}}$ resistor.

Alternatively, Linear Technology offers the easy to use TimerBlox Designer tool to quickly design any LTC6992 based circuit. Download the free TimerBlox Designer software at www.linear.com/timerblox.

Step 1: Selecting the POL Bit Setting

Most applications will use POL = 0, resulting in a positive transfer function. However, some applications may require a negative transfer function, where increasing $V_{\text{MOD}}$ reduces the output duty cycle. For example, if the LTC6992 is used in a feedback loop, POL = 1 may be required to achieve negative feedback.

Step 2: Selecting the LTC6992 Version

The difference between the LTC6992 versions is observed at the endpoints of the duty cycle control range. Applications that require the output to never stop oscillating should use the LTC6992-2. On the other hand, if the output should be allowed to rest at GND or $V^+$ (0% or 100% duty cycle), select the LTC6992-1.

The LTC6992-3 and LTC6992-4 clamp the duty cycle at only one end of the control range, allowing the output to stop oscillating at the other extreme. If POL = 1 the clamp will swap from low duty cycle to high, or vice-versa. Refer to Table 2 and Figure 4 for assistance in selecting the proper version.

Step 3: Selecting the $N_{\text{DIV}}$ Frequency Divider Value

As explained earlier, the voltage on the DIV pin sets the DIVCODE which determines both the POL bit and the $N_{\text{DIV}}$ value. For a given output frequency, $N_{\text{DIV}}$ should be selected to be within the following range.

$$62.5kHz \leq \frac{f_{\text{OUT}}}{N_{\text{DIV}}} \leq \frac{1MHz}{f_{\text{OUT}}}$$  \hspace{1cm} (1a)

To minimize supply current, choose the lowest $N_{\text{DIV}}$ value (generally recommended). For faster start-up or decreased jitter, choose a higher $N_{\text{DIV}}$ setting. Alternatively, use Table 1 as a guide to select the best $N_{\text{DIV}}$ value for the given application.

With POL already chosen, this completes the selection of DIVCODE. Use Table 1 to select the proper resistor divider or $V_{\text{DIV}}/V^+$ ratio to apply to the DIV pin.

Step 4: Calculate and Select $R_{\text{SET}}$

The final step is to calculate the correct value for $R_{\text{SET}}$ using the following equation.

$$R_{\text{SET}} = \frac{1MHz \cdot 50k}{N_{\text{DIV}} \cdot f_{\text{OUT}}}$$  \hspace{1cm} (1b)

Select the standard resistor value closest to the calculated value.

Example: Design a PWM circuit that satisfies the following requirements:

- $f_{\text{OUT}} = 20kHz$
- Positive $V_{\text{MOD}}$ to duty cycle response
- Output can reach 100% duty cycle, but not 0%
- Minimum power consumption

Step 1: Selecting the POL Bit Setting

For positive transfer function ($duty cycle increases with V_{\text{MOD}}$), choose POL = 0.

Step 2: Selecting the LTC6992 Version

To limit the minimum duty cycle, but allow the maximum duty cycle to reach 100%, choose LTC6992-4. (Note that if POL = 1 the LTC6992-3 would be the correct choice.)

Step 3: Selecting the $N_{\text{DIV}}$ Frequency Divider Value

Choose an $N_{\text{DIV}}$ value that meets the requirements of Equation (1a).

$$3.125 \leq N_{\text{DIV}} \leq 50$$

Potential settings for $N_{\text{DIV}}$ include 4 and 16. $N_{\text{DIV}} = 4$ is the best choice, as it minimizes supply current by us-
APPLICATIONS INFORMATION

-ing a large RSET resistor. POL = 0 and N_DIV = 4 requires DIVCODE = 1. Using Table 1, choose the R1 and R2 values to program DIVCODE = 1.

Step 4: Select RSET

Calculate the correct value for RSET using Equation (1b).

\[ R_{SET} = \frac{1\text{MHz} \cdot 50k}{4 \cdot 20kHz} = 625k \]

Since 625k is not available as a standard 1% resistor, substitute 619k if a 0.97% frequency shift is acceptable. Otherwise, select a parallel or series pair of resistors such as 309k and 316k to attain a more precise resistance.

The completed design is shown in Figure 7.

Figure 7. 20kHz PWM Oscillator

Duty Cycle Sensitivity to \( \Delta V_{SET} \)

The output duty cycle is proportional to the ratio of \( V_{MOD}/V_{SET} \). Since \( V_{SET} \) can vary up to \( \pm30mV \) from 1V it can effectively gain or attenuate \( V_{MOD} \), as shown below when \( \Delta V_{SET} \) is added to the equation.

\[ D = \frac{V_{MOD} - \Delta V_{SET}}{0.8 \cdot (V_{SET} + \Delta V_{SET})} = \frac{1}{8} \cdot \frac{1}{1 + \Delta V_{SET}/V_{SET}} \]

For many designs, the absolute \( V_{MOD} \) to duty cycle accuracy is not critical. For others, making the simplifying assumption of \( \Delta V_{SET} = 0V \) creates the potential for additional duty cycle error, which increases with \( V_{MOD} \), reaching a maximum of 3.4% if \( \Delta V_{SET} = -30mV \).

\[ \Delta D = -\frac{V_{MOD}}{800mV} \cdot \frac{\Delta V_{SET}}{V_{SET}} \equiv -\left( D_{IDEAL} + \frac{1}{8} \right) \cdot \frac{\Delta V_{SET}}{V_{SET}} \]

This error is in addition to the inherent PWM duty cycle accuracy spec \( \Delta D (\pm4.5\%) \), so care should be taken if accuracy at high duty cycles (\( V_{MOD} \) near 0.9V) is critical. Sensitivity to \( \Delta V_{SET} \) can be eliminated by making \( V_{MOD} \) proportional to \( V_{SET} \). For example, Figure 9 shows a simple circuit for generating an arbitrary duty cycle. The equation for duty cycle does not depend on \( V_{SET} \) at all.

Figure 8 demonstrates the worst-case impact of this variation (if \( V_{SET} \) is at its 0.97V or 1.03V limits).

Figure 8. Duty Cycle Variation Due to \( \Delta V_{SET} \)

Figure 9. Fixed-Frequency, Arbitrary Duty Cycle Oscillator
APPLICATIONS INFORMATION

I_{SET} Extremes (Master Oscillator Frequency Extremes)

When operating with I_{SET} outside of the recommended 1.25μA to 20μA range, the master oscillator operates outside of the 62.5kHz to 1MHz range in which it is most accurate.

The oscillator will still function with reduced accuracy for I_{SET} < 1.25μA. At approximately 500nA, the oscillator output will be frozen in its current state. The output could halt in a high or low state. This avoids introducing short pulses while frequency modulating a very low frequency output.

At the other extreme, it is not recommended to operate the master oscillator beyond 2MHz because the accuracy of the DIV pin ADC will suffer.

Pulse Width Modulation Bandwidth and Settling Time

The LTC6992 has a wide PWM bandwidth, making it suitable for a variety of feedback applications. Figure 10 shows that the frequency response is flat for modulation frequencies up to nearly 1/10 of the output frequency. Beyond that point, some peaking may occur (depending on N_{DIV} and average duty cycle setting).

Duty cycle settling time depends on the master oscillator frequency. Following a ±80mV step change in V_{MOD}, the duty cycle takes approximately eight master clock cycles (8 • t_{MASTER}) to settle to within 1% of the final value. Examples are shown in Figures 11a and 11b.

![Figure 10. PWM Frequency Response](image)

![Figure 11a. PWM Settling Time, 25% Duty Cycle](image)

![Figure 11b. PWM Settling Time, 50% Duty Cycle](image)
Power Supply Current

The power supply current varies with frequency, supply voltage and output loading. It can be estimated under any condition using the following equation:

If \( N_{DIV} = 1 \) (DIVCODE = 0 or 15):

\[
I_{S(TYP)} \approx V^+ \cdot f_{OUT} \cdot (39pF + C_{LOAD}) + \frac{V^+}{320k\Omega} \cdot \frac{V^+ \cdot \text{Duty Cycle}}{R_{LOAD}} + 2.2 \cdot I_{SET} + 85\mu A
\]

If \( N_{DIV} > 1 \) (DIVCODE = 1 or 14):

\[
I_{S(TYP)} \approx V^+ \cdot N_{DIV} \cdot f_{OUT} \cdot 27pF + \frac{V^+}{320k\Omega} \cdot \frac{V^+ \cdot \text{Duty Cycle}}{R_{LOAD}} + 2.6 \cdot I_{SET} + 90\mu A
\]

SUPPLY BYPASSING AND PCB LAYOUT GUIDELINES

The LTC6992 is a 2.4% accurate silicon oscillator when used in the appropriate manner. The part is simple to use and by following a few rules, the expected performance is easily achieved. Adequate supply bypassing and proper PCB layout are important to ensure this.

Figure 14 shows example PCB layouts for both the TSOT-23 and DFN packages using 0603 sized passive components. The layouts assume a two layer board with a ground plane layer beneath and around the LTC6992. These layouts are a guide and need not be followed exactly.

1. Connect the bypass capacitor, \( C1 \), directly to the \( V^+ \) and GND pins using a low inductance path. The connection from \( C1 \) to the \( V^+ \) pin is easily done directly on the top layer. For the DFN package, \( C1 \)’s connection to GND is also simply done on the top layer. For the TSOT-23, OUT can be routed through the \( C1 \) pads to allow a good \( C1 \) GND connection. If the PCB design rules do not allow that, \( C1 \)'s GND connection can be accomplished through multiple vias to the ground plane. Multiple vias for both the GND pin connection to the ground plane and the \( C1 \) connection to the ground plane are recommended to minimize the inductance. Capacitor \( C1 \) should be a 0.1\( \mu \)F ceramic capacitor.

2. Place all passive components on the top side of the board. This minimizes trace inductance.

3. Place \( R_{SET} \) as close as possible to the SET pin and make a direct, short connection. The SET pin is a current summing node and currents injected into this pin directly modulate the operating frequency. Having a short connection minimizes the exposure to signal pickup.

4. Connect \( R_{SET} \) directly to the GND pin. Using a long path or vias to the ground plane will not have a significant affect on accuracy, but a direct, short connection is recommended and easy to apply.

5. Use a ground trace to shield the SET pin. This provides another layer of protection from radiated signals.

6. Place \( R1 \) and \( R2 \) close to the DIV pin. A direct, short connection to the DIV pin minimizes the external signal coupling.
**APPLICATIONS INFORMATION**

Figure 14. Supply Bypassing and PCB Layout

**TYPICAL APPLICATIONS**

Constant On-Time Modulator

\[ V_{MOD} \]

\[ V_{IN} \]

\[ 0 \text{V TO 2V} \]

\[ R_{M1} = 1.05k \]

\[ R_{M2} = 9.31k \]

\[ R_{SET} = 44.2k \]

\[ V_{CTRL} \]

\[ C1 = 0.1\mu F \]

\[ R1 = 182k \] (÷16, POL = 1)

\[ R2 = 976k \]

\[ C1 = 0.1\mu F \]

\[ R2 = 976k \]

\[ V_{CC} \]

\[ 122k \] (DIVCODE = 2 (16, POL = 1))

\[ V^{+} \]

\[ V_{SET} \]

\[ 4.42 \text{kΩ} \]

\[ 0.1\mu F \]

\[ 0.1\mu F \]

\[ 0.1\mu F \]

*OPTIONAL RESISTOR ADJUSTS FOR DESIRED VIN RANGE.

"IF \[ \frac{R_{M2}}{R_{M1} + R_{M2}} \] = 0.9 THEN \[ I_{ON} = \frac{N_{DIV} \times 1.125\mu s \times R_{SET}}{50k} \]

AS \[ V_{IN} \] INCREASES, \[ V_{OUT} \] INCREASES AND DUTY CYCLE DECREASES (BECAUSE POL = 1) TO MAINTAIN A CONSTANT \[ I_{ON} \].

FOR CONSTANT OFF-TIME, JUST CHANGE DIVCODE SO POL = 0."
Digitally Controlled Duty Cycle with Internal $V_{\text{REF}}$ Reference Variation Eliminated

**Programming $N_{\text{DIV}}$ Using an 8-Bit DAC**
TYPICAL APPLICATIONS

Changing Between Two Frequencies

NOTES
1. WHEN THE NMOSFET IS OFF, THE FREQUENCY IS SET BY \( R_{SET} = R_{SET1} \).
2. WHEN THE NMOSFET IS ON, THE FREQUENCY IS SET BY \( R_{SET} = R_{SET1} || R_{SET2} \).
3. \( V^+ \) SUPPLY VARIATION IS NOT A FACTOR AS THE SWITCHING RESISTOR IS EITHER FLOATING OR CONNECTED TO GROUND.

Simple Diode Temperature Sensor

NOTES
1. ADJUST FOR 50% DUTY CYCLE AT 25°C
2. PWM OUTPUT FOR ISOLATED MEASUREMENT
   - +1% DUTY CYCLE CHANGE PER DEGREE C
   - -10°C TO 65°C RANGE WITH OPTO-ISOLATOR (DC: 15% TO 95%)
Motor Speed/Direction Control for Full H-Bridge (Locked Anti-Phase Drive)

2.6kHz, 5% TO 95% PWM
5% DC = CLOCKWISE
50% DC = STOPPED
95% DC = COUNTER CLOCKWISE

Motor Speed/Direction Control for Full H-Bridge (Sign/Magnitude Drive)

2.6kHz, 5% TO 95% PWM
5% DC = SLOW
95% DC = FAST

DIRECTION
H = CCW, L = CW
TYPICAL APPLICATIONS

Ratiometric Sensor to Pulse Width, Non-Inverting Response

Ratiometric Sensor to Pulse Width, Inverting Response
TYPICAL APPLICATIONS

Radio Control Servo Pulse Generator

Direct Voltage Controlled PWM Dimming (0 to 15000 Cd/m² Intensity)
TYPICAL APPLICATIONS

Wide Range LED Dimming (0 to 85000 Cd/m² Brightness)

FAST PWM CONTROLS 6000 TO 85000 Cd/m² BRIGHTNESS

SLOW PWM CONTROLS 0 TO 8000 Cd/m² BRIGHTNESS

R1 10k
R2 7.5k
R3 10k
RSET1 61.9k
RSET2 124k

VFAST
VREF

VDIMMING 0V TO 1.65V
V1

MOD OUT
LTC6992-4
GND V+
SET DIV

5V 0.1µF

DIV

R1 10k

5V 0.1µF

GND

5V 0.1µF

V1

MOD OUT
LTC6992-1
GND V+
SET DIV

5V 0.1µF

GND

5V 0.1µF

V1

A1

PWM
LT3518UF

3.3V 5V

3.3VIN PVIN

D1
D2

33 VIN PV IN

LUMILEDS LXML-BW02

5–100%
NDIV = 64
f = 12.6kHz

0–100%
NDIV = 4096
fOUT = 100Hz

0.1µF

0.1µF

0.1µF
Isolated PWM (5% to 95%) Controller

CONCEPT DESIGN USING SIMPLE R-C FILTERING FOR PWM CONTROL. NOT OPTIMIZED FOR OFFSETS.

T1: PCA EPF8119S ETHERNET TRANSFORMER
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DCB Package
6-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1715 Rev A)

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.
LTC6992-1/LTC6992-2/
LTC6992-3/LTC6992-4

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636 Rev B)

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193
## REVISION HISTORY

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<td>01/11</td>
<td>Revised $\theta_{JA}$ value for TSOT package in the Pin Configuration.</td>
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<td>Added Note 7 for $V_{OH}$ and $V_{OL}$ in the Electrical Characteristics table.</td>
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<td>Minor edit to the Block Diagram.</td>
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<td>Minor edit to the equation in the “Duty Cycle Sensitivity to $\Delta V_{SET}$” section.</td>
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<td>B</td>
<td>07/11</td>
<td>Revised Description and Order Information sections</td>
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<td>Added additional information to $f_{OUT}/\Delta V$ and included Note 11 in Electrical Characteristics section</td>
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<td>Added Typical Frequency Error vs Time curve to Typical Performance Characteristics section</td>
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<td>Added text to Basic Operation paragraph in Applications Information section</td>
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<td>Corrected $f_{OUT}$ value in Typical Applications drawing 6692 TA13</td>
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<tr>
<td>C</td>
<td>01/12</td>
<td>Added MP-Grade</td>
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### RELATED PARTS

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<tr>
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<th>DESCRIPTION</th>
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<td>LTC1799</td>
<td>1MHz to 33MHz ThinSOT Silicon Oscillator</td>
<td>Wide Frequency Range</td>
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<tr>
<td>LTC6900</td>
<td>1MHz to 20MHz ThinSOT Silicon Oscillator</td>
<td>Low Power, Wide Frequency Range</td>
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<tr>
<td>LTC6906/LTC6907</td>
<td>10kHz to 1MHz or 40kHz ThinSOT Silicon Oscillator</td>
<td>Micropower, ( I_{\text{SUPPLY}} = 35\mu A ) at 400kHz</td>
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<tr>
<td>LTC6930</td>
<td>Fixed Frequency Oscillator, 32.768kHz to 8.192MHz</td>
<td>0.09% Accuracy, 110(\mu)s Start-Up Time, 105(\mu)A at 32kHz</td>
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<td>LTC6990</td>
<td>TimerBlox, Voltage Controlled Oscillator</td>
<td>Frequency from 488Hz to 1MHz, No Caps, 2.2% Accurate</td>
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<tr>
<td>LTC6991</td>
<td>TimerBlox, Very Low Frequency Clock with Reset</td>
<td>Cycle Time from 2ms to 9.5 Hours, No Caps, 2.2% Accurate</td>
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<td>LTC6993</td>
<td>TimerBlox, Monostable Pulse Generator</td>
<td>Resistor Set Pulse Width from 1(\mu)s to 34sec, No Caps, 3% Accurate</td>
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<td>LTC6994</td>
<td>TimerBlox, Delay Block/Debouncer</td>
<td>Resistor Set Delay from 1(\mu)s to 34sec, No Caps Required, 3% Accurate</td>
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C1: KEMET C0806C225K4RAC  
C2: KEMET C1206C475K3RAC  
C3, C4: MURATA GRM21BR71H104KA01B  
C5: MURATA GRM21BR71H224KA01B  
D1: DIODE DFLS160  
L1: TOKO B992AS-6R8N  
LEDS: LUXEON I (WHITE)  
M1: ZETEX ZXMP6A13FTA