REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	08/01/11
A	**PAGE 10, REVISED CONDITIONS FOR A_{VOL} IN TABLE I – PARAMETER CONDITIONS: <u>FROM</u> V_S = ±5V; R_L = 100Ω; V_{OUT} = ±4.5V <u>TO</u> V_S = ±5V; R_L = 100Ω; V_{OUT} = ±2V**	

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12					
INDEX	REVISION	**A**	**A**	**A**	**A**	**A**	**A**	**A**	**A**	**A**	**A**	**A**	**A**					
REVISION	PAGE NO.																	
INDEX	REVISION																	

				LINEAR TECHNOLOGY CORPORATION MILPITAS, CALIFORNIA			
	ORIG			TITLE:			
	DSGN			**MICROCIRCUIT, LINEAR, RH6200M LOW NOISE, HIGH SPEED RAIL-TO-RAIL OP AMP**			
	ENGR						
	MFG						
	CM						
	QA			SIZE	CAGE CODE	DRAWING NUMBER	REV
	PROG				**64155**	**05-08-5249**	**A**
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:			

FOR OFFICIAL USE ONLY

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-STD-883	Test Method and Procedures for Microcircuits
MIL-STD-1835	Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH6200M, Low Noise, High Speed Rail-to-Rail Op Amp, processed to space level manufacturing flow.

3.2 Part Number:

3.2.1 RH6200MW (CERPAC, 10 LEADS)

3.3 Part Marking Includes:

a. LTC Logo

b. LTC Part Number (See Paragraph 3.2)

c. Date Code

d. Serial Number

e. ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings: All notes are on page 11.
(Note 1)

Total Supply Voltage (V^+ to V^-)	12.6V
Input Current (Note 2)	±40mA
Output Short-Circuit Duration (Note 3)	Indefinite
Pin Current While Exceeding Supplies (Note 4)	±30mA
Operating Junction Temperature Range (Note 5)	-55˚C to 125˚C
Storage Temperature Range	-65˚C to 150˚C
Lead Temperature (Soldering, 10 sec)	300˚C

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 1C.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in **Table I** and **Table II.**

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in **Table IV** herein.

3.8 Burn-In Requirement:

3.8.1 Cerpac (W) **Static Burn-in, Figure 4**.

3.8.2 Cerpac (W): **Dynamic Burn-In, Figure 5**.

3.9 Delta Limit Requirement: Delta limit parameters are specified in **Table III** herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with **Figure 1**.

Terminal Connections: The terminal connections shall be as specified in **Figure 2**.

3.10.2 Lead Material and Finish: The lead material and finish for device shall be Alloy 42 and the lead finish is hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

3.11 Radiation Hardness Assurance (RHA):

3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.11.3 Total dose bias circuit is specified in **Figure 3**.

3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.

3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS):

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1, and 3.4 of the test method. Electrical testing shall be as specified in Table IV herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in Table IV herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroups 1-4 plus 6 are performed on every assembly lot, and Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1

Group B, Subgroup 2c = 10%	Group B, Subgroup 5 = *5% (*per wafer or inspection lot whichever is the larger quantity)
Group B, Subgroup 3 = 10%	
Group B, Subgroup 4 = 5%	Group B, subgroup 6 = 15%

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Source Inspection:

4.5.1 The manufacturer will coordinate Source Inspection at wafer lot acceptance and pre-seal internal visual.

4.5.2 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance and final data review.

4.6 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.6.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.6.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.6.3 Burn-In Variables Data and Deltas (if applicable)

4.6.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.6.5 Generic Group D data (4.4.3 herein)

4.6.6 SEM photographs (3.13 herein)

4.6.7 Wafer Lot Acceptance Report (3.13 herein)

4.6.8 X-Ray Negatives and Radiographic Report

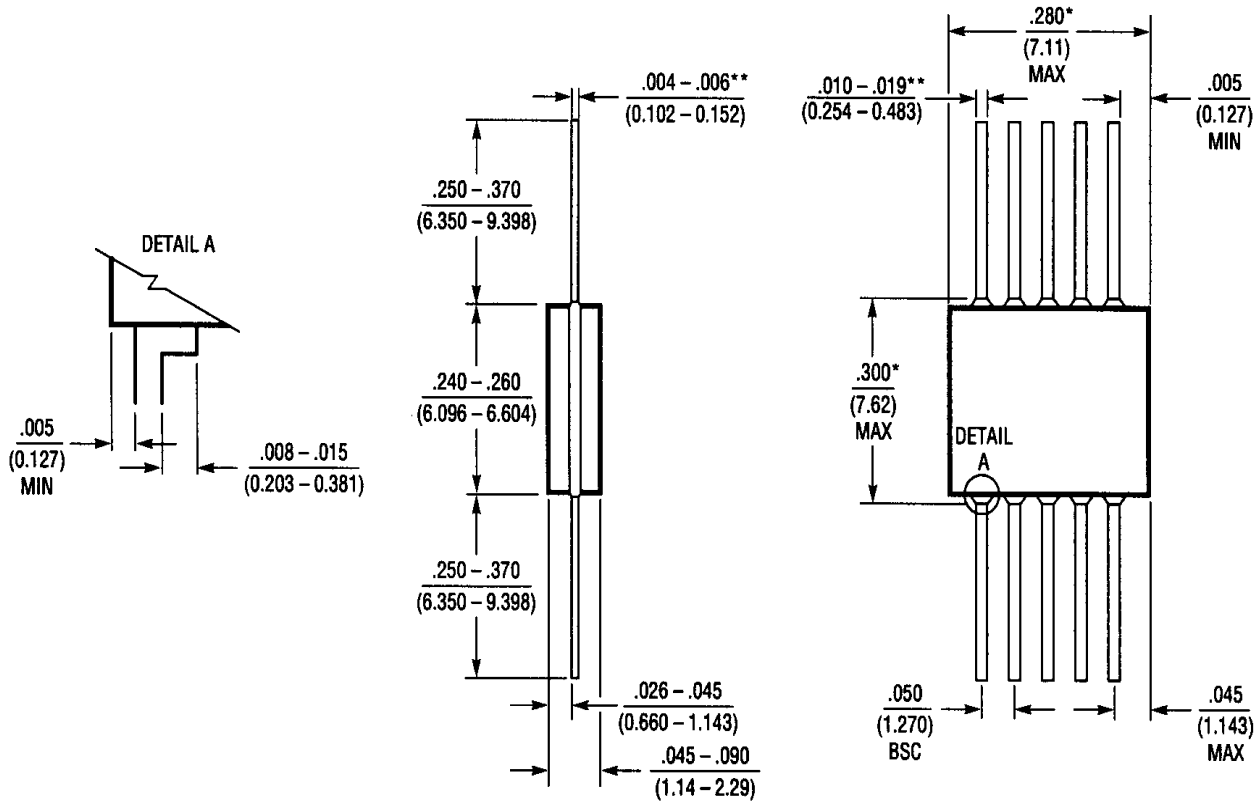
4.6.9 A copy of outside test laboratory radiation report if ordered

4.6.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 4.6.1 and 4.6.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as "No Charge Data".

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

(W) CERPAC, 10 LEAD CASE OUTLINE



NOTES:
*THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN
**INCREASE DIMENSIONS BY 0.003 INCHES (0.076 mm) WHEN LEAD FINISH A IS APPLIED (SOLDER DIPPED)

θja = +170°C / W
θjc = +40°C / W

FIGURE 1

(W) CERPAC, 10 LEAD TERMINAL CONNECTIONS

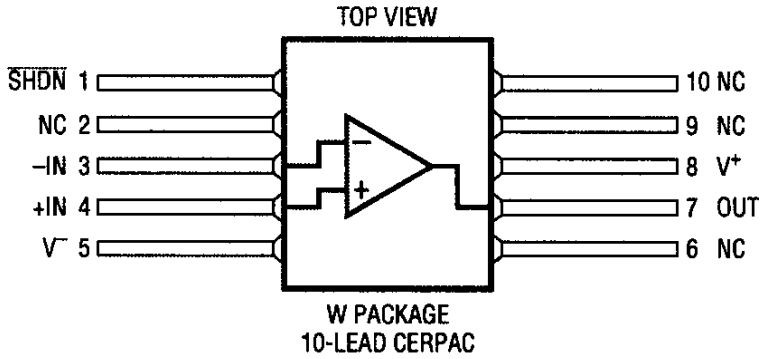
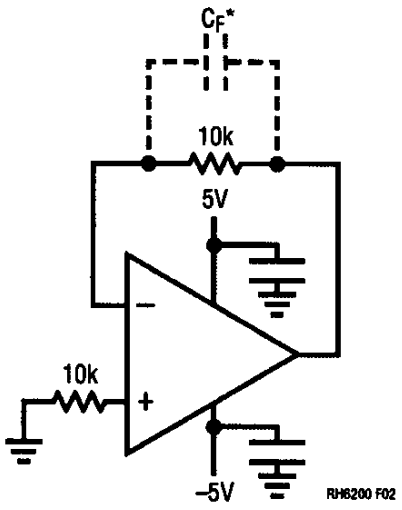


FIGURE 2

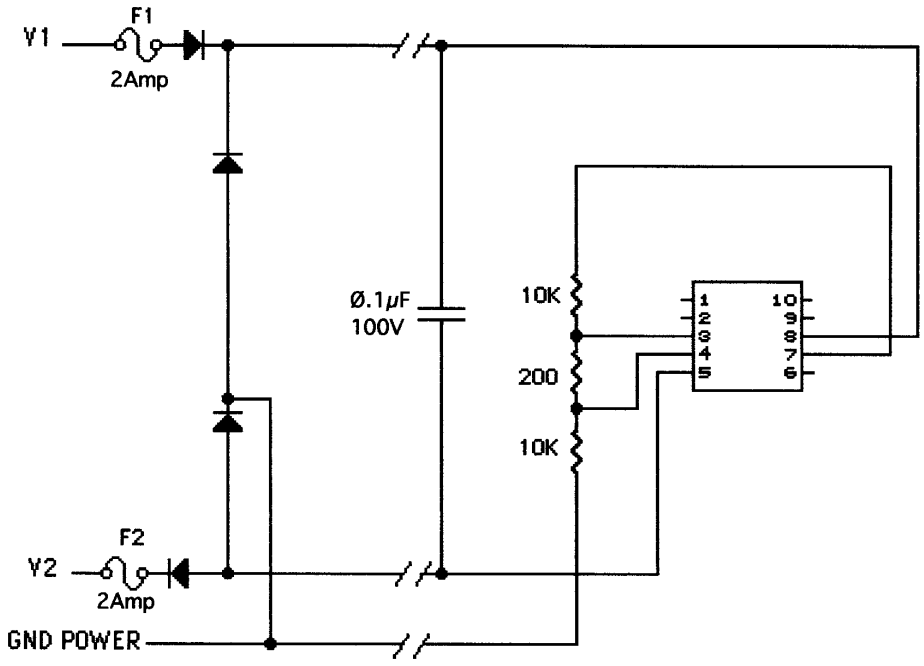
TOTAL DOSE BIAS CIRCUIT



*C_F IS COMPONENT OR PARASITIC CAPACITANCE ENSURING STABILITY

FIGURE 3

(W) CERPAC, 10 LEAD STATIC BURN-IN CIRCUIT



1. Unless otherwise specified, component tolerances shall be per military specification.
2. Ta = +90 ° C .
3. Tj = + 157° C maximum.
4. Tc = + 132° C minimum.
5. Diodes to be 1N5550.
6. Device current = 27mA.
7. Burn-in Voltages: V1 = +6.0V to +6.3V
   V2 = -6.0V to -6.3V

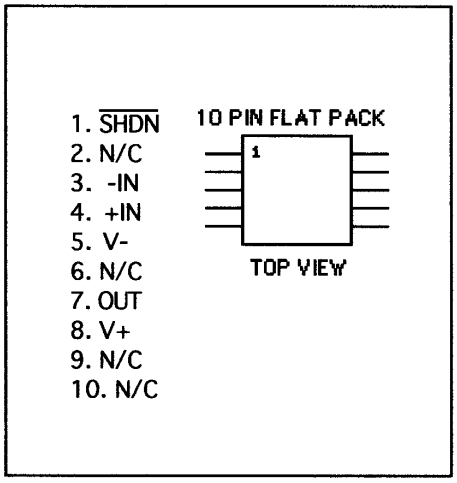
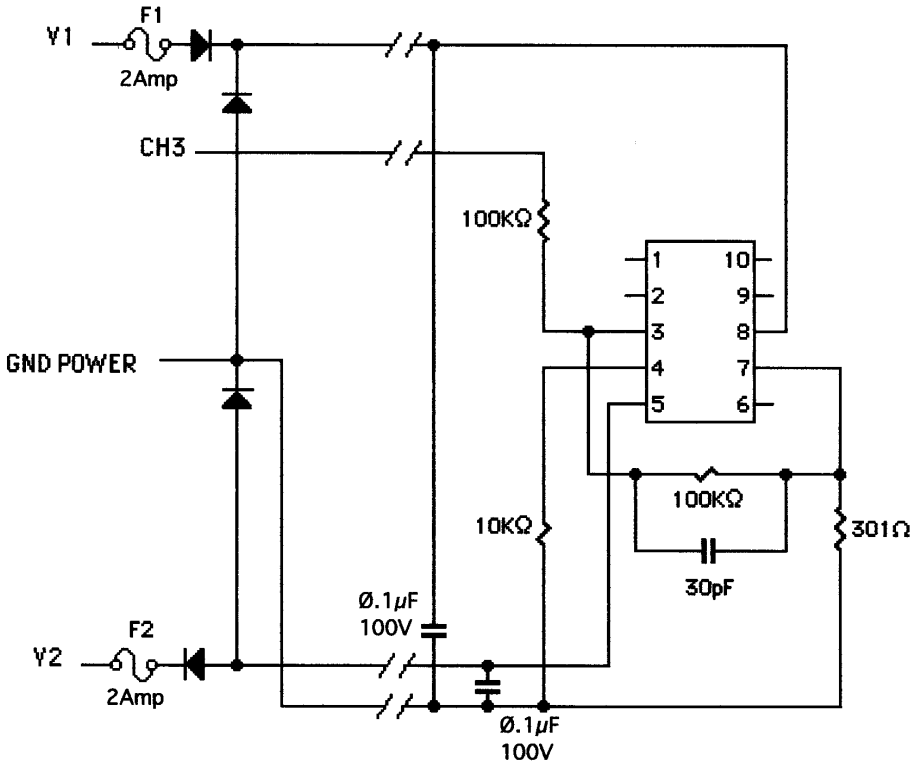
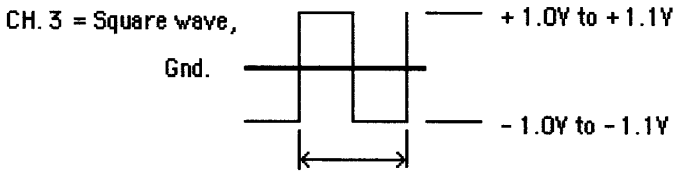


FIGURE 4

(W) CERPAC, 10 LEAD DYNAMIC BURN-IN CIRCUIT



1. Unless otherwise specified, component tolerances shall be per military specification.
2. Ta = +90 ° C .
3. Tj = + 157° C maximum.
4. Tc = + 132° C minimum.
5. Diodes to be 1N5550.
6. Device current = 27mA.
7. Burn-in Voltages: V1 = +6.0V to +6.3V
   V2 = -6.0V to -6.3V



Frequency, 4.5hz(222ms) to 5.5hz(182ms)

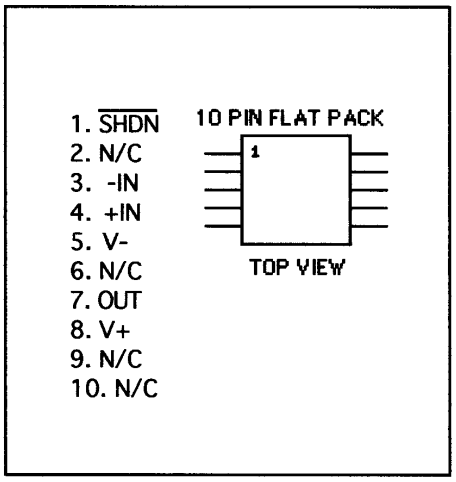


FIGURE 5

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION)

SYMBOL	PARAMETER	CONDITIONS	NOTES	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	SUB-GROUP	−55°C ≤ T_A ≤ 125°C MIN	−55°C ≤ T_A ≤ 125°C TYP	−55°C ≤ T_A ≤ 125°C MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage	V_S = 5V, 0V; V_{CM} = V^- to V^+			0.6	2	1			4	2,3	mV
		V_S = ±5V; V_{CM} = V^- to V^+			2.5	6	1			9	2,3	mV
I_B	Input Bias Current	V_S = 5V, 0V; V_{CM} = V^+			8	18	1			20	2,3	µA
		V_S = 5V, 0V; V_{CM} = V^-		−50	−23		1	−100			2,3	µA
		V_S = ±5V; V_{CM} = V^+			8	18	1			20	2,3	µA
		V_S = ±5V; V_{CM} = V^-		−50	−23		1	−200			2,3	µA
I_{OS}	Input Offset Current	V_S = 5V, 0V; V_{CM} = V^+			0.02	4	1			5	2,3	µA
		V_S = 5V, 0V; V_{CM} = V^-			0.4	5	1			25	2,3	µA
		V_S = ±5V; V_{CM} = V^+			1	7	1			12	2,3	µA
		V_S = ±5V; V_{CM} = V^-			3	12	1			50	2,3	µA
	Input Noise Voltage	0.1Hz to 10Hz	6		600							nV_{P-P}
e_n	Input Noise Voltage Density	V_S = 5V, 0V; f = 100kHz	6		1.1							nV/√Hz
		V_S = 5V, 0V; f = 10kHz			1.5	2.4						nV/√Hz
		V_S = ±5V; f = 100kHz	6		0.95							nV/√Hz
		V_S = ±5V; f = 10kHz			1.4	2.3						nV/√Hz
i_n	Input Noise Current Density	f = 10kHz Balanced Source	6		2.2							pA/√Hz
		f = 10kHz Unbalanced Source	6		3.5							pA/√Hz
A_{VOL}	Large Signal Open-Loop Voltage Gain	V_S = 5V, 0V; R_L = 1k; V_{OUT} = 0.5V to 4.5V		70	120		4	35			5,6	V/mV
		V_S = 5V, 0V; R_L = 100Ω; V_{OUT} = 1V to 4V		11	18		4					V/mV
		V_S = 5V, 0V; R_L = 100Ω; V_{OUT} = 1.5V to 3.5V						5.5			5,6	V/mV
		V_S = ±5V; R_L = 1k; V_{OUT} = ±4.5V		115	200		4	40			5,6	V/mV
		V_S = ±5V; R_L = 100Ω; V_{OUT} = ±2V		15	26		4	7			5,6	
CMRR	Common Mode Rejection Ratio	V_S = 5V, 0V; V_{CM} = 0V to 5V		65	90		1	58			2,3	dB
		V_S = 5V, 0V; V_{CM} = 1.5V to 3.5V		85	112		1	76			2,3	dB
		V_S = ±5V; V_{CM} = ±5V		68	96		1	63			2,3	dB
		V_S = ±5V; V_{CM} = ±2V		75	100		1	72			2,3	dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V		60	68		1	58			2,3	dB
V_{OL}	Output Voltage Swing Low	V_S = 5V, 0V; I_L = 0			9	50	4			100	5,6	mV
		V_S = 5V, 0V; I_L = 5mA			50	100	4			150	5,6	mV
		V_S = 5V, 0V; I_L = 20mA			150	290	4			350	5,6	mV
		V_S = ±5V; I_L = 0			12	50	4			100	5,6	mV
		V_S = ±5V; I_L = 5mA			55	110	4			150	5,6	mV
		V_S = ±5V; I_L = 20mA			150	290	4			350	5,6	mV
V_{OH}	Output Voltage Swing High	V_S = 5V, 0V; I_L = 0			55	110	4			150	5,6	mV
		V_S = 5V, 0V; I_L = 5mA			95	190	4			250	5,6	mV
		V_S = 5V, 0V; I_L = 20mA			220	400	4			500	5,6	mV
		V_S = ±5V; I_L = 0			70	130	4			200	5,6	mV
		V_S = ±5V; I_L = 5mA			110	210	4			275	5,6	mV
		V_S = ±5V; I_L = 20mA			225	420	4			550	5,6	mV
I_{SC}	Short-Circuit Current	V_S = 5V, 0V or V_S = ±5V		±60	±90		1	±45			2,3	mA
I_S	Supply Current	V_S = 5V, 0V			16.5	20	1			30	2,3	mA
		V_S = ±5V			20	23	1			35	2,3	mA
$I_{S(SHDN)}$	Shutdown Supply Current	V_S = 5V, 0V			1.3	1.8	1			2.2	2,3	mA
		V_S = ±5V			1.6	2.1	1			2.5	2,3	mA
I_{SHDN}	Shutdown Pin Current	V_S = 5V, 0V or V_S = ±5V; V_{SHDN} = 0.3V		−280	−200		1	−300			2,3	µA
t_{ON}	Turn-On Time	$\overline{SHDN}$ from Low to High	6		180							ns
t_{OFF}	Turn-On Time	$\overline{SHDN}$ from High to Low	6		180							ns
GBW	Gain Bandwidth Product	V_S = 5V, 0V; at f = 1MHz	6		145							MHz
		V_S = ±5V; at f = 1MHz		110	165							MHz
SR	Slew Rate	V_S = 5V, 0V; A_V = −1; R_L = 1k; V_O = 4V		31	44		4					V/µs
		V_S = ±5V; A_V = −1, R_L = 1k; V_O = 4V		35	50		4					V/µs

NOTES ON NEXT PAGE

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION)

T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	10KRAD(Si) MIN	10KRAD(Si) MAX	20KRAD(Si) MIN	20KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	200KRAD(Si) MIN	200KRAD(Si) MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = 5V, 0V; V_{CM} = V^- to V^+		2.2		2.4		2.6		2.8		3	mV
		V_S = ±5V; V_{CM} = V^- to V^+		6.5		7		7.5		8		8.5	mV
I_B	Input Bias Current	V_S = 5V, 0V, V_{CM} = V^+		20		22		24		26		28	µA
		V_S = 5V, 0V, V_{CM} = V^-	–55		–60		–65		–70		–75		µA
		V_S = ±5V, V_{CM} = V^+		20		22		24		26		28	µA
		V_S = ±5V, V_{CM} = V^-	–55		–60		–65		–70		–75		µA
I_{OS}	Input Offset Current	V_S = 5V, 0V; V_{CM} = V^+		5		6		7		8		9	µA
		V_S = 5V, 0V; V_{CM} = V^-		6		7		8		9		10	µA
		V_S = ±5V; V_{CM} = V^+		8		9		10		11		12	µA
		V_S = ±5V; V_{CM} = V^-		13		14		15		16		17	µA
A_{VOL}	Large Signal Open Loop Voltage Gain	V_S = 5V, 0V; R_L = 1k; V_{OUT} = 0.5V to 4.5V	65		60		55		50		45		V/mV
		V_S = 5V, 0V; R_L = 100Ω; V_{OUT} = 1V to 4V	10		9		8		7		6		V/mV
		V_S = ±5V; R_L = 1k; V_{OUT} = ±4.5V	110		100		90		80		70		V/mV
		V_S = ±5V; R_L = 100Ω; V_{OUT} = ±2V	13.5		12		10.5		9		7.5		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, 0V; V_{CM} = 0V to 5V	64		63		62		61		60		dB
		V_S = 5V, 0V; V_{CM} = 1.5V to 3.5V	84		83		82		81		80		dB
		V_S = ±5V; V_{CM} = ±5V	67		66		65		64		63		dB
		V_S = ±5V; V_{CM} = ±2V	74		73		72		71		70		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V	59		58		57		56		55		dB
V_{OL}	Output Voltage Swing Low	V_S = 5V, 0V; I_L = 0		52		54		56		58		60	mV
		V_S = 5V, 0V; I_L = 5mA		104		108		112		116		120	mV
		V_S = 5V, 0V; I_L = 20mA		296		302		308		314		320	mV
		V_S = ±5V; I_L = 0		52		54		56		58		60	mV
		V_S = ±5V; I_L = 5mA		114		118		122		126		130	mV
		V_S = ±5V; I_L = 20mA		296		302		308		314		320	mV
V_{OH}	Output Voltage Swing High	V_S = 5V, 0V; I_L = 0		114		118		122		126		130	mV
		V_S = 5V, 0V; I_L = 5mA		198		206		214		222		230	mV
		V_S = 5V, 0V; I_L = 20mA		415		430		445		460		475	mV
		V_S = ±5V; I_L = 0		134		138		142		146		150	mV
		V_S = ±5V; I_L = 5mA		218		226		234		242		250	mV
		V_S = ±5V; I_L = 20mA		430		455		470		485		500	mV
I_{SC}	Short-Circuit Current	V_S = 5V, 0V or V_S = ±5V		58		56		54		52		50	mA
I_S	Supply Current	V_S = 5V, 0V		20.4		20.8		21.2		21.6		22	mA
		V_S = ±5V		23.4		23.8		24.2		24.6		25	mA
$I_{S(SHDN)}$	Shutdown Supply Current	V_S = 5V, 0V		1.84		1.88		1.92		1.96		2	mA
		V_S = ±5V		2.14		2.18		2.22		2.26		2.3	mA
I_{SHDN}	Shutdown Pin Current	V_S = 5V, 0V or V_S = ±5V; V_{SHDN} = 0.3V		–284		–288		–292		–296		–300	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Inputs are protected by back-to-back diodes. If the differential input voltage exceeds 0.7V, the input current must be limited to less than 40mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: There are reverse-biased ESD diodes from all inputs and outputs to the respective supply pins. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient in nature and limited to less than 30mA, no damage to the device will occur.

Note 5: The RH6200 is tested under pulse load conditions such that $T_J \approx T_A$. The thermal resistance of the W 10-lead CERPAC package (without heat sink) is estimated at 170°C/W. For a given application, multiply the RMS power dissipation of the RH6200 times the package thermal resistance (including any heat sinking if present) to calculate the temperature difference between the ambient temperature and the junction temperature. The RH6200 has a thermal shutdown feature that protects the part from excessive junction temperature. The amplifier will shut down to an inactive, low current condition when the junction temperature exceeds approximately 160°C. The amplifier will remain shut down until the die cools off to below approximately 150°C, at which point the amplifier will return to normal operation.

Note 6: This parameter is not production tested. Typical bench evaluation performance listed for information only.

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

Test Condition: T_A = 25°C, V_S = ±5V, V_{CM} = +5V

	ENDPOINT LIMIT		DELTA		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
V_{OS}	-6	6	-2	2	mV
$+I_B$	0	18	-4	4	µA
$-I_B$	0	18	-4	4	µA
I_{OS}	-7	7	-2	2	µA

Test Condition: T_A = 25°C, V_S = ±5V, V_{CM} = -5V

	ENDPOINT LIMIT		DELTA		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
V_{OS}	-6	6	-2	2	mV
$+I_B$	-50	0	-8	8	µA
$-I_B$	-50	0	-8	8	µA
I_{OS}	-12	12	-4	4	µA

Test Condition: T_A = 25°C, V_S = +5V, V_{CM} = +5V

	ENDPOINT LIMIT		DELTA		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
V_{OS}	-2	2	-0.8	0.8	mV
$+I_B$	0	18	-4	4	µA
$-I_B$	0	18	-4	4	µA
I_{OS}	-4	4	-2	2	µA

Test Condition: T_A = 25°C, V_S = +5V, V_{CM} = 0V

	ENDPOINT LIMIT		DELTA		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
V_{OS}	-2	2	-0.8	0.8	mV
$+I_B$	-50	0	-8	8	µA
$-I_B$	-50	0	-8	8	µA
I_{OS}	-5	5	-2	2	µA

TABLE IV: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
FINAL ELECTRICAL TEST REQUIREMENTS (METHOD 5004)	1*, 2, 3,4,5,6
GROUP A TEST REQUIREMENTS (METHOD 5005)	1, 2, 3,4,5,6
GROUP B AND D FOR CLASS S ENDPOINT ELECTRICAL PARAMETERS (METHOD 5005)	1, 2, 3

*PDA APPLIES TO SUBGROUP 1.

PDA TEST NOTE: The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1 and delta rejects after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

LINEAR TECHNOLOGY CORPORATION RESERVES THE RIGHT TO TEST TO TIGHTER LIMITS THAN THOSE GIVEN.