REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	04/25/06
A	REMOVED NOTE #5 FROM TITLE TABLE II ELECTRICAL CHARACTERISTICS - POST-IRRADIATION, VS=5V, 3V, 50 Krads, IB, from 809 to 800 nA, PAGE 13 OF 14.	01/09/08
B	• PAGE 3, PARAGRAPH 3.7.1 CHANGED VERBIAGE.	05/06/08
C	• PAGE 12, AMENDED DICE/DWF ELECTRICAL TEST LIMITS (PRE-IRRADIATION) IB CURRENT MATCH (CHANNEL-TO-CHANNEL) MAX. • PAGE 14, CHANGED RH CANNED SAMPLE TABLE III FOR QUALIFYING DICE SALES ADDED TEMPERATURE CYCLE, CONSTANT ACCELERATION & REMOVED PIND TEST.	02/26/09
D	• PAGE 11, AMENDED DICE/DWF ELECTRICAL TEST LIMITS (PRE-IRRADIATION) IB CURRENT MATCH (CHANNEL-TO-CHANNEL) MAX FROM 120 nA TO 200 nA. • PAGE 12, AMENDED DICE/DWF ELECTRICAL TEST LIMITS (PRE-IRRADIATION), V_S = 3V,, 5V; V_{OUT} = HALF SUPPLY, I_{CS} MIN CHANGED FROM ±15mA TO ± 12mA IB CURRENT MATCH (CHANNEL-TO-CHANNEL) MAX FROM 100 nA TO 180 nA. • PAGE 13, TABLE II, CORRECTED TYPO IN THE V_{OUT}, OUTPUT VOLTAGE SWING HIGH CONDITION FROM I_{SINK} = 1Ma AND I_{SINK} = 2.5 mA TO I_{SOURCE} = 1mA AND I_{SOURCE} = 2.5mA.	9/24/09
E	• PAGE 12, TABLE II, ELECTRICAL CHARACTERISTICS, (PRE-IRRADIATION) V_S= 3V, 5V, DELETED 3V. PARAMETER A_{VOL}, DELETED V_S = 3V, V_O = 75mV TO 2.8V, R_1 = 10k. PARAMETER CMRR, COMMON MODE REJECTION RATIO - DELETED V_S = 3V, V_{CM} = V^+ TO V^- PARAMETER CMRR, MATCH (CHANNEL-TO-CHANNEL) - DELETED V_S = 3V, V_{CM} = V^+ TO V^-. PARAMETER PSSR, POWER SUPPLY REJECTION RATIO, REPLACED V_S =2.2V TO12 WITH V_S = 4.5V TO 12V; V_{CM}=V_{OUT}=0.5V. PARAMETER PSSR, MATCH (CHANNEL-TO-CHANNEL, DELETED REPLACED V_S =2V TO 16 WITH V_S = 4.5V TO 12V; V_{CM}=V_{OUT}=0.5V. • PAGE 13, TABLE IIA, ELECTRICAL CHARACTERISTICS, (PRE-IRRADIATION) V_S= 3V, 5V, DELETED 3V.	02/25/10
F	Page 2, amended section 3.3 Special Handling of Dice to more accurately describe our current procedures and requirements.	04/05/12

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
INDEX	REVISION	**G**	**G**	**G**	**G**	**G**	**G**	**G**	**G**	**G**	**G**	**G**	**G**	**G**	**G**	**G**	
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				LINEAR TECHNOLOGY CORPORATION MILPITAS, CALIFORNIA			
	ORIG			TITLE:			
	DSGN			**Microcircuit, Linear, RH1498, 10MHz, 6V /µs Rail-to-Rail Input And Output Precision C-Load Op Amp Dice**			
	ENGR						
	MFG						
	CM						
	QA			SIZE	CAGE CODE	DRAWING NUMBER	REV
	PROG				**64155**	**05-08-5208**	**G**
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:			

FOR OFFICIAL USE ONLY

REVISION RECORD		
REV	DESCRIPTION	DATE
G	**Page 15, Changed RH Canned Sample Table for Qualifying Dice Sales: Subgroup 6 Sample Size Series changed from 45 (3) to 65 (3). First note had the Sample Size Series from "15%" to "10%".**	**7/2/13**

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1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-STD-883	Test Method and Procedures for Microcircuits
MIL-STD-1835	Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH1498MW, 10MHz, 6V /µs Rail-toRail Input and Output precision C-load Op Amp Dice and Element Evaluation Test Samples, processed to space level manufacturing flow as specified herein.

3.2 Part Number: **RH1498 Dice**

3.3 **Special Handling of Dice:** Rad Hard dice require special handling as compared to standard IC dice. Rad Hard dice are susceptible to surface damage due to the absence of silicon nitride passivation that is present on most standard dice. Silicon nitride protects the dice surface from scratches by its hard and dense properties. The passivation on Linear Technology's Rad Hard dice is silicon dioxide which is much "softer" than silicon nitride. During the visual and preparation for shipment, ESD safe Tweezers are used and only the edges of the die are touched.

LTC recommends that dice handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die in or out of the chip shipment tray (waffle pack), use an ESD-Safe-Plastic-tipped Bent Metal Vacuum Probe, preferably .020" OD x .010" ID (for use with tiny parts). The wand should be compatible with continuous air vacuums. The tip material should be static dissipative Delrin (or equivalent) plastic.

During die attach, care must be exercised to ensure no tweezers, or other equipment, touch the top of the dice.

3.4 The Absolute Maximum Ratings:

(Note 1)

Total Supply Voltage (V^+ to V^-)	36V
Input Current	±10mA
Output Short-Circuit Duration **(Note 2)**	Continuous
Operating Temperature Range	-55°C to 125°C
Specified Temperature Range	-55°C to 125°C
Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (soldering, 10 sec.)	300°C

Note #1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note #2: A heat sink may be required to keep the junction temperature below this absolute maximum rating when the output is shorted indefinitely.

3.5 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.6 Outline Dimensions and Pad Functions: Dice outline dimensions, pad functions, and locations shall be specified in **Figure 1**.

3.7 Radiation Hardness Assurance (RHA):

3.7.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.7.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.7.3 Total dose bias circuit is specified in **Figure 2**.

3.8 Wafer (or Dice) Probe: Dice shall be 100% probed at Ta = +25°C to the limits shown in **Table I** herein. All reject dice shall be removed from the lot. This testing is normally performed prior to dicing the wafer into chips. Final specifications after assembly are sample tested during the element evaluation.

3.9 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Top side glassivation thickness shall be a **minimum of 4KÅ.**

3.10 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018. Copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

3.11 Traceability: Wafer Diffusion Lot and Wafer traceability shall be maintained through Quality Conformance Inspection.

4.0 QUALITY CONFORMANCE INSPECTION: Quality Conformance Inspection shall consist of the tests and inspections specified herein.

5.0 SAMPLE ELEMENT EVALUATION: A sample from **each wafer supplying dice** shall be assembled and subjected to element evaluation per **Table III** herein.

5.1 100 Percent Visual Inspection: All dice supplied to this specification shall be inspected in accordance with MIL-STD-883, Method 2010, Condition A. All reject dice shall be removed from the lot.

5.2 Electrical Performance Characteristics for Element Evaluation: The electrical performance characteristics shall be as specified in **Table I, Table IA** and **Table II** herein.

5.3 Sample Testing: Each wafer supplying dice for delivery to this specification shall be subjected to element evaluation sample testing. No dice shall be delivered until all the lot sample testing has been performed and the results found to be acceptable unless the customer supplies a written approval for shipment prior to completion of wafer qualification as specified in this specification.

5.4 Part Marking of Element Evaluation Sample Includes**:**

5.4.1 LTC Logo

5.4.2 LTC Part Number

5.4.3 Date Code

5.4.4 Serial Number

5.4.5 ESD Identifier per MIL-PRF-38535, Appendix A

5.4.6 Diffusion Lot Number

5.4.7 Wafer Number

5.5 Burn-In Requirement: Burn-In circuit for Flatpak, 10 lead package is specified in **Figure 3**.

5.6 Mechanical/Packaging Requirements: Case Outline and Dimensions are in accordance with **Figure 4.**

5.7 Terminal Connections: The terminal connections shall be as specified in **Figure 5.**

5.8 Lead Material and Finish: The lead material and finish shall be alloy 42 with hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

6.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

6.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

6.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with **Table III** herein.

6.3 Screening: Screening requirements shall be in accordance with **Table III** herein.

6.4 Source Inspection:

6.4.1 The manufacturer will coordinate Source Inspection at wafer lot acceptance and pre-seal internal visual.

6.4.2 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance, die visual, and final data review.

6.5 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

6.5.1 Lot Serial Number Sheets identifying all Canned Sample devices accepted through final inspection by serial number.

6.5.2 100% attributes (completed element evaluation traveler).
6.5.3 Element Evaluation variables data, including Burn-In and Op Life

6.5.4 SEM photographs (3.10 herein)

6.5.5 Wafer Lot Acceptance Report (3.9 herein)

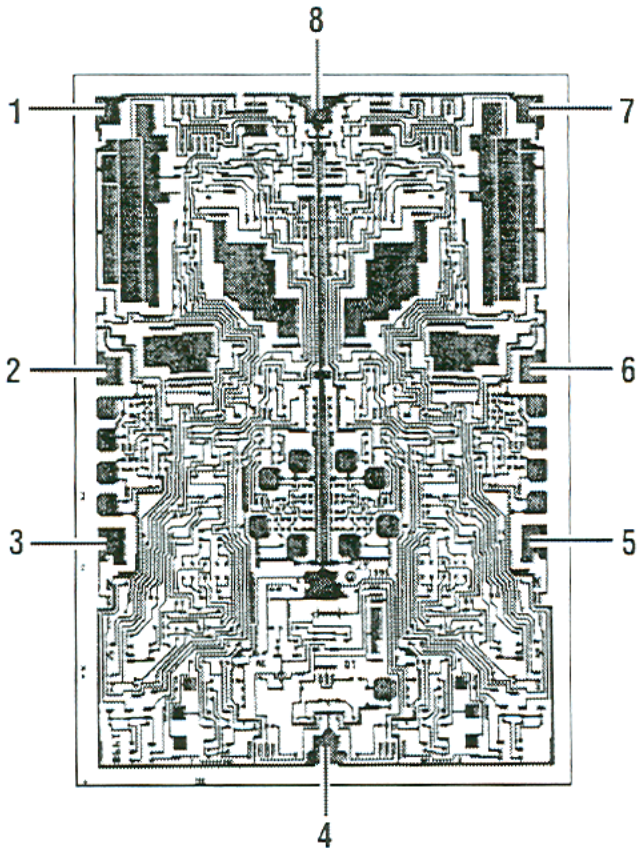
6.5.6 A copy of outside test laboratory radiation report if ordered

6.5.7 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 6.5.1 and 6.5.7 will be delivered as a minimum, with each shipment.

7.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All dice shall be packaged in multicavity containers composed of conductive, anti-static, or static dissipative material with an external conductive field shielding barrier.

DICE OUTLINE DIMENSIONS AND PAD FUNCTIONS



117mils × 82mils,
12mils thick.
Backside (substrate) is an alloyed gold layer.
Connect backside to V^+.

PAD FUNCTION

1. OUTPUT A
2. –INA
3. +INA
4. V^-
5. +INB
6. –INB
7. OUTPUT B
8. V^+

FIGURE 1

TOTAL DOSE BIAS CIRCUIT

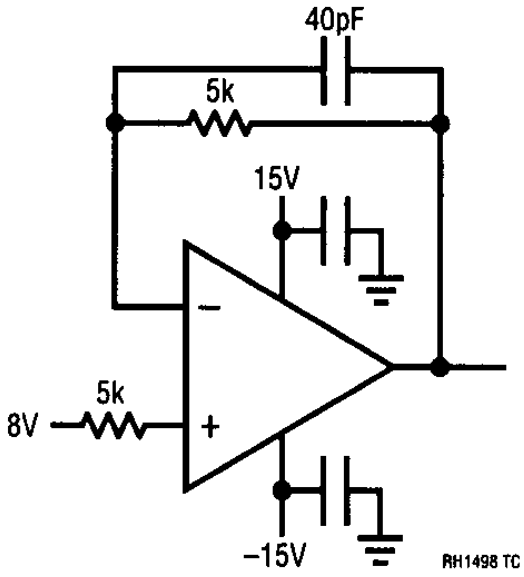
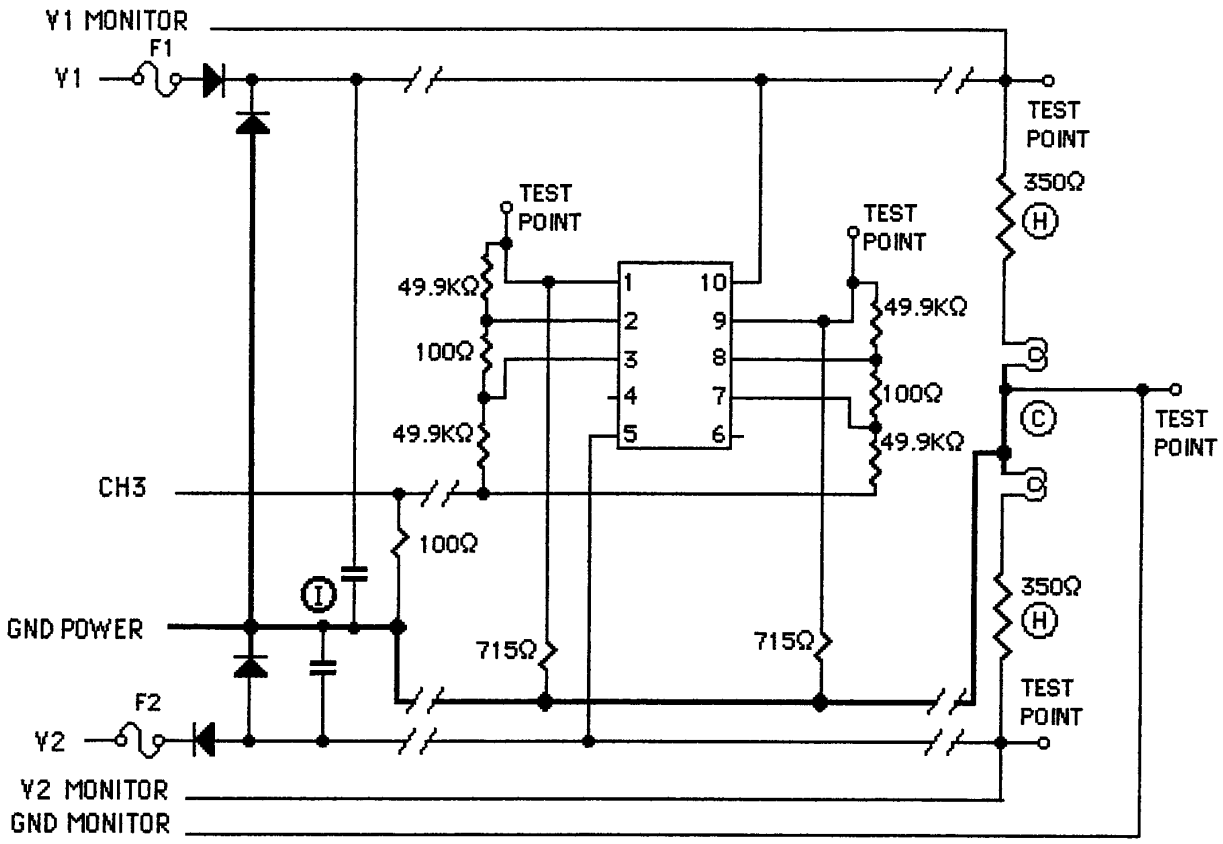


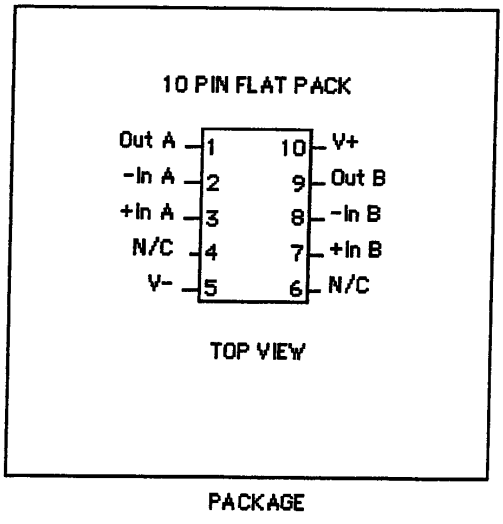
FIGURE 2

STATIC BURN-IN CIRCUIT



NOTES:

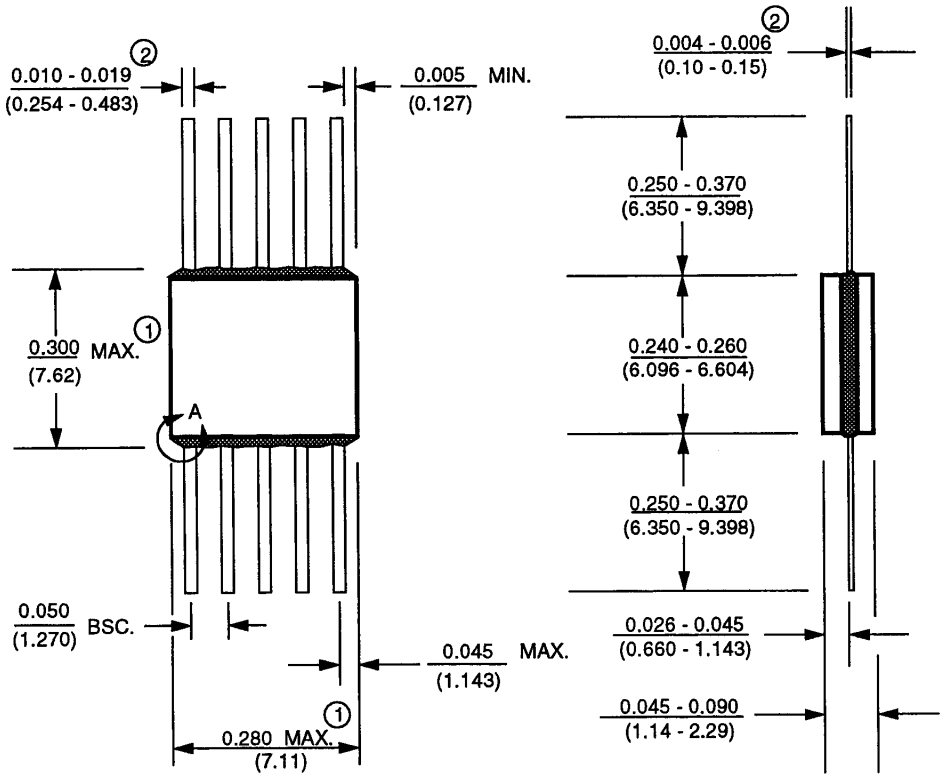
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = +161 °C maximum.
3. Ta = +125 °C.
4. Burn-in Voltages: V1 = +16V to +17V
   V2 = -16V to -17V
5. Current used per device:
   V+ = 5mA plus 50mA per board for lamp.
   V- = 5mA plus 50mA per board for lamp.
   Gnd = 4mA plus 100mA per board for lamps.
6. USE ALL OTHER INFORMATION ON # 04-06-0391



PACKAGE

FIGURE 3

Flatpak, 10 LEADS, CASE OUTLINE



NOTES:

① THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVER RUN

② INCREASE DIMENSIONS BY 0.003 INCH WHEN LEAD FINISH IS APPLIED (SOLDER DIPPED)

$\theta ja = 170°C/W$
$\theta jc = 40°C/W$

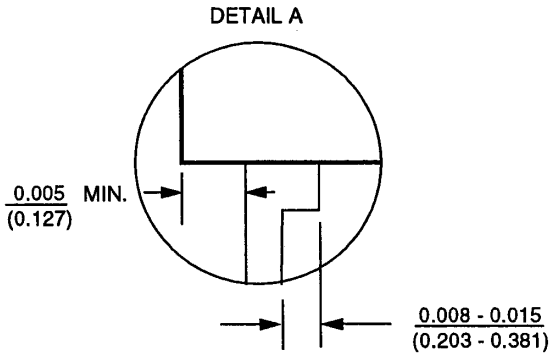


FIGURE 4

TERMINAL CONNECTIONS

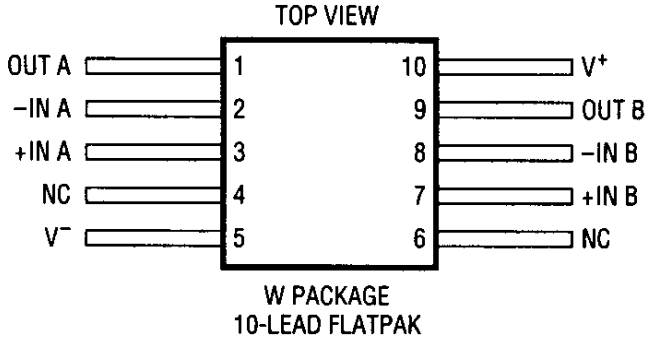


FIGURE 5

TABLE I DICE ELECTRICAL CHARACTERISTICS – Element Evaluation

DICE/DWF ELECTRICAL TEST LIMITS (Pre-Irradiation) $V_S = \pm 15V$; $V_{CM} = V_{OUT} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+, V^-$		800	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 1)	$V_{CM} = V^+$ to V^-		1400	µV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^-$	0 –715	715 0	nA nA
	Input Bias Current Match (Channel-to-Channel) (Note 1)	$V_{CM} = V^+, V^-$	0	200	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+, V^-$		70	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = –14.5V to 14.5V, R1 = 10k V_O = –10V to 10V, R1 = 2k	1000 500		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^+$ to V^-	90		dB
	CMRR Match (Channel-to-Channel) (Note 1)	$V_{CM} = V^+$ to V^-	84		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 16V$	90		dB
	PSRR Match (Channel-to-Channel) (Note 1)	$V_S = \pm 2V$ to $\pm 16V$	83		dB
V_{OL}	Output Voltage Swing (Low) (Note 2)	No Load I_{SINK} = 1mA I_{SINK} = 10mA		30 100 500	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 2)	No Load I_{SOURCE} = 1mA I_{SOURCE} = 10mA		10 150 800	mV mV mV
I_{SC}	Short-Circuit Current		±15		mA
I_S	Supply Current per Amplifier			2.5	mA
GBW	Gain-Bandwidth Product	f = 100kHz	6.8		MHz
SR	Slew Rate	$A_V = -1$, R_L = 10k $V_O = \pm 10V$, Measure at $V_O = \pm 5V$	3.5		V/µs

DICE/DWF PRE-IRRADIATION ELECTRICAL TEST LIMITS CONTINUED ON NEXT PAGE

TABLE IA DICE ELECTRICAL CHARACTERISTICS – Element Evaluation (CONTINUED)

DICE/DWF ELECTRICAL TEST LIMITS (Pre-Irradiation) V_S = 5V; V_{CM} = V_{OUT} = Half Supply, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^+, V^-		800	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 1)	V_{CM} = V^+ to V^-		1400	µV
I_B	Input Bias Current	V_{CM} = V^+ V_{CM} = V^-	0 –650	650 0	nA nA
	Input Bias Current Match (Channel-to-Channel) (Note 1)	V_{CM} = V^+, V^-	0	180	nA
I_{OS}	Input Offset Current	V_{CM} = V^+, V^-		65	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 75mV to 4.8V, R1 = 10k	600		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = V^+ to V^-	76		dB
	CMRR Match (Channel-to-Channel) (Note 1)	V_S = 5V, V_{CM} = V^+ to V^-	75		dB
PSRR	Power Supply Rejection Ratio	V_S = 4.5V to 12V; V_{CM} = V_O = 0.5V	88		dB
	PSRR Match (Channel-to-Channel) (Note 1)	V_S = 4.5V to 12V; V_{CM} = V_O = 0.5V	82		dB
V_{OL}	Output Voltage Swing (Low) (Note 2)	No Load I_{SINK} = 1mA I_{SINK} = 2.5mA		30 100 200	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 2)	No Load I_{SOURCE} = 1mA I_{SOURCE} = 2.5mA		10 150 250	mV mV mV
I_{SC}	Short-Circuit Current		±12		mA
I_S	Supply Current per Amplifier			2.2	mA

Note 1: Matching parameters are the difference between amplifiers A and B.

Note 2: Output voltage swings are measured between the output and power supply rails.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

TABLE II ELECTRICAL CHARACTERISTICS – Post-Irradiation

(Postirradiation) V_S = 5V; V_{CM} = half supply, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	10Krad(Si) MIN	10Krad(Si) MAX	20Krad(Si) MIN	20Krad(Si) MAX	50Krad(Si) MIN	50Krad(Si) MAX	100Krad(Si) MIN	100Krad(Si) MAX	200Krad(Si) MIN	200Krad(Si) MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^+, V^-			950		950		950		950		950	µV
I_B	Input Bias Current	V_{CM} = V^+, V^-			700		750		800		850		900	nA
I_{OS}	Input Offset Current	V_{CM} = V^+, V^-			65		65		65		65		65	nA
	Input Voltage Range			V^-	V^+	V^-	V^+	V^-	V^+	V^-	V^+	V^-	V^+	V
A_{VOL}	Large-Signal Voltage Gain	V_O = 75mV to V^+ – 0.2V R1 = 10k		300		300		300		300		300		V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = V^+ to V^-		70		70		70		70		70		dB
	CMRR Match (Channel-to-Channel)	V_{CM} = V^+ to V^-	3	70		70		70		70		70		dB
PSRR	Power Supply Rejection Ratio	V_S = 4.5V to 12V, V_{CM} = V_O = 0.5V		88		88		88		88		88		dB
	PSRR Match (Channel-to-Channel)	V_S = 4.5V to 12V, V_{CM} = V_O = 0.5V	3	82		82		82		82		82		dB
V_{OUT}	Output Voltage Swing Low	No Load I_{SINK} = 1mA I_{SINK} = 2.5mA	4		60 100 200		60 100 200		60 100 200		60 100 200		60 100 200	mV mV mV
	Output Voltage Swing High	No Load I_{SOURCE} = 1mA I_{SOURCE} = 2.5mA	4		20 150 250		20 150 250		20 150 250		20 150 250		20 150 250	mV mV mV
I_{SC}	Short-Circuit Current			±8		±8		±8		±8		±8		mA
I_S	Supply Current				2.2		2.2		2.2		2.2		2.2	mA
SR	Slew Rate	V_S = ±2.5V, A_V = –1, R_L = 10k, V_O = ±2V, Measure at V_O = ±1V		2		2		2		2		2		V/µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below this absolute maximum rating when the output is shorted indefinitely.

Note 3: Matching parameters are the difference between amplifiers A and B.

Note 4: Output voltage swings are measured between the output and power supply rails.

TABLE III RH ELEMENT EVALUATION TABLE QUALIFICATION OF DICE SALES

LINEAR TECHNOLOGY

RH CANNED SAMPLE TABLE FOR QUALIFYING DICE SALES

SUBGROUP	CLASS K/S	CLASS H/B	OPERATION	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY (ACCEPT NUMBER)
1	X		SEM	2018	N/A	REF. METHOD 2018 FOR S/S
2	X	X	ELEMENT ELECTRICAL (WAFER SORT @ 25°C)			100%
3	X	X	ELEMENT VISUAL (2nd OP)	2010	A	100%
4	X	X	INTERNAL VISUAL (3rd OP)	2010	A	ASSEMBLED PARTS ONLY
	X		DIE SHEAR MONITOR	2019		
	X		BOND PULL MONITOR	2011		
5	X		STABILIZATION BAKE	1008	C	ASSEMBLED PARTS ONLY
	X		TEMPERATURE CYCLE	1010	C	
	X		CONSTANT ACCELERATION	2001	E	
	X		FINE LEAK	1014	A	
	X		GROSS LEAK	1014	C	
6	X		FIRST ROOM ELECTRICAL - READ & RECORD (REPLACE ANY ASSEMBLY-RELATED REJECTS)			65 (3)
	X		ELECT. READ & RECORD @ +125°C or +150°C, -55°C			
	X		BURN-IN: +125°C/240 hrs. or +150°C/120 hrs.	1015	+125°C MINIMUM 240 HOURS	
	X		POST BURN-IN ELECTRICAL @ 25°C READ & RECORD			
	X		PRE OP-LIFE ELECTRICAL @ 25°C READ & RECORD			
	X		OPERATING LIFE: +125°C/1000 hrs. or +150°C/500 hrs.	1005	+125°C MINIMUM 1000 HOURS	
	X		POST OP-LIFE ELECT. (R&R 25°C, +125°C or +150°C, -55°C)			
7	X	X	WIRE BOND EVALUATION	2011		15 (0) or 25 (1) - # of wires

NOTE: LTC is not qualified to process to MIL-PRF-38534. This is an LTC imposed element evaluation that follows MIL-STD-883 test methods and conditions. Please note the quantity and accept number from a Sample Size Series of 10% accept on 3, and note that the actual sample and accept number does not begin until Subgroup 6.

NOTE: Tests within Subgroup 5 may be performed in any sequence.

NOTE: LTC's radiation tolerant (RH) die has a topside glassivation thickness of 4KÅ minimum.

NOTE: Sample sizes on the travelers may be larger than that indicated in the above table; however, the larger sample size is to accommodate extra units for replacement devices in the event of equipment or operator error and for assembly related rejects in Subgroup 6, and for Wire Bond Evaluation, Subgroup 7. The larger sample size is at all times kept segregated and, if used for qualification, has all the required processing imposed.

05/22/13