REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	07/10/96
A	DELETION OF PARAGRAPHS 3.12.1, 3.12.2, AND INCORPORATION OF PARAGRAPH 3.12.1 INTO PARAGRAPH 3.12, PAGE 4. PARAGRAPH 4.4.3 MOVED FROM PAGE 5 TO PAGE 4.	09/25/96
B	• PAGE 2: ADDED PARAGRAPHS 3.2.1, 3.2.2, AND 3.2.3. PARAGRAPH 3.3.b, ADDED "SEE PARAGRAPH 3.2". • PAGE 3: ADDED PARAGRAPHS 3.8.1, 3.8.2, AND 3.8.3. • PAGE 4: 4.4.2, GROUP B INSPECTION, REDEFINED. • PAGE 5: PARAGRAPH 4.4.3, GROUP D INSPECTION, REDEFINED. PARAGRAPH 4.5, SOURCE INSPECTION, REDEFINED. • PAGE 6: ADDED θja AND θjc TO FIGURE 1, TO5 CASE OUTLINE. • PAGE 7: ADDED θja AND θjc TO FIGURE 2, CERAMIC DIP CASE OUTLINE. • PAGE 8: ADDED θja AND θjc TO FIGURE 3, BOTTOM BRAZED FLATPACK CASE OUTLINE.	11/25/97
C	PAGE 4, AMENDED PARAGRAPHS 4.1 AND 4.1.1 TAKING EXCEPTION TO ANALYSIS OF CATASTROPHIC FAILURES.	02/23/98
D	ADDED OPTION 4, 10 LEAD GLASS SEALED FLATPACK.	05/29/98
E	PAGE 6, 7, 8, CHANGED θja AND θjc .	09/24/99
F	• PAGE 3: PARAGRAPHS 3.2.1, 3.2.2, 3.2.3, 3.2.4, FIGURES 1, 2, 3 AND 4 REMOVED. • PAGE 4: PARAGRAPHS 3.7 AND PARAGRAPH 3.9 CHANGED VERBIAGE IN LINE 2 OF EACH PARAGRAPH. • PAGE 5: PARAGRAPHS 4.3, 4.4.1, 4.4.2.2 CHANGED VERBIAGE IN LINE 2 OF EACH PARAGRAPH. • PAGE 6: PARAGRAPHS 4.4.3.2 CHANGED VERBIAGE IN LINE 1.	11/19/99
G	PAGE 9: CHANGED θja FROM +225°C/W TO +170°C/W AND θjc FROM +40°C/W TO 18°C/W PER PACKAGE ENGINEERING.	09/05/00
H	PAGE 9: CHANGED θja FROM +170°C/W TO +160°C/W PER PACKAGE ENGINEERING.	01/09/01
J	CHANGED DELTA IB LIMITS FROM 50na TO 100na. CONVERSION OF SPECIFICATION FROM WORD PERFECT TO MSWORD.	08/29/01
K	• PAGE 2, AN ADDITIONAL REVISION RECORD PAGE WAS INSTALLED. CONTINUED ON NEXT PAGE…..	03/26/02

REVISION RECORD AND DESCRIPTION CONTINUED ON NEXT PAGE.

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
INDEX	REVISION	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
REVISION	PAGE NO.	18	19	20														
INDEX	REVISION	U	U	U														

				LINEAR TECHNOLOGY CORPORATION MILPITAS, CALIFORNIA			
	ORIG						
	DSGN			TITLE:			
	ENGR			**MICROCIRCUIT, LINEAR, RH119, HIGH PERFORMANCE DUAL COMPARATOR**			
	MFG						
	CM						
	QA			SIZE	CAGE CODE	DRAWING NUMBER	REV
	PROG				**64155**	**05-08-5026**	**U**
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:			

FOR OFFICIAL USE ONLY

REVISION RECORD		
REV	DESCRIPTION	DATE
K	• PAGE 3: PARAGRAPH 3.2, DELETED OPTION 3, RH119WB, RENUMBERED PARAGRAPH AND OPTIONS. • PAGE 4: PARAGRAPH 3.6, TABLE IA CHANGED TO TABLE II. PARAGRAPH 3.7, TABLE III CHANGED TO TABLE IV. PARAGRAPH 3.8, DELETED OPTION 3, RH119WB BURN-IN FIGURES, RENUMBERED PARAGRAPHS AND OPTIONS. PARAGRAPH 3.10.1, DELETED FIGURE 3, RH119WB CASE OUTLINE, RENUMBERED FIGURES. PARAGRAPH 3.10.2, RENUMBERED TERMINAL CONNECTIONS FIGURES. PARAGRAPH 3.10.3, RENUMBERED LEAD MATERIAL AND FINISH DEVICE OPTIONS. PARAGRAPH 3.11.1 WAS CHANGED FROM "…dosage rate of approximately 20 Rads per Second" TO "…dosage rate of less than or equal to 10 Rads per second". • PAGE 5: PARAGRAPH 3.11.3, FIGURE 14 CHANGED TO FIGURE 13. PARAGRAPHS 4.1 THROUGH 4.4.2 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. • PAGE 6: PARAGRAPHS 4.4.2.1 THROUGH 4.4.3 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. PARAGRAPHS 4.6.2 THROUGH 4.6.4 WERE RE-WRITTEN. THESE DATA PROVIDED, AND DATA AVAILABLE. • PAGE 7: PARAGRAPH 4.6.10 NOTE, ADDED FURTHER EXPLANATION OF MINIMUM DELIVERED DATA. • DELETED CASE OUTLINE, TERMINAL CONNECTION, AND STATIC / DYNAMIC BURN-IN FIGURES FOR RH119WB (BOTTOM BRAZED PACKAGE). • PAGES 8 THROUGH 18, ALL FIGURE TITLES CHANGED TO HAVE DEVICE OPTIONS AND PACKAGE TYPES AT TOP OF PAGE, AND HAVE ALL FIGURES AT BOTTOM OF PAGE. • PAGE 11, MOVED FIGURES TO BETTER FIT ON THE PAGE. • PAGE 19, TABLES I, II AND CORRESPONDING NOTES ALL ON ONE PAGE.	03/26/02
L	• PAGE 1: REMOVED REDUNDANT INFORMATION ALREADY SPECIFIED IN REVISION J REGARDING THE CONVERSION FROM WORD PERFECT TO MICROSOFT WORD. CORRECTED CAGE CODE FROM 94155 TO 64155. • PAGE 3: CORRECTED DEVICE TYPE OPTION 2 FROM RH119J14 TO RH119J. • PAGE 20: TABLE IV, ELECTRICAL TEST REQUIREMENTS: SUBGROUPS 5 AND 6 WERE ADDED TO THE FINAL ELECTRICAL TEST REQUIREMENTS AND GROUP A TEST REQUIREMENTS.	05/30/02
M	• PAGE 18, TABLES I AND II CHANGED TO MATCH THE DATASHEET. OUTPUT LEAKAGE CURRENT CHANGED V_{OUT} 35V TO V^{-} = 35V. • ENTIRE SPECIFICATION REVISED TO M. SPEC VERBIAGE REDUCED TO PAGES 3 – 6 MAKING THE SPEC 19 PAGES INSTEAD OF 20 PAGES.	12/03/02
N	• PAGE 9, CHANGED OUTLINE DRAWING PIN 1 NOTCH MOVED TO INSIDE LEAD LOCATION.	5/19/03
P	• PAGE 4, CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC	03/15/05
R	• PAGE 5, CHANGED IN BOTH PARAGRAPHS 4.2, 4.3 IN CONJUNCTION TO 3.3 CHANGED TO 3.4 AND PARAGRAPH 4.3 CHANGED 3.1.1 TO 3.1 AND 3.2.1 TO 3.1.1 • PAGE 4, PARAGRAPH 3.10.3 ADDED OPTION 3 IS ALLOY 42 FOR FLATPACK. • TABLE 1: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION) OUTPUT LEAKAGE CURRENT CHANGED FROM Vin $\leq$ 5mV, TO Vin $\geq$ 5mV. FIGURE 7 STATIC B/I CHANGED NOTES: 2 FROM Tj = 194°C MAX. AT 150°C AMBIENT TO Ta = 125°C. CHANGED NOTES: 3 FROM Tj = 169°C MAX. AT 125°C AMBIENT TO Tj = +166°C MAX AT 150°C/W. CHANGED NOTES: 4 FROM BURN-IN VOLTAGES:V1 = +18V TO + 19.8V. V2 = -18V TO -19.8V. TO Tc = +149°CMIN AT 40°C/W. ADDED NOTE: 5 BURN-IN VOLTAGES: V1 = +15V TO +16.5V. V2 = -15V TO -16.5V.	01/07/08

CONTINUED ON NEXT PAGE

REVISION RECORD		
REV	DESCRIPTION	DATE
R	FIGURE 9 STATIC B/I CHANGED NOTE: 2 FROM Tj = 182°C MAX AT Ta OF 150°C TO Ta = +125°C. CHANGED NOTE: 3 FROM Tj = 157°C MAX AT Ta OF 125°C TO Tj = +154°C MAX AT 95°C/W. CHANGED NOTE: 4 FROM BURN-IN VOLTAGES: V1 = +18V TO +19.8V. V2 = -18V TO -19.8V. TO Tc = +140°C MIN AT 25°C/W. ADDED NOTE 5 BURN-IN VOLTAGE: V1 = +15V TO +16.5V. V2 = -15 TO -16.5V FIGURE 11 STATIC B/I CHANGED NOTE: 2 FROM Tj = 197°C MAX FOR Ta OF 150°C TO Ta = +125°C. NOTE: 3 CHANGED FROM Tj = 172°C MAX FOR Ta OF 125°C TO Tj = +170°C MAX AT 170°C/W. CHANGED NOTE: 4 FROM BURN-IN VOLTAGES: V1 = +18V TO +19.8V. V2 = -18V TO -19.8V. TO Tc = +153°C MIN AT 40°C/W. ADDED NOTE 5 BURN-IN VOLTAGE: V1 = +15V TO +16.5V. V2 = -15 TO -16.5V. PER PRODUCT ENG.	01/07/08
S	• PAGE 5 PARAGRAPH 3.10.3 CHANGED OPTION 2 TO ALLOY 42 PACKAGE REQUIREMENT. • PAGE 6 PARAGRAPH 3.11.1 CHANGED VERBIAGE.	05/13/08
T	• PAGE 6, PARAGRAPH 4.4.2 CHANGED VERBIAGE. • PAGE 10, FIGURE 3 NOTE 2 ADDED TO LEAD THICKNESS.	06/12/08
U	• **PAGE 12, FIGURE 7, PAGE 14, FIGURE 9, PAGE 16, FIGURE 11, BURN IN CIRCUITS AMENDED.**	**11/10/08**

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-STD-883	Test Method and Procedures for Microcircuits
MIL-STD-1835	Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH119 High Performance Comparator, processed to space level manufacturing flow.

3.2 Part Number:

3.2.1 Option 1 – RH119H (TO5 Metal Can, 10 Leads)

3.2.2 Option 2 – RH119J (Ceramic Dip, 14 Leads)

3.2.3 Option 3 – RH119W (Glass Sealed Flatpack, 10 Leads)

3.3 Part Marking Includes:

a. LTC Logo

b. LTC Part Number (See Paragraph 3.2)

c. Date Code

d. Serial Number

e. ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings:

Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Differential Input Current	±5mA
Input Voltage (See Note 1)	
Output Short-Circuit Duration	10 Sec
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

Note 1: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 2.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and Table II.

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in Table IV herein.

3.8 Burn-In Requirement:

3.8.1 Option 1 (TO5): Static Burn-In, Figure 7; Dynamic Burn-In, Figure 8

3.8.2 Option 2 (Ceramic Dip): Static Burn-In, Figure 9; Dynamic Burn-In, Figure 10

3.8.3 Option 3 (Glass Sealed Flatpack) : Static Burn-In, Figure 11; Dynamic Burn-In, Figure 12

3.9 Delta Limit Requirement: Delta limit parameters are specified in Table III herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1, Figure 2, and Figure 3.

3.10.2 Terminal Connections: The terminal connections shall be as specified in Figure 4, Figure 5, and Figure 6.

3.10.3 Lead Material and Finish: The lead material and finish for Device Options 1, shall be Kovar. Option 2, 3 is Alloy 42. The lead finishes shall be hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

3.11 Radiation Hardness Assurance (RHA):

3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.11.3 Total dose bias circuit is specified in Figure 13.

3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: To side glassivation thickness shall be a minimum of 4KÅ.

3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1, and 3.4 of the test method. Electrical testing shall be as specified in Table IV herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in Table IV herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroups 1-4 plus 6 are performed on every assembly lot, and Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1

Group B, Subgroup 2c = 10%	Group B, Subgroup 5 = *5% (*per wafer or inspection lot whichever is the larger quantity)
Group B, Subgroup 3 = 10%	
Group B, Subgroup 4 = 5%	Group B, Subgroup 6 = 15%

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Source Inspection:

4.5.1 The manufacturer will coordinate Source Inspection at wafer lot acceptance and pre-seal internal visual.

4.5.2 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance and final data review.

4.6 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.6.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.6.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.6.3 Burn-In Variables Data and Deltas (if applicable)

4.6.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.6.5 Generic Group D data (4.4.3 herein)

4.6.6 SEM photographs (3.13 herein)

4.6.7 Wafer Lot Acceptance Report (3.13 herein)

4.6.8 X-Ray Negatives and Radiographic Report

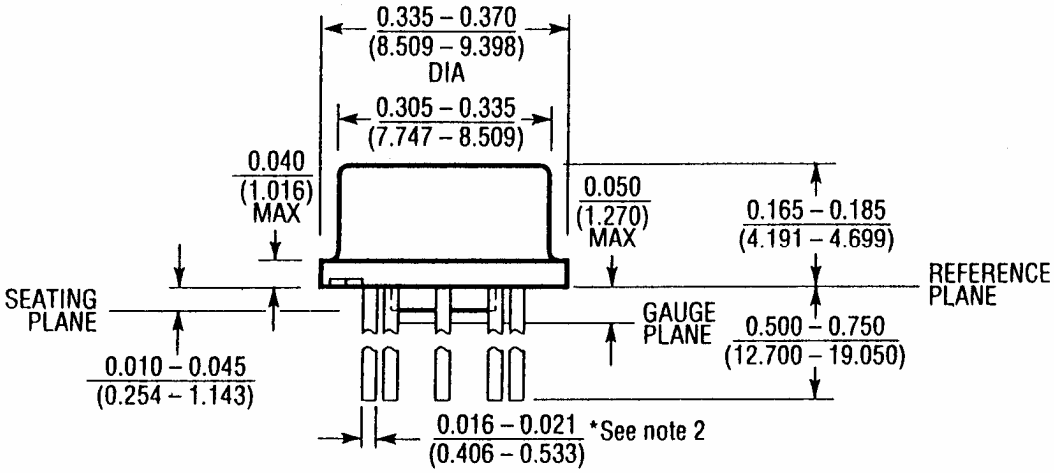
4.6.9 A copy of outside test laboratory radiation report if ordered

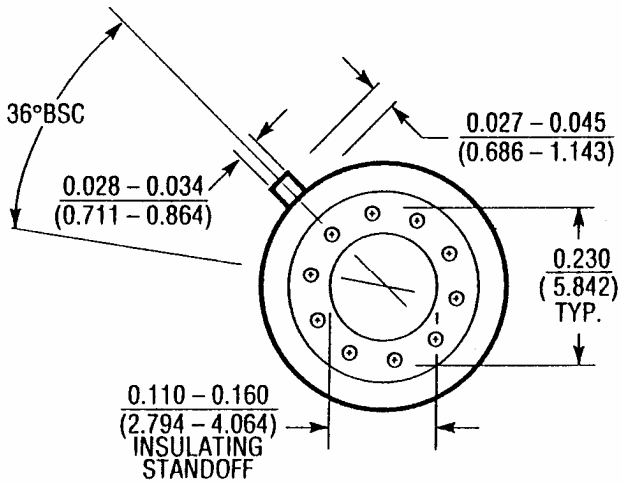
4.6.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 4.6.1 and 4.6.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as "No Charge Data".

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

DEVICE OPTION # 1
(H) TO5 / 10 LEADS CASE OUTLINE





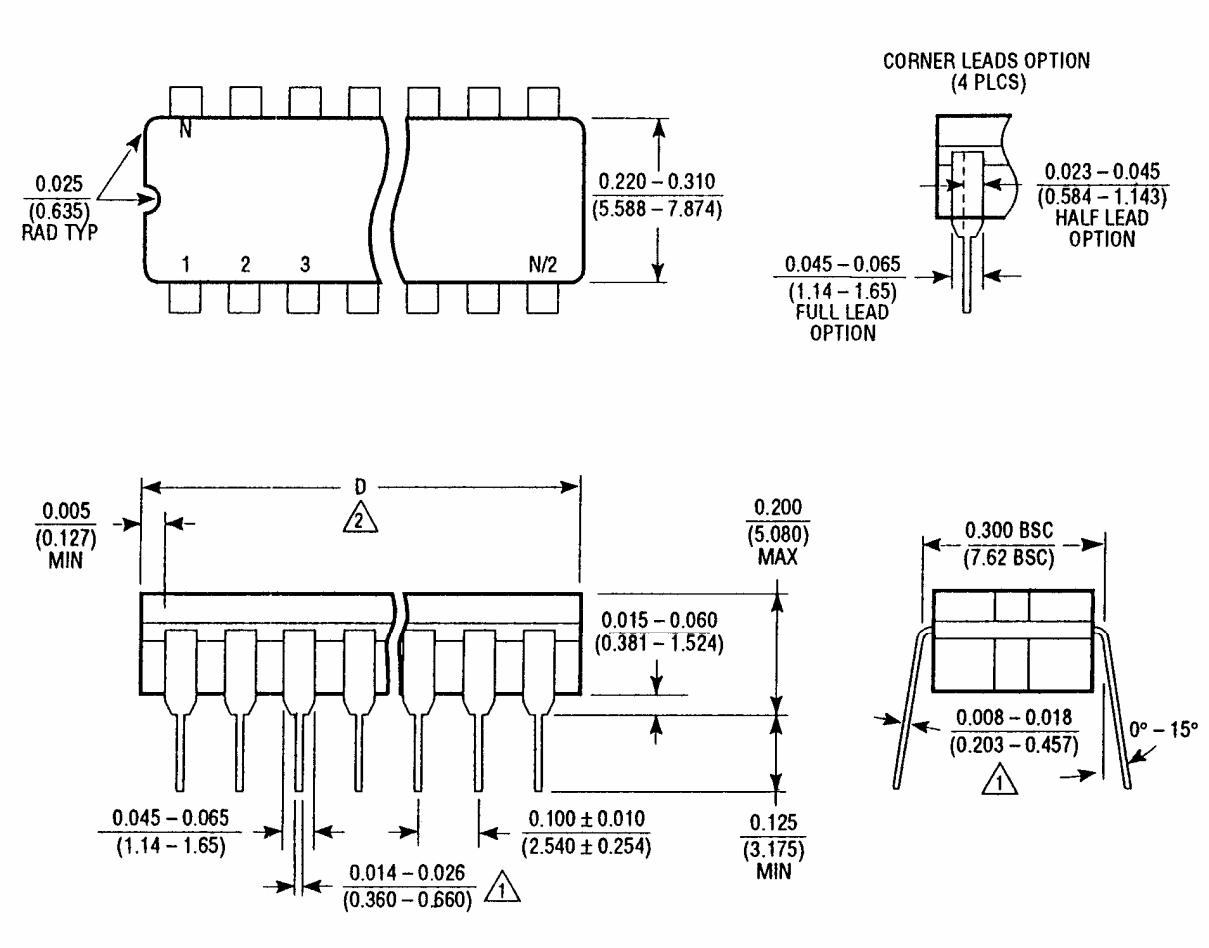
NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLAN.

2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 – 0.024 (0.406 – 0.610)

θja = +150°C/W
θjc = +40°C/W

FIGURE 1

DEVICE OPTION # 2
(J14) CERAMIC DIP / 14 LEADS CASE OUTLINE

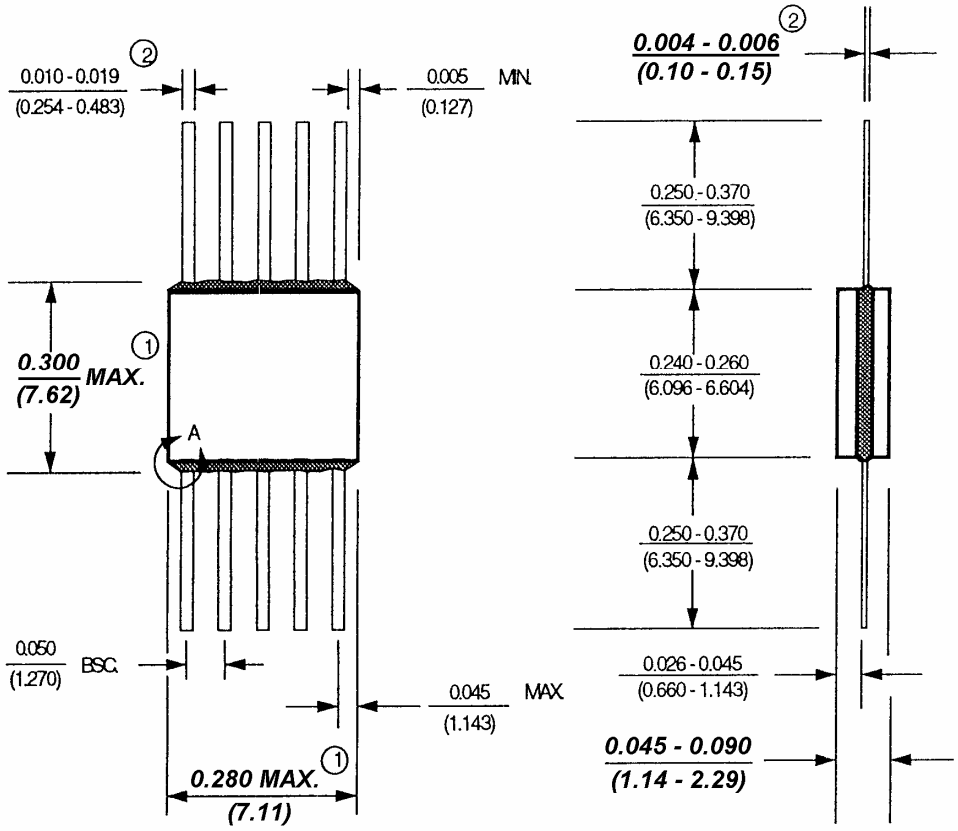


NOTE: 1. LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.
2. 14 LEAD D MAX = .0785 (19.939)

θja = +95°C/W
θjc = +25°C/W

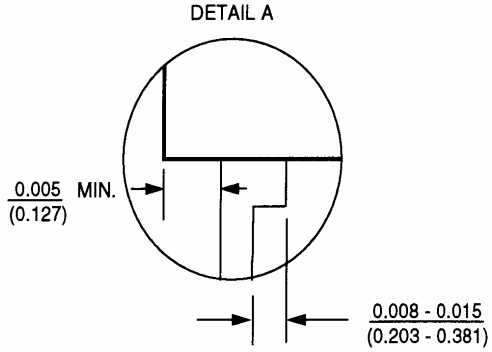
FIGURE 2

DEVICE OPTION # 3
(W10) GLASS SEALED FLATPACK / 10LEADS CASE OUTLINE



NOTE: 1. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVER RUN.

NOTE: 2. INCREASE DIMENSION BY 0.003 INCH WHEN LEAD FINISH IS APPLIED (SOLDER DIPPED).

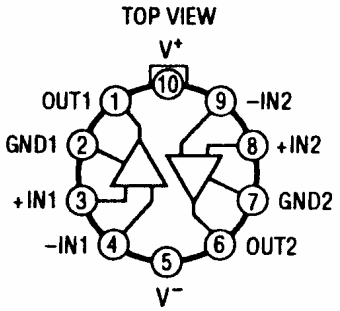


θ_{ja} = +170°C/W
θ_{jc} = +40°C/W

FIGURE 3

TERMINAL CONNECTIONS

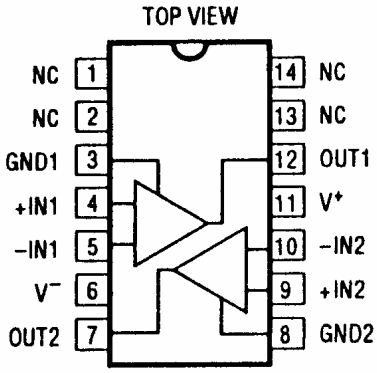
DEVICE OPTION #1, TO5 10 LEAD METAL CAN



H PACKAGE
10-LEAD TO-5 METAL CAN

FIGURE 4

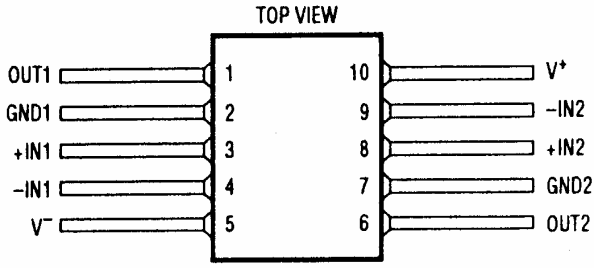
DEVICE OPTION #2, 14 LEAD CERAMIC DIP



J PACKAGE
14-LEAD CERDIP

FIGURE 5

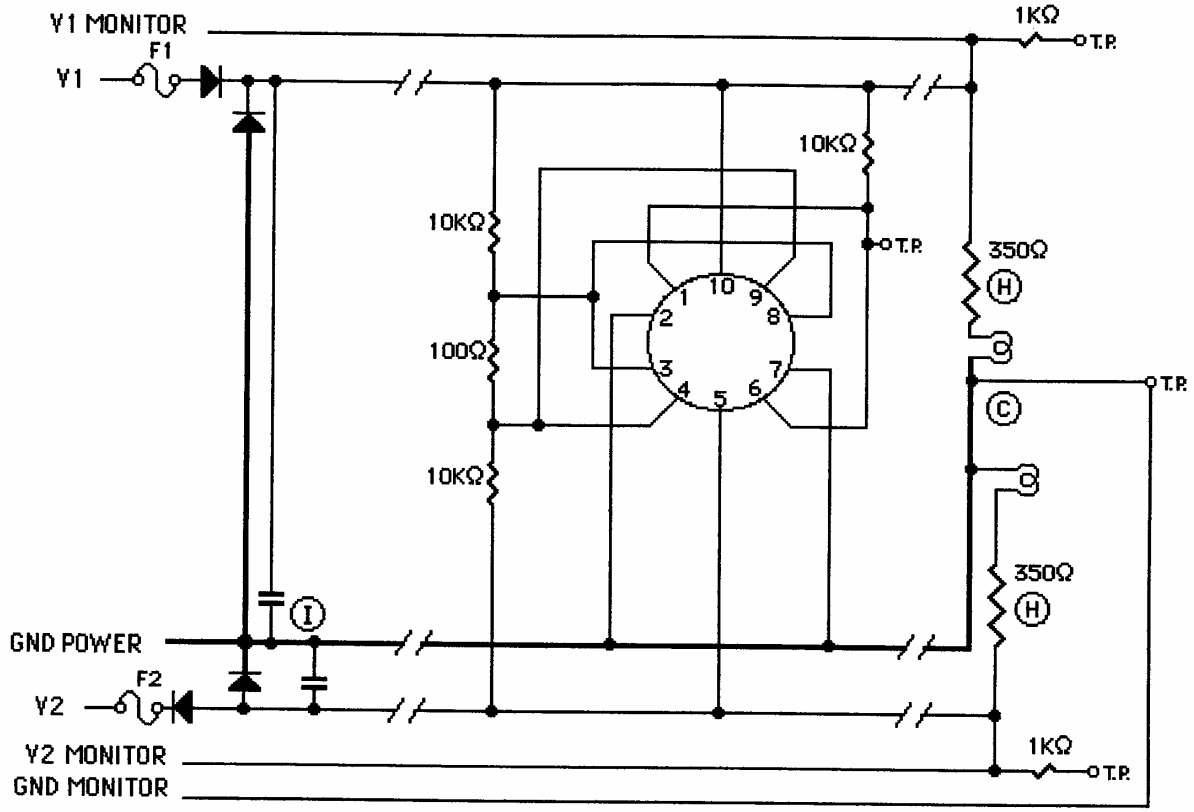
DEVICE OPTION #3, GLASS SEALED 10 LEAD FLATPACK



W PACKAGE
10-LEAD CERPAC

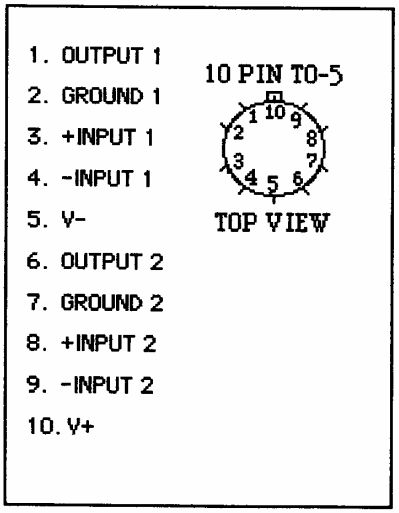
FIGURE 6

STATIC BURN-IN CIRCUIT
OPTION 1, TO5 METAL CAN / 10 LEADS



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Ta = +125 °C.
3. Tj = +152 °C max at 150 °C/W.
4. Tc = +134 °C min at 40 °C/W.
5. Burn-in voltages: V1 = +15V to +16.5V
   V2 = -15V to -16.5V

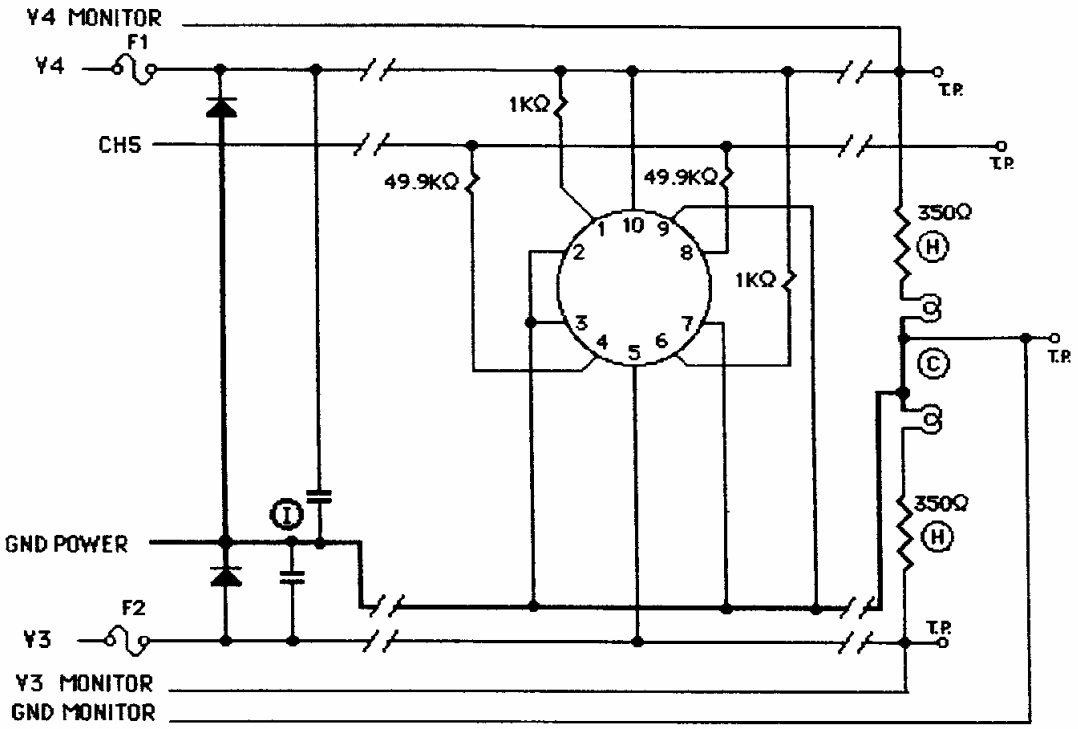


PACKAGE AND PINOUT

FIGURE 7

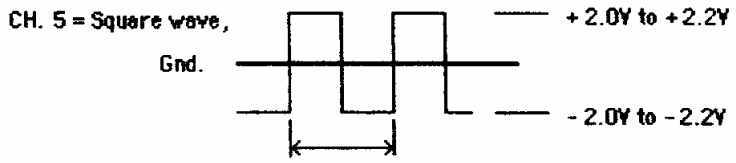
θja = 150°C/W
θjc = 40°C/W

DYNAMIC BURN-IN CIRCUIT
OPTION 1, TO5 METAL CAN / 10 LEADS



NOTES:

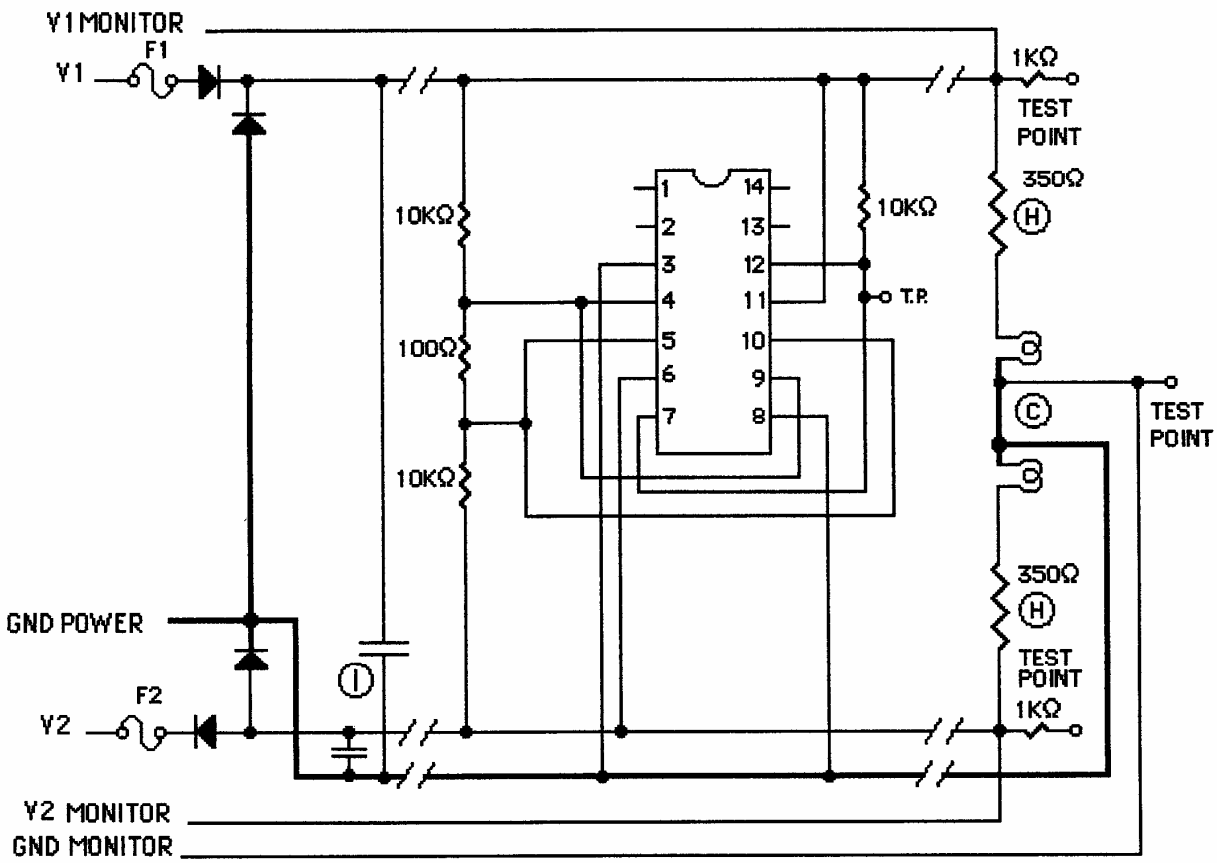
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 159°C maximum.
3. Ta = 125°C.
4. Burn-in Voltages: V4 = +15V to +16.5V
   V3 = -15V to -16.5V



Frequency, 900hz(1.1ms) to 1.1khz(909µs) ms)

FIGURE 8

STATIC BURN-IN CIRCUIT
OPTION #2, CERDIP / 14 LEADS



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Ta = +125 °C.
3. Tj = +154 °C max at 95 °C/W.
4. Tc = +140 °C min at 25 °C/W.
5. Burn-in voltages: V1 = +15V to +16.5V
   V2 = -15V to -16.5V

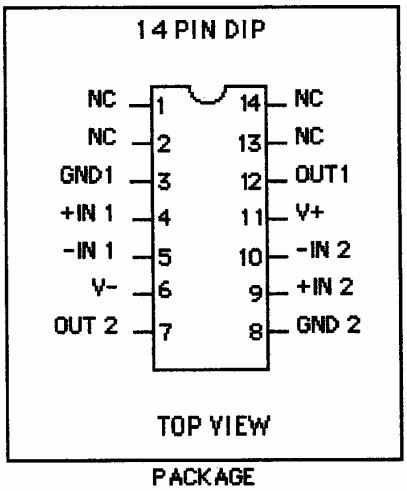
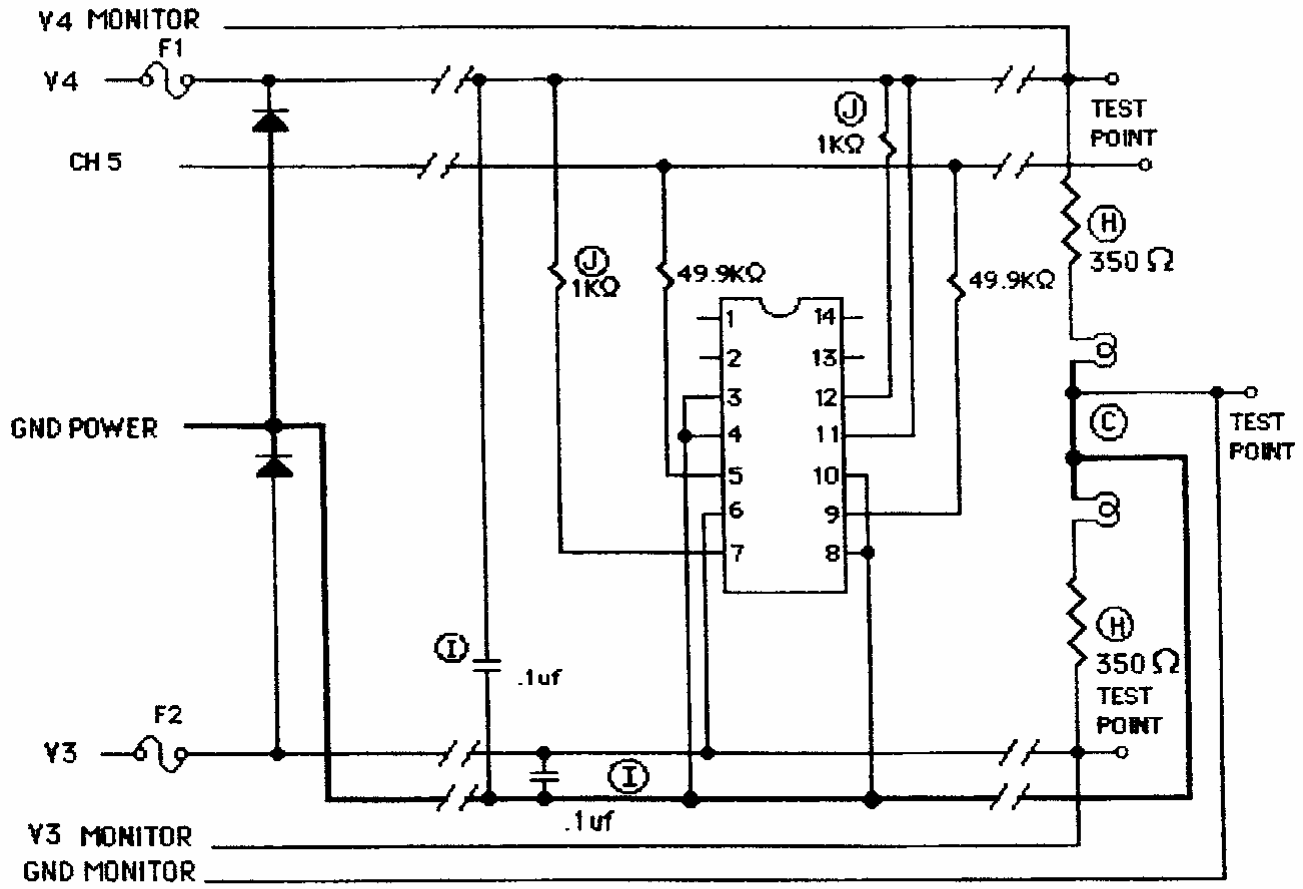


FIGURE 9

θja = 95°C/W
θjc = 25°C/W

DYNAMIC BURN-IN CIRCUIT
OPTION 2, CERDIP / 14 LEADS

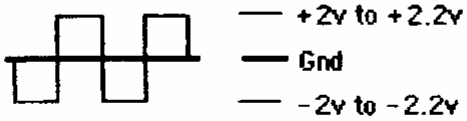


NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.

2. Burn-in Voltages: V4 = +15v to +16.5v
   V3 = - 15v to -16.5v

3. CH 5 = Square wave,

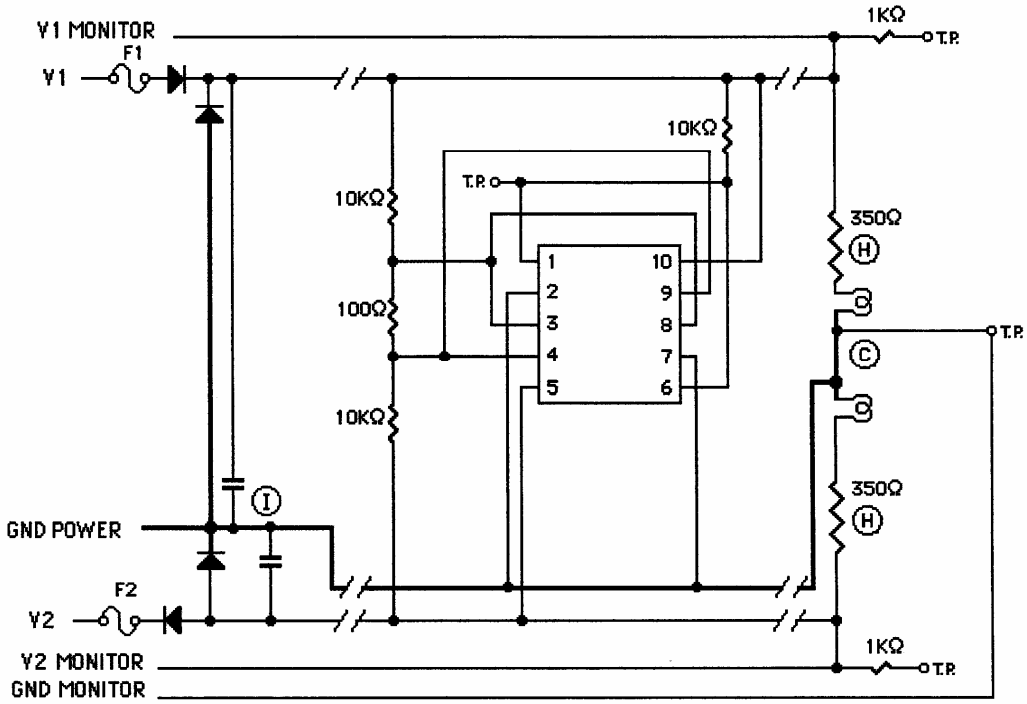


   Frequency, 900Hz (1.1ms) to 1.1 KHz (909us)

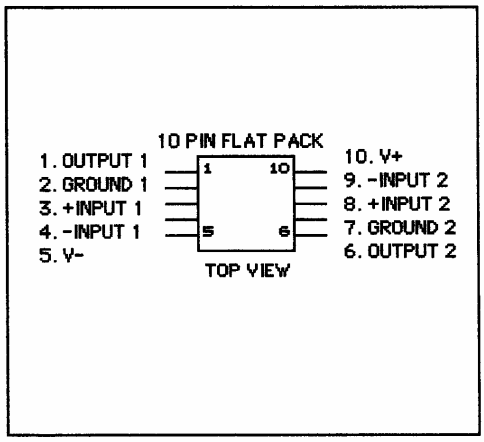
4. Tj max at 125°C ambient = 156°C

FIGURE 10

STATIC BURN-IN CIRCUIT
OPTION 3, GLASS SEALED FLATPACK / 10 LEAD



NOTES:
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Ta = +125 °C.
3. Tj = +170 °C max at 170 °C/W.
4. Tc = +153 °C min at 40 °C/W.
5. Burn-in voltages: V1 = +15V to +16.5V
   V2 = -15V to -16.5V

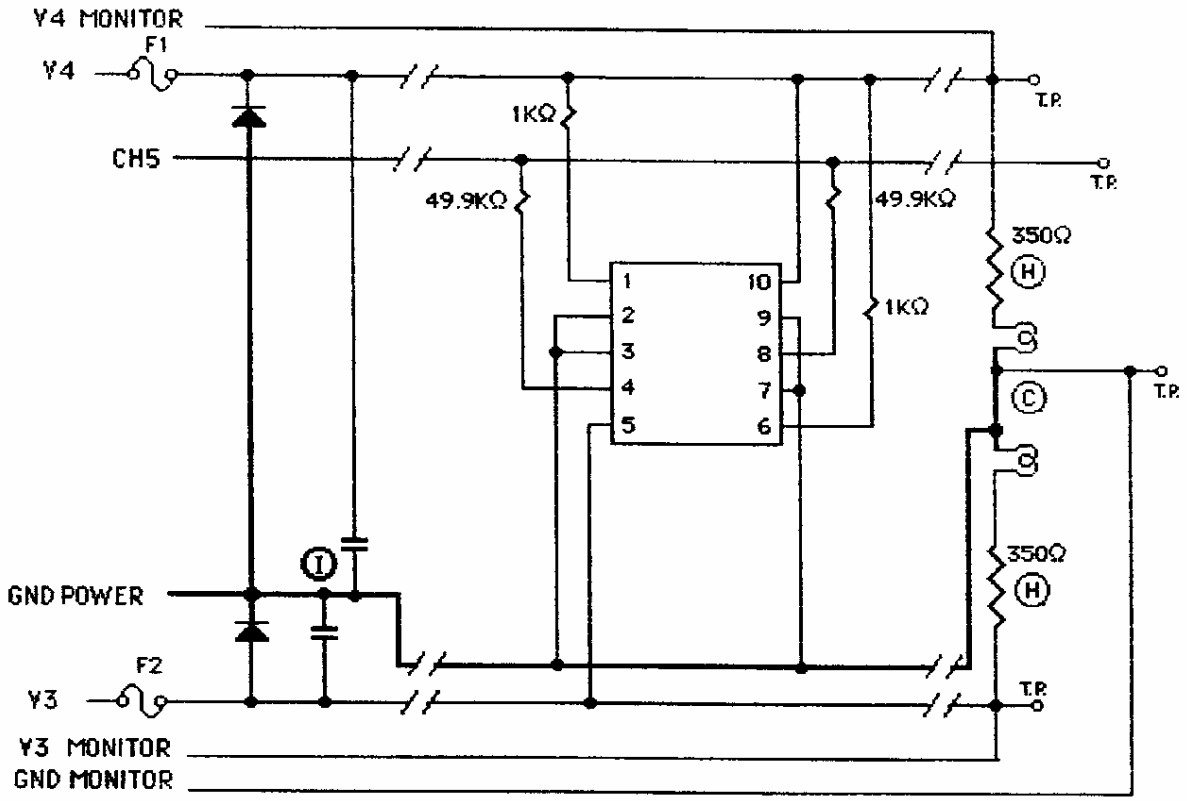


PACKAGE AND PINOUT

FIGURE 11

θja = 170°C/W
θjc = 40°C/W

DYNAMIC BURN-IN CIRCUIT
OPTION 3, GLASS SEALED FLATPACK / 10 LEAD



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 168°C maximum.
3. Ta = 125°C.
4. Burn-in Voltages: V4 = +15V to +16.5V
   V3 = -15V to -16.5V

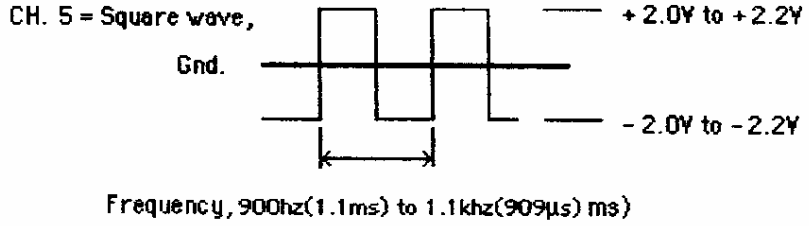


FIGURE 12

TOTAL DOSE BIAS CIRCUIT

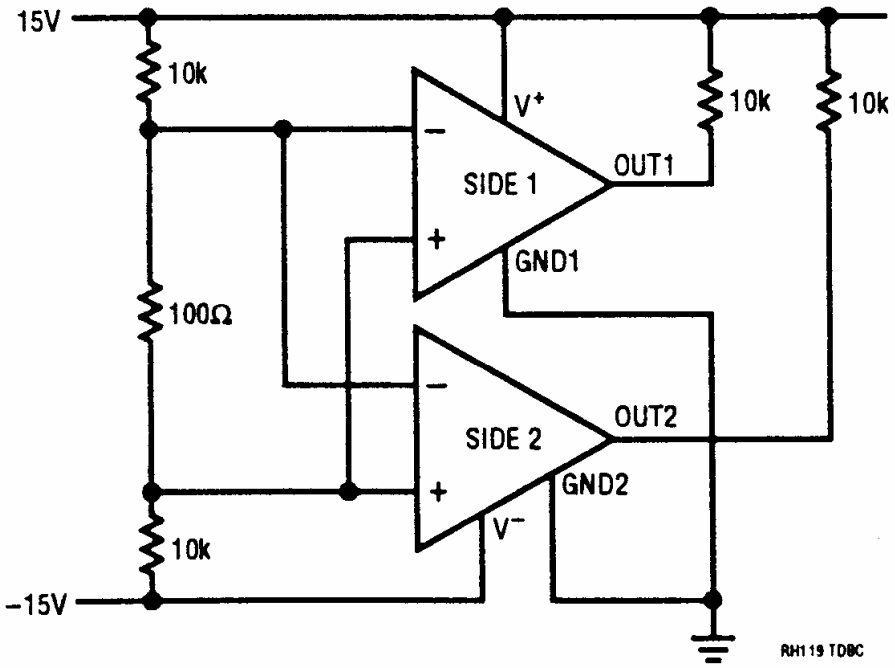


FIGURE 13

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION) NOTE 2

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_J = 25°C$ MIN	TYP	MAX	SUB-GROUP	$-55°C \le T_{AJ} \le 125°C$ MIN	TYP	MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage	$V_S = \pm15V$, $V_{CM} = 0V$				4	1					mV
			3							7	2,3	mV
CMRR	Common Mode Rejection Ratio			90			1					dB
I_{OS}	Input Offset Current		3			75	1			100	2,3	nA
I_B	Input Bias Current					500	1			1000	2,3	nA
A_V	Voltage Gain			10			4					V/mV
t_R	Response Time		4		80	200	4			200	5,6	ns
V_{SAT}	Saturation Voltage	$V_{IN} \le -5mV$, $I_O = 25mA$				1.5	1					V
		$V^+ \ge 4.5V$, $V^- = 0V$ $V_{IN} \le -6mV$, $I_{SINK} \le 3.2mA$ $T_A \ge 0°C$ $T_A \le 0°C$				0.4	1			0.4 0.6	2 3	V V
	Output Leakage Current	$V_{IN} \ge 5mV$, V_{OUT} to $V^- = 35V$				2	1			10	2,3	μA
	Input Voltage Range	$V_S = \pm15V$ $V^+ = 5V$, $V^- = 0V$		−12 1		12 3	1 1	−12 1		12 3	2,3 2,3	V V
	Differential Input Voltage					±5	1			±5	2.3	V
I_S	Supply Current	$V^+ = 5V$, $V^- = 0V$			4.3							mA
	Positive Supply Current	$V_S = \pm15V$				11.5	1					mA
	Negative Supply Current	$V_S = \pm15V$				4.5	1					mA

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION) NOTE 5

SYMBOL	PARAMETER	CONDITIONS	NOTES	10Krad(Si) MIN	MAX	20Krad(Si) MIN	MAX	50Krad(Si) MIN	MAX	100Krad(Si) MIN	MAX	200Krad(Si) MIN	MAX	UNITS
V_{OS}	Offset Voltage				4		4		4		4		8	mV
I_{OS}	Input Offset Current		3		75		100		150		300		500	nA
I_B	Input Bias Current		3		500		750		1000		1500		2000	nA
A_{VOL}	Large-Signal Voltage Gain			10		10		10		10		5		V/mV
V_{SAT}	Saturation Voltage	$V_{IN} \le -5mV$, $I_O = 25mA$			1.5		1.5		1.5		1.5		1.5	V
		$V^+ \ge 4.5V$, $V^- = 0V$ $V_{IN} \le -6mV$, $I_{SINK} \le 3.2mA$			0.4		0.4		0.4		0.4		0.4	V
CMRR	Common Mode Rejection Ratio			90		90		90		90		90		dB
I_S	Positive Supply Current	$V_S = \pm15V$			11.5		11.5		11.5		11.5		11.5	mA
	Negative Supply Current	$V_S = \pm15V$			4.5		4.5		4.5		4.5		4.5	mA
	Output Leakage Current	$V_{IN} \ge 5mV$, V_{OUT} to $V^- = 35V$			2		2		2		2		2	μA

SEE ELECTRICAL CHARACTERISTICS NOTES ON NEXT PAGE.

ELECTRICAL CHARACTERISTICS (NOTES)

Note 1: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

Note 2: Unless otherwise noted, supply voltage equals ±15V, V_{CM} = 0V and T_A = 25°C. The GND pin is grounded. Note that the maximum voltage allowed between the GND pin and V^+ is 18V. Do not tie the GND pin to V^- when the power supply voltage exceeds ±9V. The offset voltage, offset current and bias current specifications apply for all supply voltages between ±15V and 5V unless otherwise specified.

Note 3: The offset voltages and currents given are the maximum values required to drive the output within 1V of either supply with a 1mA load—thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 4: Response time specified for a 100mV input step with 5mV overdrive.

Note 5: V_S = ±15V, V_{CM} = 0V, T_A = 25°C unless otherwise noted.

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

T_A = 25°C, V_{CC} = ±15V

	ENDPOINT LIMIT		DELTA		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
V_{OS}	-4	+4	-1	1	mV
$+I_{IB}$	-0.1	+500	-100	100	nA
$-I_{IB}$	-0.1	+500	-100	100	nA

TABLE IV: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
FINAL ELECTRICAL TEST REQUIREMENTS (METHOD 5004)	1*, 2, 3, 4, 5, 6
GROUP A TEST REQUIREMENTS (METHOD 5005)	1, 2, 3, 4, 5, 6
GROUP B AND D FOR CLASS S ENDPOINT ELECTRICAL PARAMETERS (METHOD 5005)	1, 2, 3

*PDA APPLIES TO SUBGROUP 1.

PDA TEST NOTE: The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1 and delta rejects after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.