REVISION RECORD

REV	DESCRIPTION	DATE
0	INITIAL RELEASE	02/11/09
A	RH1185MK DICE/DWF DATA SHEET AMENDED. PAGE 11, PRE-IRRADIATION ELECTRICAL TEST LIMITS CHANGED REFERENCE VOLTAGE FROM -1.1V MIN, 1.1V MAX TO -2.344V MIN., -2.396V MAX, WITH A TYPICAL OF -2.37 V.	12/02/09
B	RH1185AMK DICE DATA SHEET CHANGED ON NOVEMBER 2011. THE FOLLOWING ARE THE COMPLETE AND CORRECT CHANGES. ALL PAGES: RH1185MK HAS BEEN CHANGED TO REFLECT RH1185AMK. PAGES 11 AND 12, REMOVED REF PIN SHUTDOWN CURRENT FROM TABLE I AND TABLE II ELECTRICAL CHARACTERISTICS.	01/19/12
C	Page 2, amended section 3.3, Special Handling of Dice, to more accurately describe our current procedures and requirements.	04/05/12
D	Page 13, Changed RH Canned Sample Table for Qualifying Dice Sales: Subgroup 6 Sample Size Series changed from 45 (3) to 65 (3). First note had the Sample Size Series from “15%” to “10%”.	07/02/13
E	**Updated Die Sales table on pg 13.**	

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13			
INDEX	REVISION	**E**	**E**	**E**	**E**	**E**	**E**	**E**	**E**	**E**	**E**	**E**	**E**	**E**			
REVISION	PAGE NO.																
INDEX	REVISION																

				LINEAR TECHNOLOGY CORPORATION MILPITAS, CALIFORNIA
	ORIG			
	DSGN			TITLE: **MICROCIRCUIT, LINEAR, RH1185AMK DICE NEGATIVE REGULATOR WITH ADJUSTABLE CURRENT LIMIT**
	ENGR			
	MFG			
	CM			
	QA			SIZE / CAGE CODE / DRAWING NUMBER / REV
	PROG			**64155** / **05-08-5232** / **E**
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:

FOR OFFICIAL USE ONLY

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-STD-883	Test Method and Procedures for Microcircuits
MIL-STD-1835	Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the **RH1185AMK**, DICE and Element Evaluation Test Samples, processed to space level manufacturing flow as specified herein.

3.2 Part Number: **RH1185AMKDice**

3.3 **Special Handling of Dice:** Rad Hard dice require special handling as compared to standard IC dice. Rad Hard dice are susceptible to surface damage due to the absence of silicon nitride passivation that is present on most standard dice. Silicon nitride protects the dice surface from scratches by its hard and dense properties. The passivation on Linear Technology's Rad Hard dice is silicon dioxide which is much "softer" than silicon nitride. During the visual and preparation for shipment, ESD safe Tweezers are used and only the edge of the die are touched.

LTC recommends that dice handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die in or out of the chip shipment tray (waffle pack), use an ESD-Safe-Plastic-tipped Bent Metal Vacuum Probe, preferably .020" OD x .010" ID (for use with tiny parts). The wand should be compatible with continuous air vacuums. The tip material should be static dissipative Delrin (or equivalent) plastic.

During die attach, care must be exercised to ensure no tweezers, or other equipment, touch the top of the dice.

3.4 The Absolute Maximum Ratings:

Input Voltage	35V
Input - Output Differential	30V
FB Voltage	7V
REF Voltage	7V
Output Voltage	30V
Output Reverse Voltage	2V
Operating Ambient Temperature Range	-55°C to 125°C

Operating Junction Temperature Range
- Control Section . . . . . -55°C to +150°C
- Power Transistor Section . . . . . -55°C to +175°C

Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

3.5 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.6 Outline Dimensions and Pad Functions: Dice outline dimensions, pad functions, and locations shall be specified in **Figure 1**.

3.7 Radiation Hardness Assurance (RHA):

3.7.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.7.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.7.3 Total dose bias circuit is specified in **Figure 2**.

3.8 Wafer (or Dice) Probe: Dice shall be 100% probed at Ta = +25°C to the limits shown in **Table I** herein. All reject dice shall be removed from the lot. This testing is normally performed prior to dicing the wafer into chips. Final specifications after assembly are sample tested during the element evaluation.

3.9 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Top side glassivation thickness shall be a **minimum of 4KÅ.**

3.10 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018. Copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

3.11 Traceability: Wafer Diffusion Lot and Wafer traceability shall be maintained through Quality Conformance Inspection.

4.0 QUALITY CONFORMANCE INSPECTION: Quality Conformance Inspection shall consist of the tests and inspections specified herein.

5.0 SAMPLE ELEMENT EVALUATION: A sample from **each wafer supplying dice** shall be assembled and subjected to element evaluation per **Table III** herein.

5.1 100 Percent Visual Inspection: All dice supplied to this specification shall be inspected in accordance with MIL-STD-883, Method 2010, Condition A. All reject dice shall be removed from the lot.

5.2 Electrical Performance Characteristics for Element Evaluation: The electrical performance characteristics shall be as specified in **Table I** and **Table II** herein.

5.3 Sample Testing: Each wafer supplying dice for delivery to this specification shall be subjected to element evaluation sample testing. No dice shall be delivered until all the lot sample testing has been performed and the results found to be acceptable unless the customer supplies a written approval for shipment prior to completion of wafer qualification as specified in this specification.

5.4 Part Marking of Element Evaluation Sample Includes**:**

5.4.1 LTC Logo

5.4.2 LTC Part Number

5.4.3 Date Code

5.4.4 Serial Number

5.4.5 ESD Identifier per MIL-PRF-38535, Appendix A

5.4.6 Diffusion Lot Number

5.4.7 Wafer Number

5.5 Burn-In Requirement: Burn-In circuit for TO3 package is specified in **Figure 3**.

5.6 Mechanical/Packaging Requirements: Case Outline and Dimensions are in accordance with **Figure 4.**

5.7 Terminal Connections: The terminal connections shall be as specified in **Figure 5.**

5.8 Lead Material and Finish: The lead material and finish shall be alloy 52 with hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

6.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

6.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

6.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with **Table III** herein.

6.3 Screening: Screening requirements shall be in accordance with **Table III** herein.

6.4 Source Inspection:

6.4.1 The manufacturer will coordinate Source Inspection at wafer lot acceptance and pre-seal internal visual.

6.4.2 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance, die visual, and final data review.

6.5 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

6.5.1 Lot Serial Number Sheets identifying all Canned Sample devices accepted through final inspection by serial number.

6.5.2 100% attributes (completed element evaluation traveler).

6.5.3 Element Evaluation variables data, including Burn-In and Op Life

6.5.4 SEM photographs (3.10 herein)

6.5.5 Wafer Lot Acceptance Report (3.9 herein)

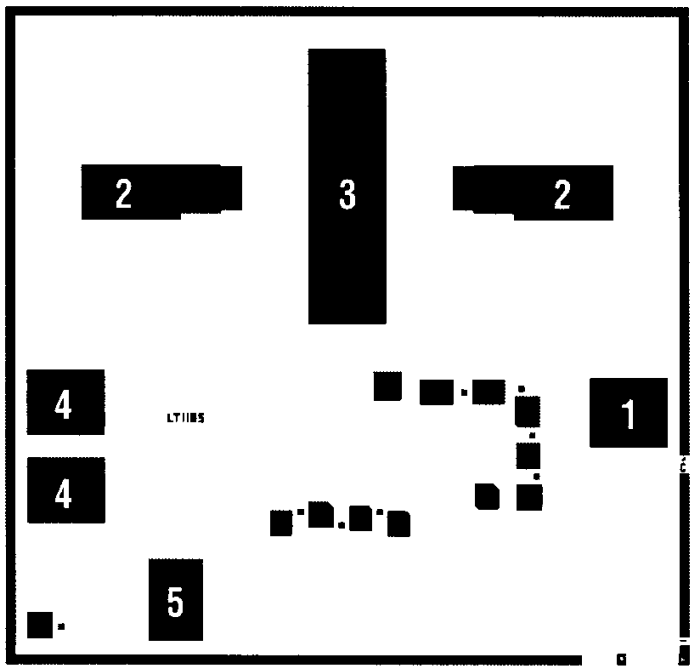
6.5.6 A copy of outside test laboratory radiation report if ordered

6.5.7 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 6.5.1 and 6.5.7 will be delivered as a minimum, with each shipment.

7.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All dice shall be packaged in multicavity containers composed of conductive, anti-static, or static dissipative material with an external conductive field shielding barrier.

DICE OUTLINE DIMENSIONS AND PAD FUNCTIONS



PAD FUNCTION

1. REF
2. V_{IN}
3. V_{OUT}
4. GND
5. FB

110mils × 116mils
Backside metal: Alloyed Gold Layer
Backside Potential: V_{IN} Pads 2

FIGURE 1

TOTAL DOSE BIAS CIRCUIT

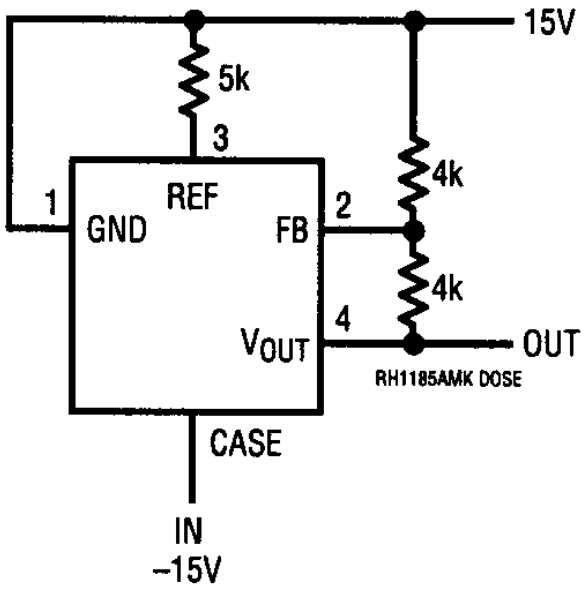
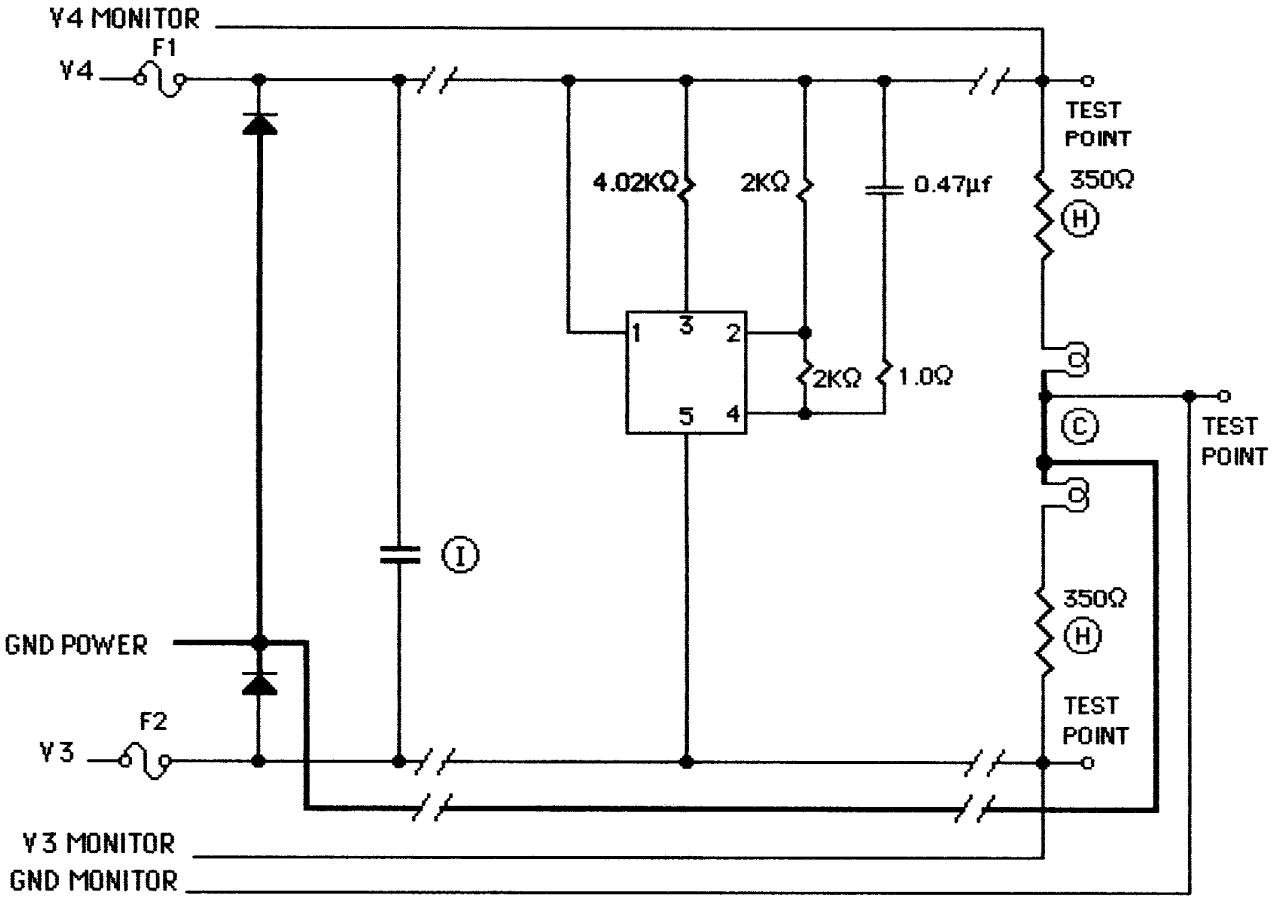


FIGURE 2

BURN-IN CIRCUIT

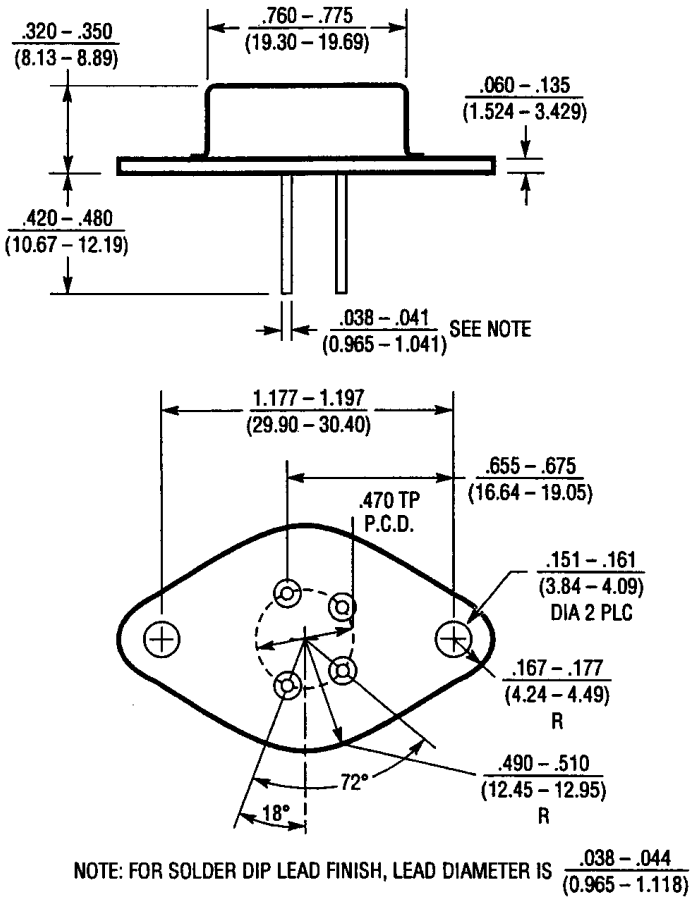


NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 163°C maximum.
3. Ta = 150 °C.
4. Burn-in voltages: V4 = +15V to +16.5V
   V3 = -15V to -16.5V

FIGURE 3

TO3, 4 LEADS, CASE OUTLINE



θja = +35°C/W
θjc = +3°C/W

FIGURE 4

TERMINAL CONNECTIONS

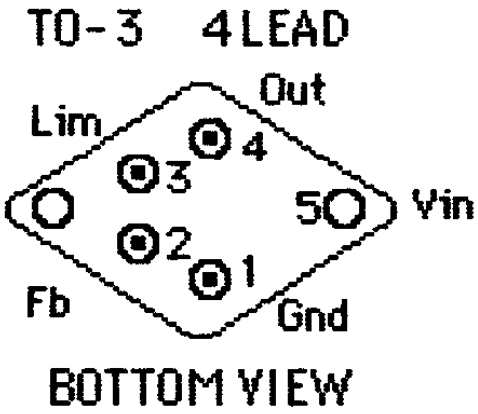


FIGURE 5

TABLE I DICE ELECTRICAL CHARACTERISTICS – Element Evaluation

V_{IN} = 7.4V, V_{OUT} = 5V, I_{OUT} = 1mA, R_{LIM} = 4.02k, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Voltage (at FB Pin, Note 2)	$V_{IN} - V_{OUT}$ = 5V, $V_{OUT} = V_{REF}$	–2.344	–2.37	–2.396	V
Feedback Pin Bias Current	$V_{OUT} = V_{REF}$			2	µA
Dropout Voltage (Note 3)	I_{OUT} = 0.5A, V_{OUT} = 5V I_{OUT} = 3A, V_{OUT} = 5V			0.4 1.05	V V
Line Regulation (Note 6)	$V_{IN} - V_{OUT}$ = 1V to 20V, V_{OUT} = 5V			0.01	%/V
Minimum Input Voltage (Note 4)	I_{OUT} = 1A, $V_{OUT} = V_{REF}$			4.5	V
Internal Current Limit (Note 8)	$V_{IN} - V_{OUT}$ = 1.5V $V_{IN} - V_{OUT}$ = 20V $V_{IN} - V_{OUT}$ = 30V	3.3 1 0.2		4.2 2.6 1	A A A
External Current Limit (Note 7)	R_{LIM} = 5k, V_{OUT} = 1V R_{LIM} = 15k, V_{OUT} = 1V	2.7 0.9		3.3 1.1	A A
Quiescent Supply Current (Note 5)	I_{OUT} = 5mA, $V_{OUT} = V_{REF}$, 4V ≤ V_{IN} ≤ 25V			3.5	mA

Note 1: Dice are probe tested at 25°C to the limits shown except for high current tests. Dice are tested under low current conditions which assure full load current specifications when assembled in packaging systems approved by Linear Technology. For absolute maximum ratings, typical specifications, performance curves and finished product specifications, please refer to the standard product RH data sheet.

Note 2: Testing is done using a pulsed low duty cycle technique. See thermal regulation specifications in the LT1185 data sheet for output changes due to heating effects.

Note 3: Dropout voltage is tested by reducing input voltage until the output drops 1% below its nominal value. Tests are done at 0.5A and 3A. The power transistor looks basically like a pure resistance in this range so that minimum differential at any intermediate current can be calculated by interpolation; $V_{DROPOUT} = 0.25V + 0.25\Omega \bullet I_{OUT}$. For load current other than 0.5A and 3.0A, see the graph in the LT1185 data sheet.

Note 4: Minimum input voltage is limited by base emitter voltage drive of the power transistor section, not saturation as measured in Note 3. For output voltages below 4V, minimum input voltage specification may limit dropout voltage before transistor saturation limit.

Note 5: Supply current is measured on the ground pin, and does not include load current, R_{LIM}, or output divider current.

Note 6: Line regulation is measured on a pulse basis with a pulse width of ≈2ms to minimize heating. DC regulation will be affected by thermal regulation and temperature coefficient of the reference. See the Applications Information section of the LT1185 data sheet for details.

Note 7: External current limit is programmed with a resistor from REF pin to GND pin. The value is $15K \bullet A/I_{LIMIT}$.

Note 8: For $V_{IN} - V_{OUT}$ = 1.5V, V_{IN} = 5V and V_{OUT} = 3.5V. For all other current limit tests V_{OUT} = 1V.

TABLE II ELECTRICAL CHARACTERISTICS – Post-Irradiation

PARAMETER AND CONDITONS	10KRAD(Si) MIN	10KRAD(Si) MAX	20KRAD(Si) MIN	20KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	200KRAD(Si) MIN	200KRAD(Si) MAX	UNITS
Reference Voltage Tolerance $V_{IN} - V_{OUT} = 5V$, $V_{OUT} = V_{REF}$	–1.2	1.2	–1.2	1.2	–1.5	1.5	–1.5	1.5	–2	2	%
Reference Voltage Tolerance $V_{IN} - V_{OUT} = 1.2V$ to $V_{IN} = 30V$, $1mA \le I_{OUT} \le 3A$, $P_D \le 25W$ (Note 6), $V_{OUT} = 5V$, $T_{MIN} \le T_J \le T_{MAX}$ (Note 9)	–3	3	–3	3	–3.2	3.2	–3.5	3.5	–4	4	%
Feedback PIn Bias Current, $V_{OUT} = V_{REF}$		2		2		2.5		3		3	µA
Dropout Voltage (Note 3) $I_{OUT} = 0.5A$, $V_{OUT} = 5V$ $I_{OUT} = 3A$, $V_{OUT} = 5V$		0.4 1		0.4 1		0.4 1		0.425 1.05		0.45 1.1	V V
Load Regulation (Note 7) $I_{OUT} = 5mA$ to $3A$ $V_{IN} - V_{OUT} = 1.5V$ to $10V$, $V_{OUT} = 5V$		0.3		0.4		0.5		0.8		1	%
Line Regulation, Absolute Value (Note 7) $V_{IN} - V_{OUT} = 1V$ to $20V$, $V_{OUT} = 5V$		0.01		0.01		0.01		0.02		0.05	%/V
Minimum Input Voltage (Note 4) $I_{OUT} = 1A$, $V_{OUT} = V_{REF}$ $I_{OUT} = 3A$, $V_{OUT} = V_{REF}$		3.9 4.4		3.9 4.4		3.9 4.4		4 4.5		4 4.5	V V
Internal Current Limit (Note 12) $1.5V \le V_{IN} - V_{OUT} \le 10V$ $V_{IN} - V_{OUT} = 15V$ $V_{IN} - V_{OUT} = 20V$ $V_{IN} - V_{OUT} = 30V$	3.3 2 1 0.2	4.3 4.3 2.7 1	3.3 2 1 0.2	4.3 4.3 2.75 1.15	3.3 2 1 0.2	4.4 4.35 2.85 1.3	3.3 2 1 0.2	4.55 4.5 3.1 1.6	3.3 2 1 0.2	4.75 4.7 3.3 2	A A A A
External Current Limit (Note 11) $R_{LIM} = 5k$ $R_{LIM} = 15k$	2.7 0.9	3.3 1.1	2.7 0.9	3.4 1.25	2.7 0.9	3.5 1.4	2.7 0.9	3.7 1.6	2.7 0.9	3.9 1.9	A A
Quiescent Supply Current $I_{OUT} = 5mA$, $V_{OUT} = V_{REF}$, $4V \le V_{IN} \le 25V$		3.5		3.5		3.5		3.5		3.5	mA
Supply Current Change With Load $V_{IN} - V_{OUT} = V_{SAT}$ $V_{IN} - V_{OUT} \ge 2V$		25 15		27 16		30 18		35 21		45 27	mA/A mA/A

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Reference voltage is guaranteed both at nominal conditions (no load, 25°C) and at worst-case conditions of load, line, power and temperature.

Note 3: Dropout voltage is tested by reducing input voltage until the output drops 1% below its nominal value. Tests are done at 0.5A and 3A. The power transistor looks basically like a pure resistance in this range so that minimum differential at any intermediate current can be calculated by interpolation; $V_{DROPOUT} = 0.25V + 0.25\Omega \bullet I_{OUT}$. For load current other than 0.5A and 3.0A, see graph in LT1185 data sheet.

Note 4: "Minimum input voltage" is limited by base emitter voltage drive of the power transistor section, not saturation as measured in Note 3. For output voltages below 4V, "minimum input voltage" specification may limit dropout voltage before transistor saturation limitation.

Note 5: Supply current is measured on the ground pin, and does not include load current, R_{LIM}, or output divider current.

Note 6: The 25W power level is guaranteed for an input-output voltage of 8.3V to 17V. At lower voltages the 3A limit applies, and at higher voltages the internal power limiting may restrict regulator power below 25W. See graph of Internal Current Limit in LT1185 data sheet.

Note 7: Line and load regulation are measured on a pulse basis with a pulse width of ≈2ms, to minimize heating. DC regulation will be affected by thermal regulation and temperature coefficient of the reference. See the Applications Information section of LT1185 data sheet for details.

Note 8: Guaranteed by design and correlation to other tests, but not tested.

Note 9: $T_{JMIN} = -55°C$ for the RH1185AMK. Power transistor area and control circuit area have different maximum junction temperatures. Control area limit is $T_{JMAX} = 150°C$ for the RH1185AMK. Power area limit is 175°C for RH1185AMK.

Note 10: V_{SAT} is the maximum specified dropout voltage; $0.25V + 0.25\Omega \bullet I_{OUT}$.

Note 11: Current limit is programmed with a resistor from REF pin to GND pin. The value is 15k • A/I-limit.

Note 12: For $V_{IN} - V_{OUT} = 1.5V$, $V_{IN} = 5V$ and $V_{OUT} = 3.5V$. For all other current limit tests, $V_{OUT} = 1.0V$

TABLE III RH ELEMENT EVALUATION TABLE QUALIFICATION OF DICE SALES

LINEAR TECHNOLOGY

RH CANNED SAMPLE TABLE FOR QUALIFYING DICE SALES

SUBGROUP	CLASS K/S	CLASS V	CLASS H/B	OPERATION	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY (ACCEPT NUMBER)
1	X	X		SEM	2018	N/A	REF. METHOD 2018 FOR S/S
2	X	X	X	ELEMENT ELECTRICAL (WAFER SORT @ 25ºC)			100%
3	X	X	X	ELEMENT VISUAL (2nd OP)	2010	A	100%
4	X	X	X	INTERNAL VISUAL (3rd OP)	2010	A	ASSEMBLED PARTS ONLY
	X	X		DIE SHEAR MONITOR	2019		
	X	X		BOND PULL MONITOR	2011		
5	X	X		STABILIZATION BAKE	1008	C	ASSEMBLED PARTS ONLY
	X	X		TEMPERATURE CYCLE	1010	C	
	X	X		CONSTANT ACCELERATION	2001	E	
	X	X		FINE LEAK	1014	A	
	X	X		GROSS LEAK	1014	C	
6	X	X		FIRST ROOM ELECTRICAL - READ & RECORD (REPLACE ANY ASSEMBLY-RELATED REJECTS)			45(0)
	X	X		PRE BURN-IN ELECT. READ & RECORD @ +125ºC or +150ºC, -55ºC			
	X	X		BURN-IN: +125ºC/240 hrs. or +150ºC/120 hrs.	1015	+ 125ºc MINIMUM 240 HOURS	
	X	X		POST BURN-IN ELECT. READ & RECORD @ 25ºC			
	X	X		POST BURN-IN ELECT. READ & RECORD @ +125ºC or +150ºC, -55ºC			
		X		TOTAL IRRADIATION DOSE	1019	A	
	X	X		PRE OP-LIFE ELECTRICAL @ 25ºC READ & RECORD			
	X	X		OPERATING LIFE: +125ºC/1000 hrs. or +150ºC/500 hrs.	1005	+ 125ºc MINIMUM 1000 HOURS	
	X	X		POST OP-LIFE ELECT. (R & R @ 25ºC, +125ºC OR +150ºC, -55ºC			
7	X	X	X	WIRE BOND EVALUATION	2011		15(0) OR 25(1) - # of wires

NOTE: LTC is not qualified to process to MIL-PRF-38534. This is an LTC imposed element evaluation that follows MIL-STD-883 test methods and conditions. Please note the quantity and accept number from Sample Size Series of 5%, accept on 0, and note that the actual sample and accept number does not begin until Subgroup 6 OP-LIFE.

NOTE: Tests within Subgroup 5 may be performed in any sequence.

NOTE: LTC's radiation tolerance (RH) die has a topside glassivation thickness of 4KA minimum.

NOTE: Sample sizes on the travelers may be larger than that indicated in the above table; however, the larger sample size is to accommodate extra units for replacement devices in the event of equipment or operator error and for assembly related rejects in Subgroup 6, and for Wire Bond Evaluation, Surgroup 7. The larger sample size is at all times kept segregated and, if used for qualification, has all the required processing imposed.