REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	06/12/96
A	• PAGE 2, ADDED PARAGRAPHS 3.2.1 AND 3.2.2. PARAGRAPH 3.3.b, ADDED "(SEE PARAGRAPH 3.2)". • PAGE 3, ADDED PARAGRAPHS 3.8.1 AND 3.8.3. PARAGRAPH 3.12, WAFER LOT ACCEPTANCE REDEFINED. • PAGE 4, PARAGRAPH 4.4.2, GROUP B INSPECTION, REDEFINED. PARAGRAPH 4.4.3, GROUP D INSPECTION, REDEFINED. PARAGRAPH 4.5, SOURCE INSPECTION, REDEFINED. • PAGE 6, ADDED TO FIGURE 1, TO39 CASE OUTLINE θja AND θjc. • PAGE 7, ADDED TO FIGURE 2, TO3 CASE OUTLINE θja AND θjc.	11/27/97
B	PAGE 4, AMENDED PARAGRAPHS 4.1 AND 4.1.1 TAKING EXCEPTION TO ANALYSIS OF CATASTROPHIC FAILURES.	02/23/98
C	PAGE 6 AND 7 FIGURE 1 AND 2 CHANGED θja AND θjc.	09/29/99
D	• PAGE 2: PARAGRAPHS 3.2.1, 3.2.2, FIGURES 1, 2 REMOVED. • PAGE 3: PARAGRAPHS 3.7 CHANGED VERBIAGE FROM "SPECIFIED IN TABLE III" TO "AND AS SPECIFIED IN TABLE III HEREIN", LINE 2. PARAGRAPH 3.9, ADDED "HEREIN" AFTER TABLE II, LINE 2. • PAGE 4: PARAGRAPH 4.3, ADDED "HEREIN" AFTER TABLE III", LINE 2. 4.4.1, ADDED "HEREIN" AFTER TABLE III", LINE 2. 4.4.2.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IIa OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IIa IN MIL-STD-883". PARAGRAPH 4.4.3.2 CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IV OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IV IN MIL-STD-883".	11/17/99
E	• CONVERSION FROM WORD PERFECT TO MICROSOFT WORD. • PAGE 1: CORRECTED CAGE CODE # FROM 94155 TO 64155. • PAGE 2: AN ADDITIONAL REVISION RECORD PAGE WAS INSTALLED. • PAGE 3: PARAGRAPH 3.2.1 ADDED "OPTION 1" AND PARAGRAPH 3.2.2, ADDED "OPTION 2". CONTINUED ON NEXT PAGE…..	05/30/02

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
INDEX	REVISION	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K		

				LINEAR TECHNOLOGY CORPORATION MILPITAS, CALIFORNIA	
	ORIG				
	DSGN			TITLE:	
	ENGR			**MICROCIRCUIT, LINEAR, RH117, POSITIVE ADJUSTABLE REGULATOR**	
	MFG				
	CM				
	QA			SIZE	CAGE CODE / DRAWING NUMBER / REV
	PROG				**64155** / **05-08-5024** / **K**
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:	

FOR OFFICIAL USE ONLY

REVISION RECORD		
REV	DESCRIPTION	DATE
	• PAGE 4: PARAGRAPH 3.4 , MOVED PARAGRAPH AND NOTES FROM PAGE 3. PARAGRAPH 3.6, TABLE IA CHANGED TO TABLE II. PARAGRAPH 3.7, TABLE III CHANGED TO TABLE IV. PARAGRAPH 3.9, TABLE II CHANGED TO TABLE III. PARAGRAPH 3.11.1 WAS CHANGED FROM "…dosage rate of approximately 20 Rads per second" TO "…dosage rate of less than or equal to 10 Rads per second". • PAGE 5: PARAGRAPHS 4.1 THROUGH 4.4.2 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. PARAGRAPHS 4.4.2.1 THROUGH 4.4.3 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. PARAGRAPH 4.4.3.1 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. • PAGE 6: PARAGRAPHS 4.6.2 THROUGH 4.6.4 WERE RE-WRITTEN TO CLARIFY DATA PROVIDED AND DATA AVAILABLE. PARAGRAPH 4.6.10 NOTE, ADDED FURTHER EXPLANATION OF MINIMUM DELIVERED DATA. • PAGES 7 THROUGH 12, ALL FIGURE TITLES CHANGED TO HAVE DEVICE OPTIONS AND PACKAGE TYPES AT TOP OF PAGE, AND HAVE FIGURES 1 - 7 AT BOTTOM OF PAGE. • PAGE 13, TABLE IA WAS CHANGED TO TABLE II • PAGE 14, TABLE II CHANGED TO TABLE III, TABLE III CHANGED TO TABLE IV.	
F	• ADDED "≤" CORRECTIONS TO CONDITIONS IN TABLES I AND II DUE TO DATASHEET TYPOS. ADDED PAGE 15.	06/24/02
G	• PAGE 4: CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC.	03/15/05
H	• PAGE 5, CHANGED IN BOTH PARAGRAPHS 4.2, 4.3 IN CONJUNCTION TO 3.3 CHANGED TO 3.4 AND PARAGRAPH 4.3 CHANGED 3.1.1 TO 3.1 AND 3.2.1 TO 3.1.1	03/07/08
J	• PAGE 4, PARAGRAPH 3.11.1 CHANGED VERBIAGE AND PARAGRAPH 3.10.3 CHANGED "ALLOY 42" TO "ALLOY 52" REQUIREMENT ON TO3 PACKAGE.	04/30/08
K	• **PAGE 5, PARAGRAPH 4.4.2 CHANGED VERBIAGE.** • **PAGE 8 FIGURE 2 NOTE 2 ADDED TO LEAD THICKNESS.**	**07/11/08**

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-STD-883	Test Method and Procedures for Microcircuits
MIL-STD-1835	Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH117 Positive Adjustable Regulator, processed to space level manufacturing flow.

3.2 Part Number:

3.2.1 Option 1 – RH117H (TO39 METAL CAN, 3 LEADS)

3.2.2 Option 2 – RH117K (TO3 METAL CAN, 2 LEADS)

3.3 Part Marking Includes:

a. LTC Logo

b. LTC Part Number (See Paragraph 3.2)

c. Date Code

d. Serial Number

e. ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings:

Power Dissipation	Internally Limited
Input to Output Voltage Differential	40V
Operating Junction Temperature Range	-55°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Sec)	+300°C

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 1.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and Table II.

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in Table IV herein.

3.8 Burn-In Requirement:

3.8.1 Option 1 (TO39): Static Burn-In, Figure 5

3.8.2 Option 2 (TO3): Static Burn-In, Figure 6

3.9 Delta Limit Requirement: Delta limit parameters are specified in Table III herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1 and Figure 2.

3.10.2 Terminal Connections: The terminal connections shall be as specified in Figure 3 and Figure 4.

3.10.3 Lead Material and Finish: The lead material and finish shall be Kovar for device option 1 and Alloy 52 for device option 2, with hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

3.11 Radiation Hardness Assurance (RHA):

3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019Condition A as a guideline.

3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.11.3 Total dose bias circuit is specified in Figure 7.

3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.

3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1, and 3.4 of the test method. Electrical testing shall be as specified in Table IV herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in Table IV herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroups 1-4 plus 6 are performed on every assembly lot, and Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1

Group B, Subgroup 2c = 10%	Group B, Subgroup 5 = *5% (*per wafer or inspection lot whichever is the larger quantity)
Group B, Subgroup 3 = 10%	
Group B, Subgroup 4 = 5%	Group B, Subgroup 6 = 15%

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Source Inspection:

4.5.1 The manufacturer will coordinate Source Inspection at wafer lot acceptance and pre-seal internal visual.

4.5.2 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance and final data review.

4.6 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.6.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.6.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.6.3 Burn-In Variables Data and Deltas (if applicable)

4.6.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.6.5 Generic Group D data (4.4.3 herein)

4.6.6 SEM photographs (3.13 herein)

4.6.7 Wafer Lot Acceptance Report (3.13 herein)

4.6.8 X-Ray Negatives and Radiographic Report

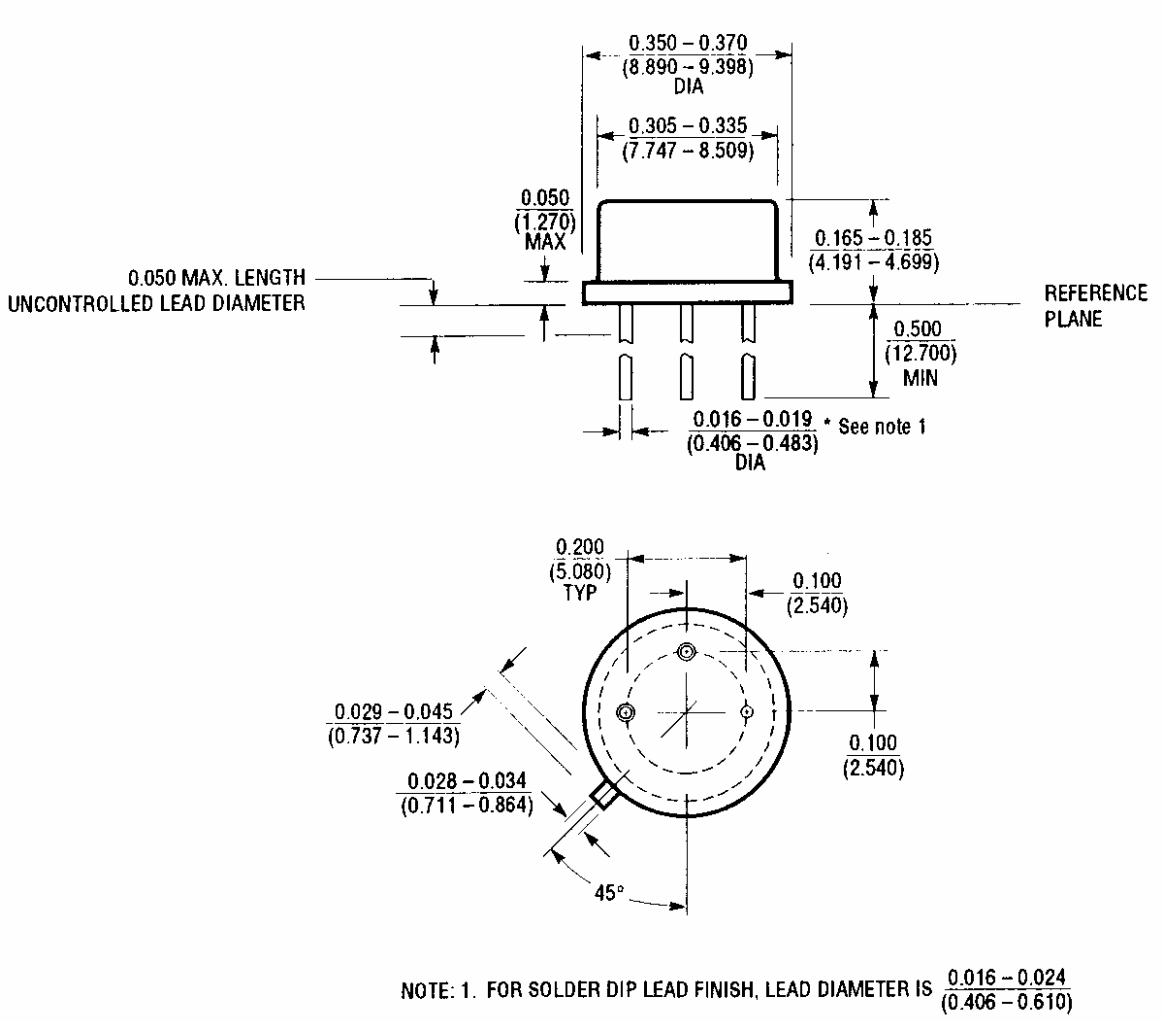
4.6.9 A copy of outside test laboratory radiation report if ordered

4.6.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 4.6.1 and 4.6.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as "No Charge Data".

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

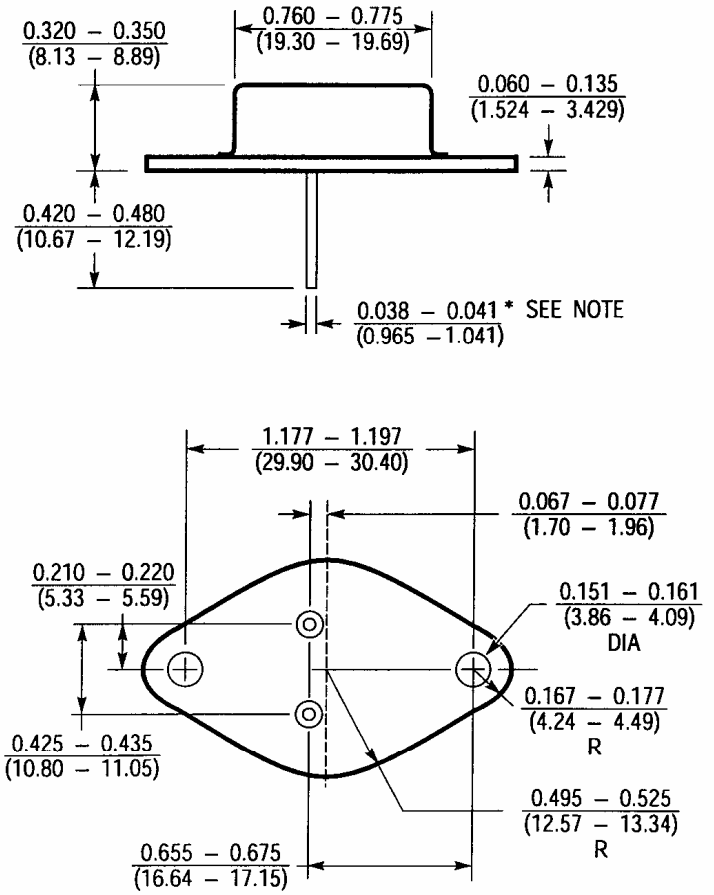
DEVICE OPTION # 1
(H) TO39 METAL CAN / 3 LEADS CASE OUTLINE



θja = +150°C/W
θjc = +15°C/W

FIGURE 1

DEVICE OPTION # 2
(K) TO3 METAL CAN / 2 LEADS CASE OUTLINE



NOTE: FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.038 – 0.044 (0.965 – 1.118)

θja = +35°C/W
θjc = +3°C/W

FIGURE 2

TERMINAL CONNECTIONS

DEVICE OPTION #1, TO39 / 3 LEAD METAL CAN

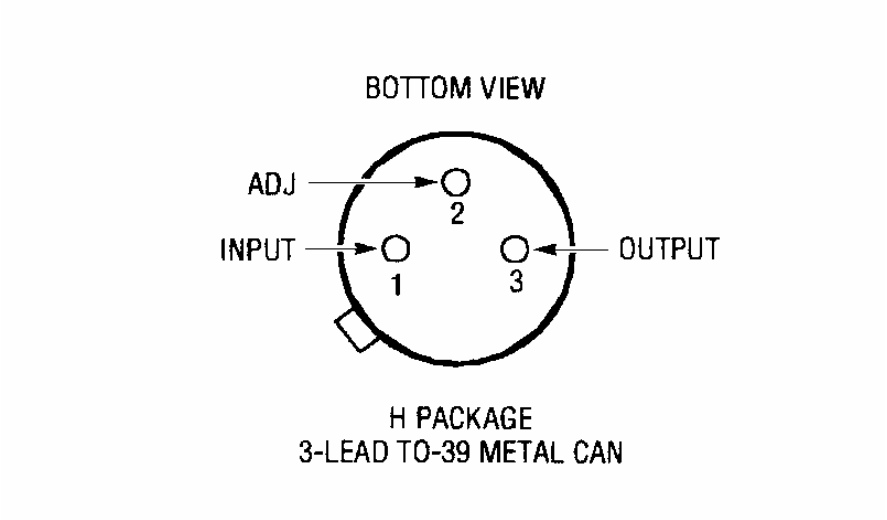


FIGURE 3

DEVICE OPTION #2, TO3 / 2 LEADS

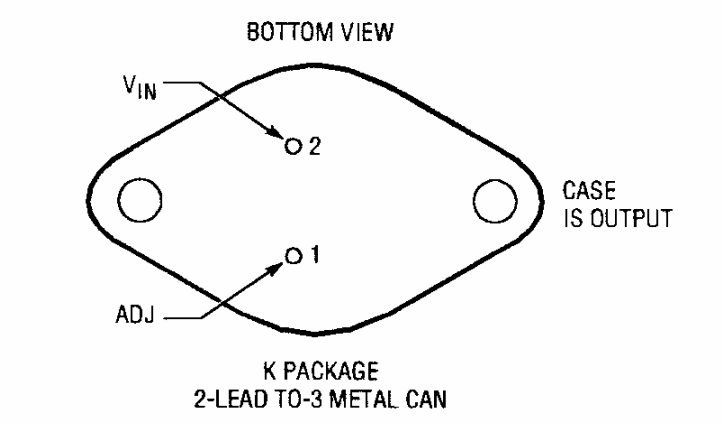
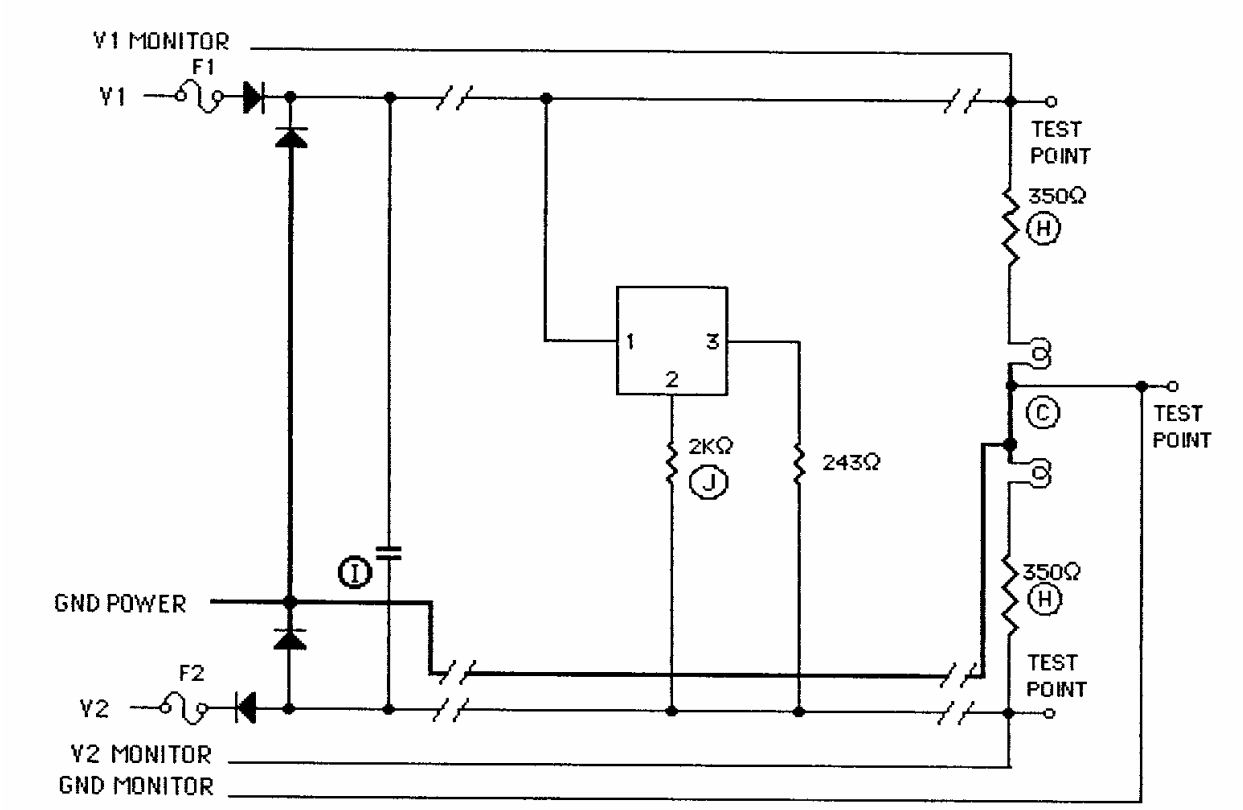


FIGURE 4

STATIC BURN-IN CIRCUIT
OPTION 1, T039 METAL CAN / 3 LEADS



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 148°C maximum at 125°C ambient.
3. Burn-in Voltages: V1 = +20V to +22V
   V2 = -20V to -22V

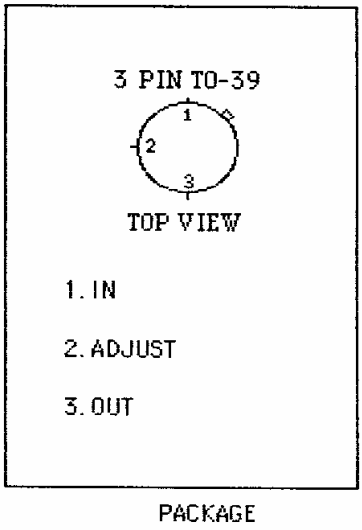
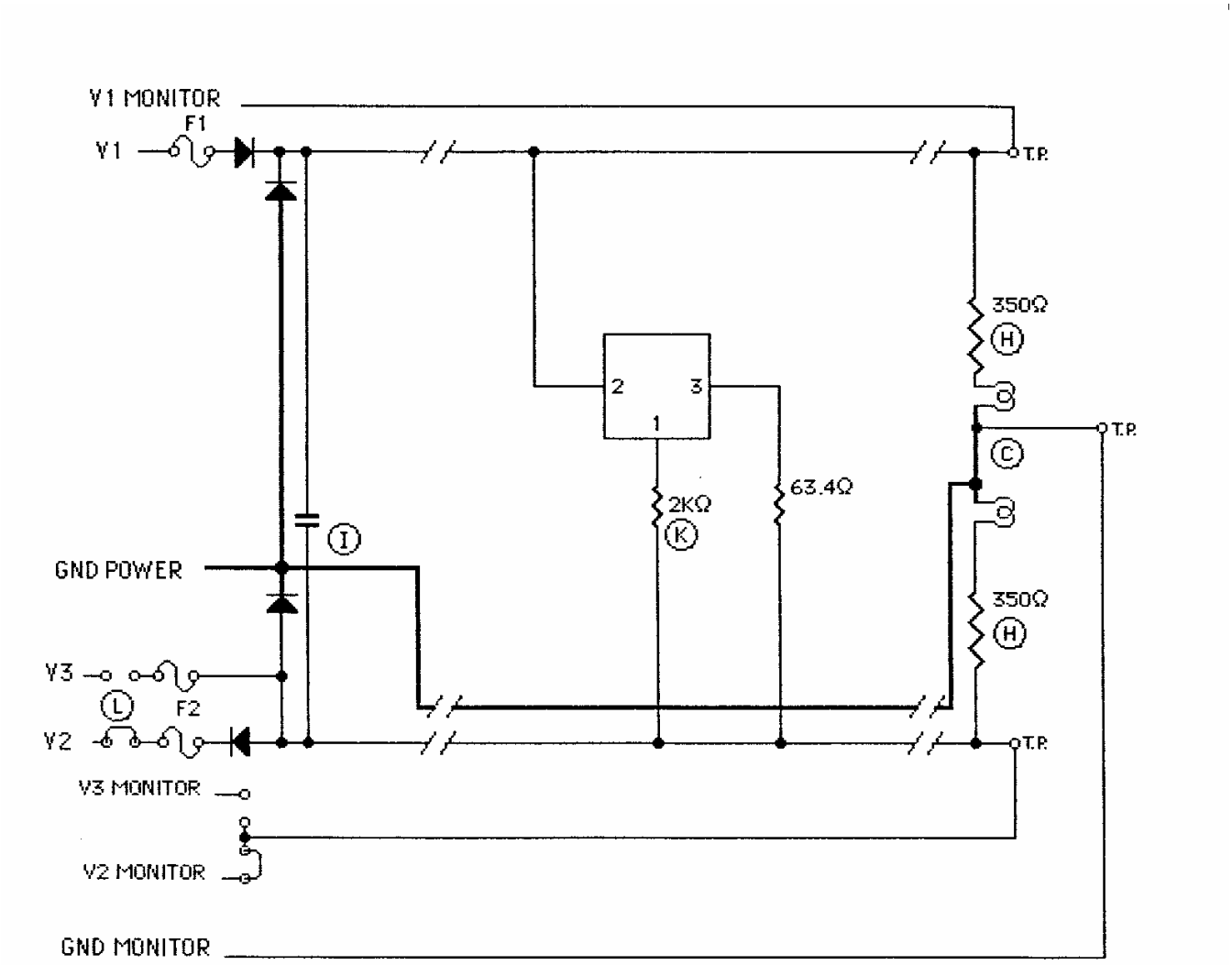


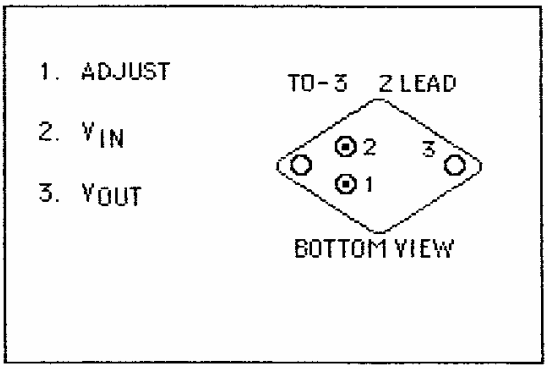
FIGURE 5

STATIC BURN-IN CIRCUIT
OPTION #2, TO3 / 2 LEADS



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 150°C maximum at 125°C
3. Burn-in Voltages: V1 = +20V to +22V
   V2 = -20V to -22V



PACKAGE AND PINOUT

FIGURE 6

TOTAL DOSE BIAS CIRCUIT

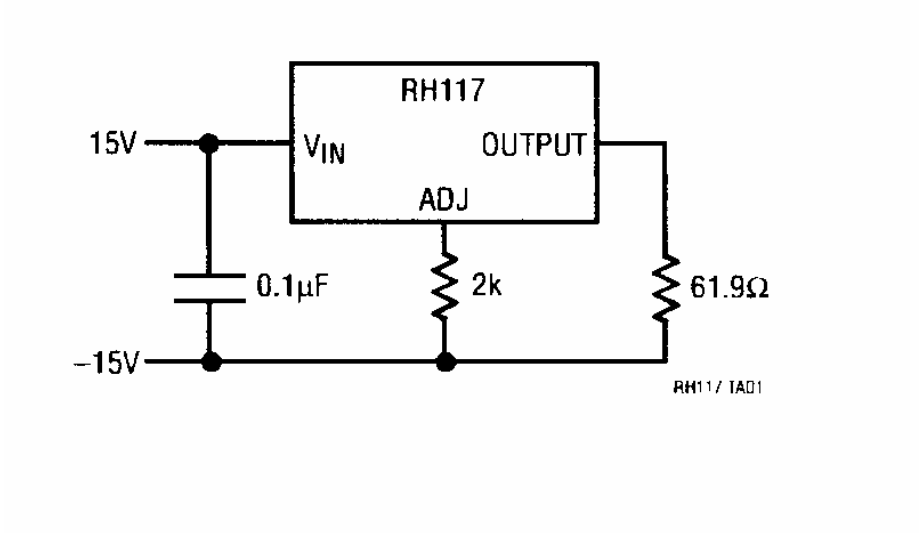


FIGURE 7

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION) NOTE 1

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_J = 25°C$ MIN	TYP	MAX	SUB-GROUP	$-55°C \le T_J \le 150°C$ MIN	TYP	MAX	SUB-GROUP	UNITS
V_{REF}	Reference Voltage	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $10mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$		1.20		1.30	1	1.20		1.30	2,3	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $I_{OUT} = 10mA$	2			0.02	1			0.05	2,3	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \le I_{OUT} \le I_{MAX}$, $V_{OUT} \le 5V$	2			15	1			50	2,3	mV
		$10mA \le I_{OUT} \le I_{MAX}$, $V_{OUT} \ge 5V$	2			0.3	1			1	2,3	%
	Thermal Regulation	20ms Pulse				0.07	1					%/W
	Ripple Rejection	$V_{OUT} = 10V$, f = 120Hz, $C_{ADJ} = 0$			65				65			dB
		$V_{OUT} = 10V$, f = 120Hz, $C_{ADJ} = 10\mu F$	3	66				66				dB
I_{ADJ}	Adjust Pin Current					100	1			100	2,3	µA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \le I_{OUT} \le I_{MAX}$				5	1			5	2,3	µA
		$2.5V \le (V_{IN} - V_{OUT}) \le 40V$, $I_{OUT} = 10mA$				5	1			5	2,3	µA
I_{MIN}	Minimum Load Current	$(V_{IN} - V_{OUT}) = 40V$				5	1			5	2,3	mA
	Current Limit	$(V_{IN} - V_{OUT}) \le 15V$ H Package		0.5			1	0.5			2,3	A
		K Package		1.5			1	1.5			2,3	A
		$(V_{IN} - V_{OUT}) = 40V$ H Package		0.15			1					A
		K Package		0.30			1					A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability	$-55°C \le T_J \le 150°C$							1			%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125°C$	3							1		%
e_n	RMS Output Noise	$10Hz \le f \le 10kHz$			0.001							%
θ_{JC}	Thermal Resistance (Junction to Case)	H Package	3			15						°C/W
		K Package	3			3						°C/W

NOTE: TABLE II ELECTRICAL CHARACTERISTICS (POST-IRRADIATION) AND NOTES FOR BOTH TABLE I AND TABLE II ARE CONTINUED ON PAGE 13.

TABLE II ELECTRICAL CHARACTERISTICS (POSTIRRADIATION) (Note 4)

T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD(Si) MIN	10KRAD(Si) MAX	20KRAD(Si) MIN	20KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	UNITS
V_{REF}	Reference Voltage	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $10mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$		1.20	1.30	1.20	1.30	1.20	1.30	1.20	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 40V$, I_{OUT} = 10mA	2		0.02		0.02		0.02		0.03	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \le I_{OUT} \le I_{MAX}$, $V_{OUT} \le 5V$	2		36		42		48		60	mV
		$10mA \le I_{OUT} \le I_{MAX}$, $V_{OUT} \ge 5V$	2		0.72		0.84		0.96		1.20	%
I_{ADJ}	Adjust Pin Current				100		100		100		100	µA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \le I_{OUT} \le I_{MAX}$			5		5		5		5	µA
		$3V \le (V_{IN} - V_{OUT}) \le 40V$, I_{OUT} = 10mA			5		5		5		5	µA
I_{MIN}	Minimum Load Current	$(V_{IN} - V_{OUT}) = 40V$			5		5		5		5	mA
	Current Limit	$(V_{IN} - V_{OUT}) \le 15V$ H Package		0.5		0.5		0.5		0.5		A
		K Package		1.5		1.5		1.5		1.5		A
		$(V_{IN} - V_{OUT}) = 40V$ H Package		0.15		0.15		0.15		0.15		A
		K Package		0.30		0.30		0.30		0.30		A

Note 1: Unless otherwise specified, these specifications apply for $V_{IN} - V_{OUT}$ = 5V; and I_{OUT} = 0.1A for the H package (TO-39) and I_{OUT} = 0.5A for the K package (TO-3) package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and 20W for the TO-3. I_{MAX} is 0.5A for the TO-39 and 1.5A for the TO-3.

Note 2: Regulation is measured at a constant junction temperature using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 3: Guaranteed by design, characterization or correlation to other tested parameters.

Note 4: T_J = 25°C unless otherwise noted.

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

T_J = 25°C

	ENDPOINT LIMIT		DELTA		
PARAMETER	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
V_{REF}	-1.20	-1.30	-0.010	0.010	V
I_{ADJ}		100	-10	10	µA
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	-9.62	9.62	-4.0	4.0	mV

TABLE IV: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
FINAL ELECTRICAL TEST REQUIREMENTS (METHOD 5004)	1*, 2, 3
GROUP A TEST REQUIREMENTS (METHOD 5005)	1, 2, 3
GROUP B AND D FOR CLASS S ENDPOINT ELECTRICAL PARAMETERS (METHOD 5005)	1, 2, 3

***PDA APPLIES TO SUBGROUP 1.**

PDA TEST NOTE: The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1 and delta rejects after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

LINEAR TECHNOLOGY CORPORATION

DOCUMENT TITLE: MICROCIRCUIT, LINEAR, RH117, POSITIVE ADJUSTABLE REGULATOR
DOCUMENT NUMBER: 05-08-5024

REV & APPROVAL	ECN No. & ISSUE DATE	CHANGE
0	122530 (06-12-96)	1. TO INITIATE
A	125878 (9-25-96)	1. CORRECTED TYPO ON PARA. 3.10.3, PAGE 3 2. DELETED PARAS. 3.12.1 AND 3.12.2; INCORPORATED 3.12.1 IN PARA. 3.12, PAGE 3
B	141343 (12-05-97)	1. PAGE 2, ADD PARAGRAPHS 3.2.1 & 3.2.2 2. PAGE 3, ADD PARAGRAPHS 3.8.1 & 3.8.2 3. PAGE 4, PARAGRAPH 4.4.2,GROUP B INSPECTION, WAS REDEFINED. PARAGRAPH 4.4.3, GROUPD D INSPCTION, WAS REDEFINED. PARAGRAPH 4.5, SOURCE INSPECTION,WAS REDEFINED 4. PAGE 6, FIG 1, T039 CASE OUTLINE,ADD oja and ojc 5. PAGE 7, FIG 2, T03 CASE OUTLINE,ADD oja and ojc
C	144134 (02-12-98)	1. AMENDED PARAS. 4.1 AND 4.1.1. 2. ADD MKTG TO DISTRIBUTION.
D	163159 (11-18-99)	1. PAGE 3, ¶3.7 ADDED "AND AS" AND "HEREIN"; AND ¶3.9 ADDED "HEREIN". 2. PAGE 4, ¶s4.3 & 4.4.1 ADDED "HEREIN"; ¶s4.4.2.2 & 4.4.3.2 ADDED "PERTAINING TO" AND "IN". 3. PAGE 2, ¶s 3.2.1 & 3.2.2 HAD FIGURES 1 & 2 REMOVED.
E	501570 (05-30-02)	1. PAGE 2 ADDED FOR RECORD REVISIONS.PAGES 3 TO 14 HAD VARIOUS CHANGES - TOO MANY TO LIST.SEE PAGE 2 AND SHADED PARAS THROUGH OUT THE SPEC FOR CHANGES.
F 7/24/02	502503 JUL 2 4 2002	1. ADD THE CORRECT DATA SHEET WITH CORRECTED CONDITIONS.

REV. CHANGES DENOTED BY "REDLINED" AREAS.

DCBS: **CONTROLLED**: MPQA/ QA06
NON-CONTROLLED: SPEC REVIEW/ HI-REL/ PC / MIL MKT MGR

RH117

Positive Adjustable Regulator

DESCRIPTION

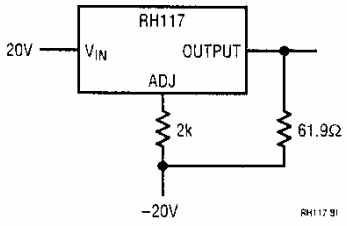
The RH117 is a 3-terminal positive adjustable regulator capable of supplying up to 0.5A (H package) or 1.5A (K package). The output is adjusted using two external resistors for a range of 1.2V to 37V. The devices have full current limit thermal overload safe area protection, all of which remain functional even if the adjustment terminal is disconnected.

The wafer lots are processed to LTC's in-house Class S flow to yield circuits usable in stringent military applications. In addition to 883 processing, the RH117 is subjected to 100% burn-in in thermal limit.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input-to-Output Voltage Differential 40V
Operating Junction
Temperature Range ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

BURN-IN CIRCUIT



PACKAGE/ORDER INFORMATION

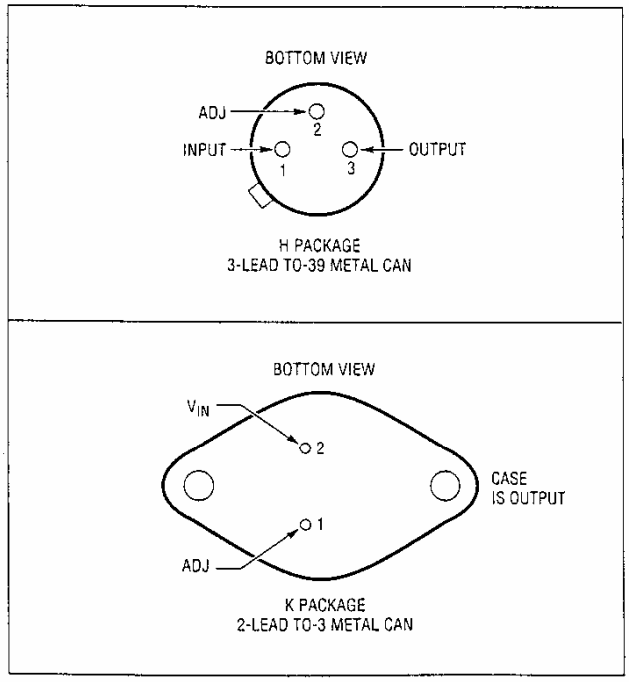


TABLE 1: ELECTRICAL CHARACTERISTICS (Preirradiation) (Note 1)

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_J = 25°C$ MIN	TYP	MAX	SUB-GROUP	$-55°C \le T_J \le 150°C$ MIN	TYP	MAX	SUB-GROUP	UNITS
V_{REF}	Reference Voltage	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $10mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$		1.20		1.30	1	1.20		1.30	2,3	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $I_{OUT} = 10mA$	2			0.02	1			0.05	2,3	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \le I_{OUT} \le I_{MAX}$, $V_{OUT} \le 5V$	2			15	1			50	2,3	mV
		$10mA \le I_{OUT} \le I_{MAX}$, $V_{OUT} \ge 5V$	2			0.3	1			1	2,3	%
	Thermal Regulation	20ms Pulse				0.07	1					%/W
	Ripple Rejection	$V_{OUT} = 10V$, f = 120Hz, $C_{ADJ} = 0$			65				65			dB
		$V_{OUT} = 10V$, f = 120Hz, $C_{ADJ} = 10\mu F$	3	66				66				dB
I_{ADJ}	Adjust Pin Current					100	1			100	2,3	µA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \le I_{OUT} \le I_{MAX}$				5	1			5	2,3	µA
		$2.5V \le (V_{IN} - V_{OUT}) \le 40V$, $I_{OUT} = 10mA$				5	1			5	2,3	µA
I_{MIN}	Minimum Load Current	$(V_{IN} - V_{OUT}) = 40V$				5	1			5	2,3	mA
	Current Limit	$(V_{IN} - V_{OUT}) \le 15V$ H Package		0.5			1	0.5			2,3	A
		K Package		1.5			1	1.5			2,3	A
		$(V_{IN} - V_{OUT}) = 40V$ H Package		0.15			1					A
		K Package		0.30			1					A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability	$-55°C \le T_J \le 150°C$							1			%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125°C$	3							1		%
e_n	RMS Output Noise	$10Hz \le f \le 10kHz$			0.001							%
θ_{JC}	Thermal Resistance (Junction to Case)	H Package	3			15						°C/W
		K Package	3			3						°C/W

TABLE 1A: ELECTRICAL CHARACTERISTICS (Postirradiation) (Note 4)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD(Si) MIN	MAX	20KRAD(Si) MIN	MAX	50KRAD(Si) MIN	MAX	100KRAD(Si) MIN	MAX	UNITS
V_{REF}	Reference Voltage	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $10mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$		1.20	1.30	1.20	1.30	1.20	1.30	1.20	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $I_{OUT} = 10mA$	2		0.02		0.02		0.02		0.03	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \le I_{OUT} \le I_{MAX}$, $V_{OUT} \le 5V$	2		36		42		48		60	mV
		$10mA \le I_{OUT} \le I_{MAX}$, $V_{OUT} \ge 5V$	2		0.72		0.84		0.96		1.20	%

TABLE 1A: ELECTRICAL CHARACTERISTICS (Postirradiation) (Note 5)

SYMBOL	PARAMETER	CONDITIONS		NOTES	10KRAD(Si) MIN	10KRAD(Si) MAX	20KRAD(Si) MIN	20KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	UNITS
I_{ADJ}	Adjust Pin Current					100		100		100		100	µA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \le I_{OUT} \le I_{MAX}$				5		5		5		5	µA
		$3V \le (V_{IN} - V_{OUT}) \le 40V$, $I_{OUT} = 10mA$				5		5		5		5	µA
I_{MIN}	Minimum Load Current	$(V_{IN} - V_{OUT}) = 40V$				5		5		5		5	mA
	Current Limit	$(V_{IN} - V_{OUT}) \le 15V$	H Package		0.5		0.5		0.5		0.5		A
			K Package		1.5		1.5		1.5		1.5		A
		$(V_{IN} - V_{OUT}) = 40V$	H Package		0.15		0.15		0.15		0.15		A
			K Package		0.30		0.30		0.30		0.30		A

Note 1: Unless otherwise specified, these specifications apply for $V_{IN} - V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the H package (TO-39) and $I_{OUT} = 0.5A$ for the K package (TO-3) package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and 20W for the TO-3. I_{MAX} is 0.5A for the TO-39 and 1.5A for the TO-3.

Note 2: Regulation is measured at a constant junction temperature using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 3: Guaranteed by design, characterization or correlation to other tested parameters.

Note 4: $T_J = 25°C$ unless otherwise noted.

TOTAL DOSE BIAS CIRCUIT

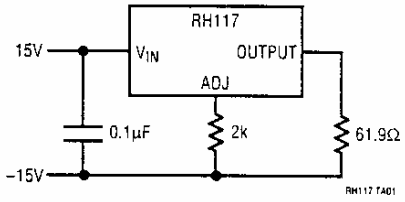


TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3
Group A Test Requirements (Method 5005)	1,2,3
Group C and D End Point Electrical Parameters (Method 5005)	1

* PDA Applies to subgroup 1. See PDA Test Notes.

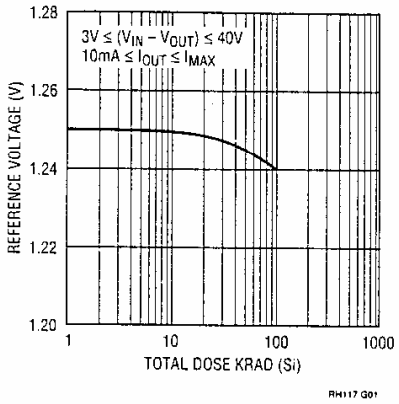
PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

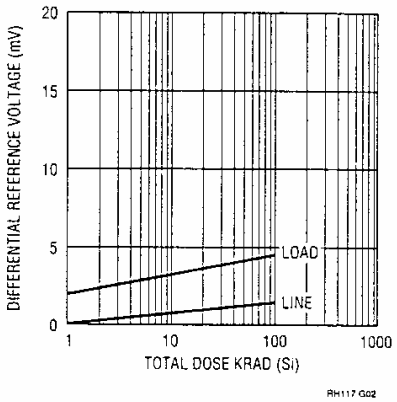
Linear Technology Corporation reserves the right to test to tighter limits than those given.

TYPICAL PERFORMANCE CHARACTERISTICS

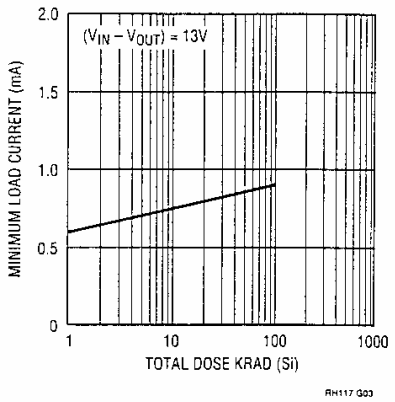
Reference Voltage



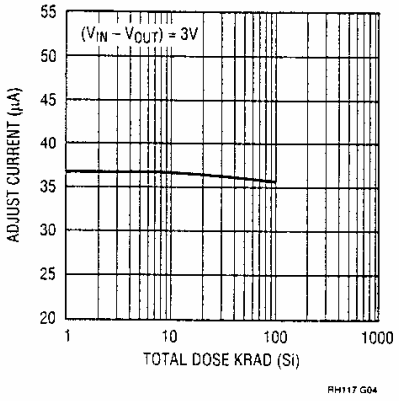
Regulation



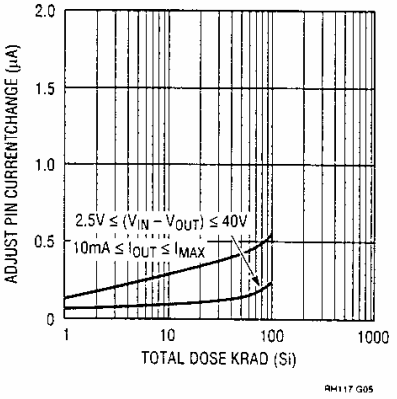
Minimum Load Current



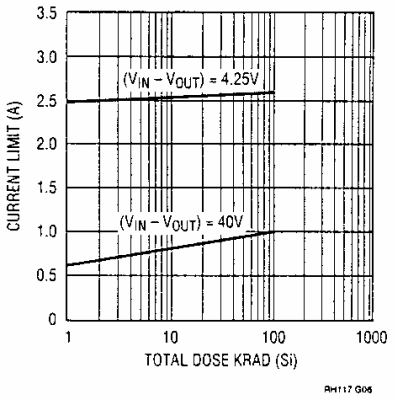
Adjust Pin Current



Adjust Pin Current Change



Current Limit



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