REVISION RECORD

| REV | DESCRIPTION | DATE |
|---|---|---|
| 0 | INITIAL RELEASE | 06/12/96 |
| A | • PAGE 2: ADDED PARAGRAPHS 3.2.1, 3.2.2, AND 3.2.3.<br>• PAGE 2: PARAGRAPH 3.3.b, ADDED "see paragraph 3.2".<br>• PAGE 3: ADDED PARAGRAPHS 3.8.1, 3.8.2, 3.8.3 TO EXPLAIN DEVICE OPTION BURN-IN. PARAGRAPH 3.10.1, ADDED FIG. 3 FOR WB PKG. PARAGRAPH 3.10.2, ADDED FIGURE 6 FOR WB PACKAGE.<br>• PAGE 4: PARAGRAPH 3.11.3, FIGURE 9 BECAME FIGURE 13. PARAGRAPH 3.12, WAFER LOT ACCEPTANCE EXPLANATION WAS REWRITTEN. PARAGRAPH 4.4.2, GROUP B INSPECTION, REDEFINED.<br>• PAGE 5: PARAGRAPH 4.4.3, GROUP D INSPECTION, REDEFINED. PARAGRAPH 4.5.1, SOURCE INSPECTION, REDEFINED.<br>• PAGES 6, 7, 8, FIGS. 1, 2, 3: ADDED θja AND θjc TO CASE OUTLINE.<br>• PAGE 9, ADDED FIGURE 6 FOR WB PACKAGE.<br>• PAGE 10, FIG 5 BECAME FIG. 7. PAGE 11, FIG. 6 BECAME FIG. 8. PAGE 12, FIG. 7 BECAME FIG. 9. PAGE 13, FIG. 8 BECAME FIG. 10. PAGE 14, ADDED FIG. 11. PAGE 15, ADDED FIG. 12. PAGE 17, MOVED NOTES TO PAGE 18. | 12/12/97 |
| B | PAGE 5, AMENDED PARAGRAPHS 4.1 AND 4.1.1 TAKING EXCEPTION TO ANALYSIS OF CATASTROPHIC FAILURES.<br>ADDED A SECOND PAGE FOR REVISION RECORD. UPDATED ENTIRE SPEC TO NEXT REVISION DUE TO THE ADDITIONAL PAGE. | 04/20/98 |
| C | PAGE 7, CHANGED TO5 CASE OUTLINE θja FROM 180°C/W TO 150°C/W, θjc REMAINED THE SAME.<br>PAGE 8, CHANGED CERDIP CASE OUTLINE θja FROM 100°C/W TO 110°C/W, θjc CHANGED FROM 25°C/W TO 30°C/W.<br>CHANGED PACKAGE "WB" (BOTTOM BRAZED FLATPACK) TO "W" (GLASS SEAL FLATPACK) ON PAGES 3, 4, 9, 10, 15, AND 16. | 07/19/99 |
| D | • PAGE 3, PARAGRAPHS 3.2.1, 3.2.2, 3.2.3 HAD FIGURES 1, 2, AND 3 REMOVED.<br>• PAGE 4, PARAGRAPH 3.7 CHANGED VERBIAGE FROM "SPECIFIED IN TABLE III" TO "AND AS SPECIFIED IN TABLE III HEREIN", LINE 2. PARAGRAPH 3.9, ADDED "HEREIN" AFTER "TABLE II" LINE 2.<br>CONTINUED ON NEXT PAGE….. | 12/29/99 |

**REVISION RECORD AND DESCRIPTION CONTINUED ON NEXT PAGE.**

**CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART**

| REVISION | PAGE NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INDEX | REVISION | **K** | **K** | **K** | **K** | **K** | **K** | **K** | **K** | **K** | **K** | **K** | **K** | **K** | **K** | **K** | **K** | **K** |
| REVISION | PAGE NO. | 18 | 19 | 20 | | | | | | | | | | | | | | |
| INDEX | REVISION | **K** | **K** | **K** | | | | | | | | | | | | | | |

| | | | | |
|---|---|---|---|---|
| | | | | **LINEAR TECHNOLOGY CORPORATION MILPITAS, CALIFORNIA** |
| | ORIG | | | |
| | DSGN | | | TITLE: |
| | ENGR | | | **MICROCIRCUIT, LINEAR, RH07, OPERATIONAL AMPLIFIER** |
| | MFG | | | |
| | CM | | | |
| | QA | | | SIZE: |
| | PROG | | | |
| APPLICATION | FUNCT | SIGNOFFS | DATE | CONTRACT: |

| SIZE | CAGE CODE | DRAWING NUMBER | REV |
|---|---|---|---|
| | **64155** | **05-08-5010** | **K** |

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| REVISION RECORD | | |
|---|---|---|
| REV | DESCRIPTION | DATE |
| D | • PAGE 5, PARAGRAPH 4.3, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.1, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.2.2 CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IIA OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IIA OF MIL-STD-883".<br>• PAGE 6: PARAGRAPH 4.4.3.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IV OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IV OF MIL-STD-883". | 12/29/99 |
| E | • PAGE 3:<br>PARAGRAPH 3.2.1 ADDED "OPTION 1", PARAGRAPH 3.2.2, ADDED "OPTION 2", PARAGRAPH 3.2.3, ADDED "OPTION 3".<br><br>• PAGE 4:<br>PARAGRAPH 3.6, TABLE IA CHANGED TO TABLE II.<br>PARAGRAPH 3.7, TABLE III CHANGED TO TABLE IV.<br>PARAGRAPH 3.9, TABLE II CHANGED TO TABLE III.<br>PARAGRAPH 3.10.3, ADDED "DEVICE OPTIONS 1, 2, AND 3" TO LINE 1.<br>PARAGRAPH 3.11.1 WAS CHANGED FROM "…dosage rate of approximately 20 Rads per second" TO "…dosage rate of less than or equal to 10 Rads per second".<br><br>• PAGE 5:<br>PARAGRAPHS 4.1 THROUGH 4.4.2.1 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING.<br><br>• PAGE 6:<br>PARAGRAPH 4.4.3 CHANGE WAS DONE TO CLARIFY GROUP SAMPLING.<br>PARAGRAPHS 4.6.2 THROUGH 4.6.4 WERE RE-WRITTEN. THESE DATA PROVIDED, AND DATA AVAILABLE.<br>PARAGRAPH 4.6.10 NOTE, ADDED FURTHER EXPLANATION OF MINIMUM DELIVERED DATA.<br><br>• PAGES 7 THROUGH 17, ALL FIGURE TITLES CHANGED TO HAVE DEVICE OPTIONS AND PACKAGE TYPES AT TOP OF PAGE, AND HAVE ALL FIGURES AT BOTTOM OF PAGE.<br><br>• PAGE 10, MOVED FIGURES TO BETTER FIT ON THE PAGE.<br><br>• PAGE 11, STATIC BURN-IN CIRCUIT CHANGED FROM 04-06-0202 TO 04-06- 0001, PER ENGINEERING REQUEST.<br><br>• PAGE 18, TABLE I NOTE CHANGED FROM "Note E" to "NOTE 5".<br><br>• PAGE 19, TABLE II NOTE CHANGED FROM "Note F" TO "NOTE 6". | 09/20/02 |
| F | • CHANGED PACKAGE OUTLINE DRAWING FOR THE "W" FLATPAK, 10 LEAD, GLASS SEAL , DETAIL A, NOTCH MOVED TO THE INSIDE LEAD LOCATION. | 05/19/03 |
| G | • PAGE 4, CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC. | 03/16/05 |
| H | • PAGE 5, CHANGED IN BOTH PARAGRAPHS 4.2, 4.3 IN CONJUNCTION TO 3.3 CHANGED TO 3.4 AND PARAGRAPH 4.3 CHANGED 3.1.1 TO 3.1 AND 3.2.1 TO 3.1.1<br>• PAGE 4, PARAGRAPH 3.10.3 ADDED OPTION 3 ALLOY 42 FOR FLATPACK. | 10/11/07 |
| J | • PAGE 4, PARAGRAPH 3.11.1 CHANGED VERBIAGE. PARAGRAPH 3.10.3 CHANGED OPTION 2 TO ALLOY 42 PACKAGE REQUIREMENT. | 04/29/08 |
| **K** | • **PAGE 5, PARAGRAPH 4.4.2 CHANGED VERBIAGE**<br>• **PAGE 9, FIGURE 3 NOTE 2 ADDED TO LEAD THICKNESS.** | **05/27/08** |

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

| | |
|---|---|
| MIL-PRF-38535 | Integrated Circuits (Microcircuits) Manufacturing, General Specification for |
| MIL-STD-883 | Test Method and Procedures for Microcircuits |
| MIL-STD-1835 | Microcircuits Case Outlines |

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH07 Operational Amplifier, processed to space level manufacturing flow.

3.2 Part Number:

3.2.1 Option 1 – RH07H (TO5 Metal Can, 8 Leads)

3.2.2 Option 2 – RH07J8 (Ceramic Dip, 8 Leads)

3.2.3 Option 3 – RH07W (Glass Sealed Flatpack, 10 Leads)

3.3 Part Marking Includes:

a. LTC Logo

b. LTC Part Number (See Paragraph 3.2)

c. Date Code

d. Serial Number

e. ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings:

| | |
|---|---|
| Supply Voltage | ±22V |
| Differential Input Voltage | ±30V |
| Input Voltage | ±22V |
| Output Short Circuit Duration **1/** | Indefinite |
| Operating Temperature Range | -55°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (Soldering, 10 sec) | +300°C |

**1/ Parameter is guaranteed by design, characterization, or correlation to other tested parameters.**

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 1.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and Table II.

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in Table IV herein.

3.8 Burn-In Requirement:

3.8.1 Option 1 (TO5): Static Burn-In, Figure 7; Dynamic Burn-In, Figure 8

3.8.2 Option 2 (Ceramic Dip): Static Burn-In, Figure 9; Dynamic Burn-In, Figure 10

3.8.3 Option 3 (Glass Sealed Flatpack) : Static Burn-In, Figure 11; Dynamic Burn-In, Figure 12

3.9 Delta Limit Requirement: Delta limit parameters are specified in Table III herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1, Figure 2, and Figure 3.

3.10.2 Terminal Connections: The terminal connections shall be as specified in Figure 4, Figure 5, and Figure 6.

3.10.3 Lead Material and Finish: The lead material and finish for Device Options 1, shall be Kovar and Options 2, 3 are Alloy 42. The lead finishes shell be hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

3.11 Radiation Hardness Assurance (RHA):

3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.11.3 Total dose bias circuit is specified in Figure 13.

3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.

3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1, and 3.4 of the test method. Electrical testing shall be as specified in **Table IV** herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in **Table IV** herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroups 1-4 plus 6 are performed on every assembly lot, and Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1

| | |
|---|---|
| Group B, Subgroup **2c** = 10% | Group B, Subgroup **5** = *5% (*per wafer or inspection lot whichever is the larger quantity) |
| Group B, Subgroup **3** = 10% | |
| Group B, Subgroup **4** = 5% | Group B, Subgroup **6** = 15% |

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Source Inspection:

4.5.1 The manufacturer will coordinate Source Inspection at wafer lot acceptance and pre-seal internal visual.

4.5.2 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance and final data review.

4.6 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.6.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.6.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.6.3 Burn-In Variables Data and Deltas (if applicable)

4.6.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.6.5 Generic Group D data (4.4.3 herein)

4.6.6 SEM photographs (3.13 herein)

4.6.7 Wafer Lot Acceptance Report (3.13 herein)

4.6.8 X-Ray Negatives and Radiographic Report

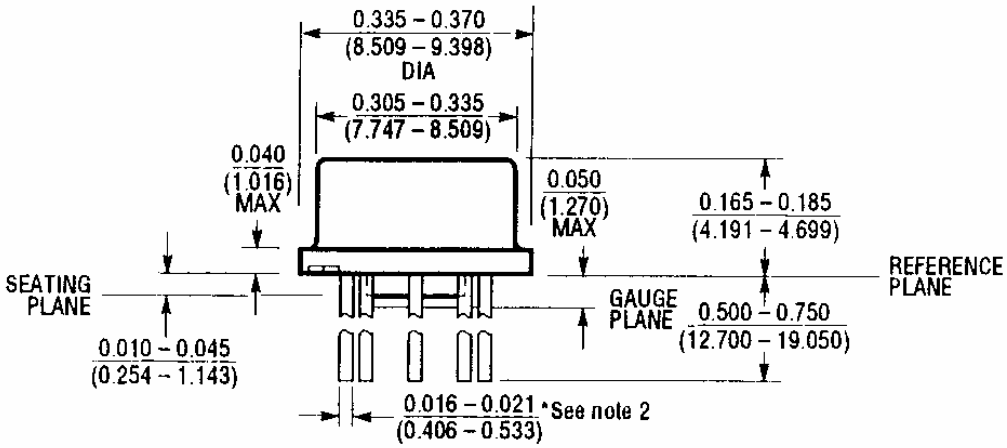
4.6.9 A copy of outside test laboratory radiation report if ordered

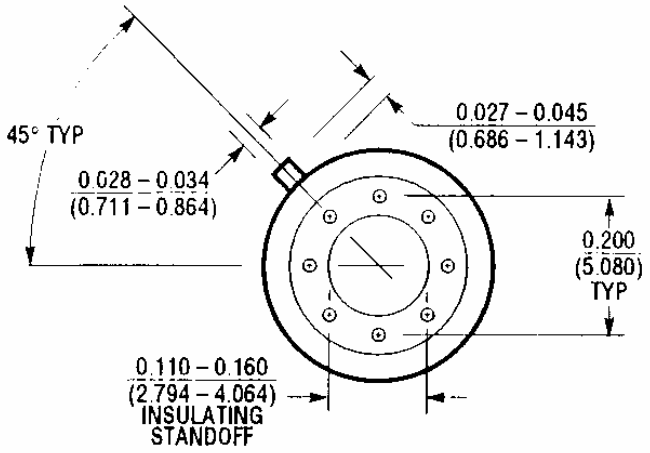
4.6.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 4.6.1 and 4.6.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as "No Charge Data".

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

**DEVICE OPTION # 1**
**(H) TO5 / 8 LEADS CASE OUTLINE**



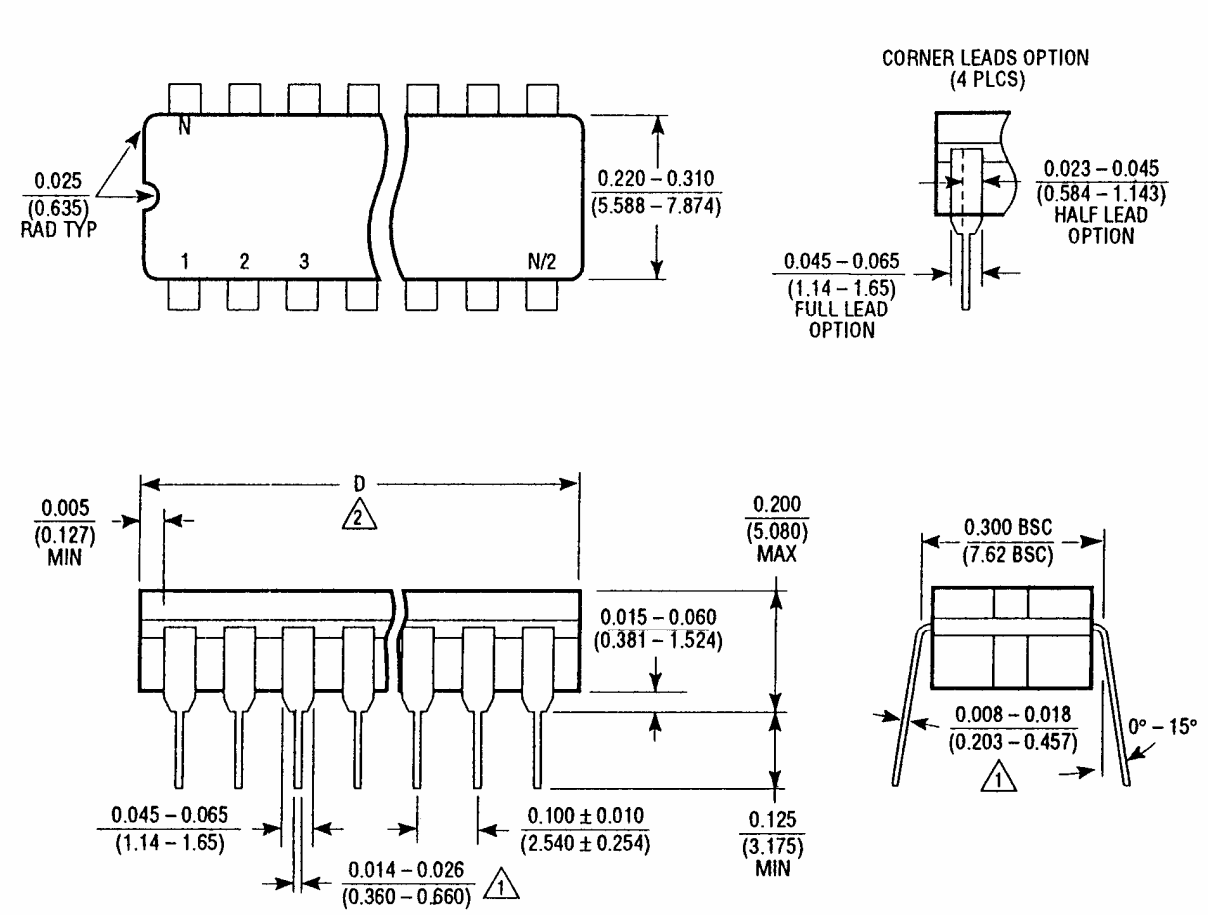




NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.
2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 – 0.024 (0.406 – 0.610)

θja = +150°C/W
θjc = +40°C/W

**FIGURE 1**

**DEVICE OPTION # 2**
**(J8) CERAMIC DIP / 8 LEADS CASE OUTLINE**

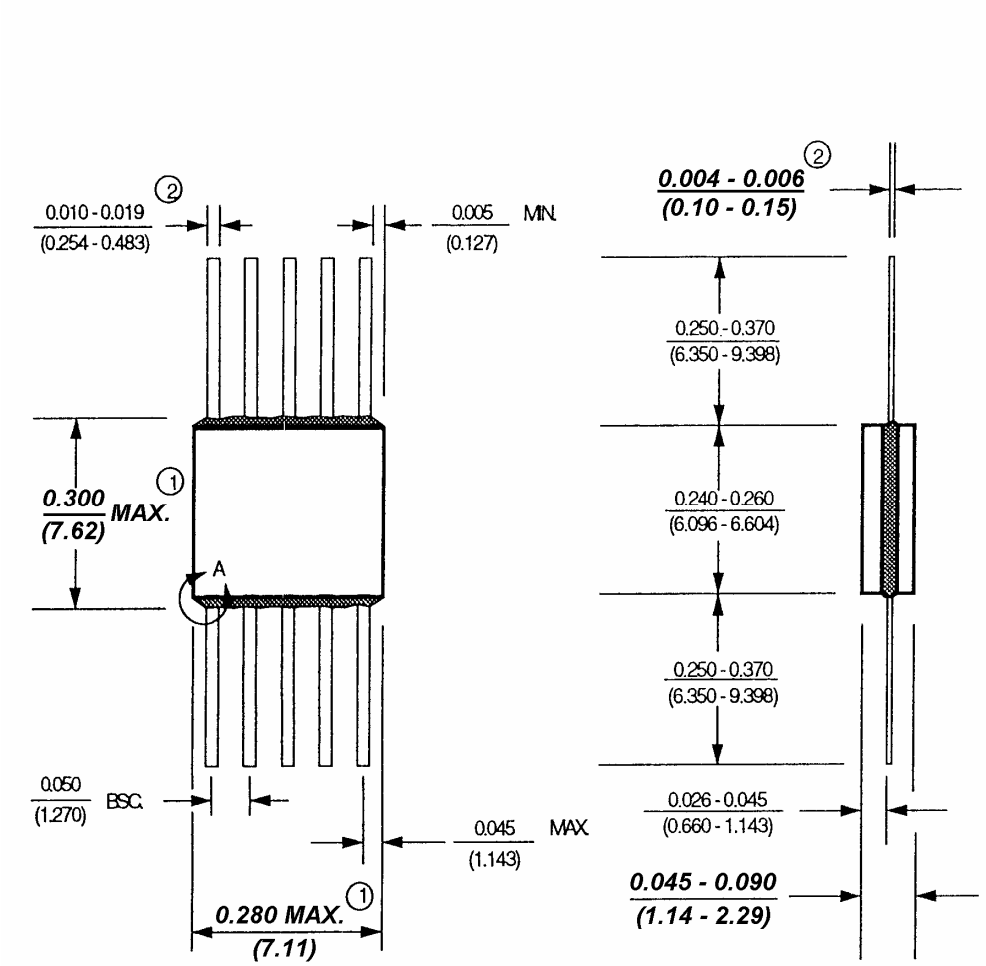



NOTE: 1. LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.
2. 8 LEAD D MAX = .405 (10.287)

θja = +110°C/W
θjc = +30°C/W

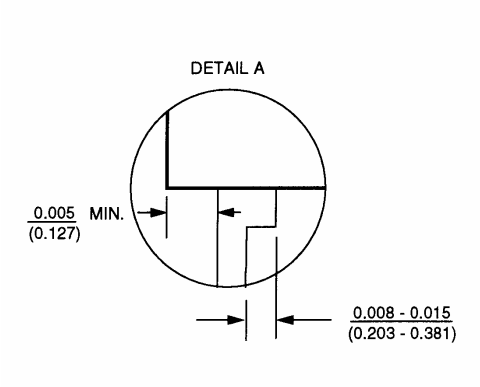
**FIGURE 2**

**DEVICE OPTION # 3**
**(W10) GLASS SEALED FLATPACK / 10LEADS CASE OUTLINE**




NOTE: 1. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVER RUN.

NOTE: 2. INCREASE DIMENSION BY 0.003 INCH WHEN LEAD FINISH IS APPLIED (SOLDER DIPPED).




$\theta ja$ = +170°C/W
$\theta jc$ = +40°C/W

**Figure 3**

## TERMINAL CONNECTIONS

### DEVICE OPTION #1, TO5 8 LEAD METAL CAN

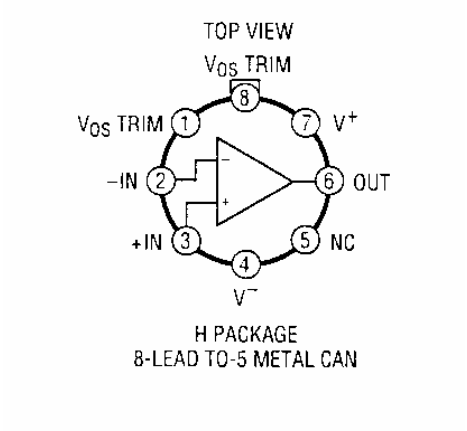



**FIGURE 4**

### DEVICE OPTION #2, 8 LEAD CERAMIC DIP

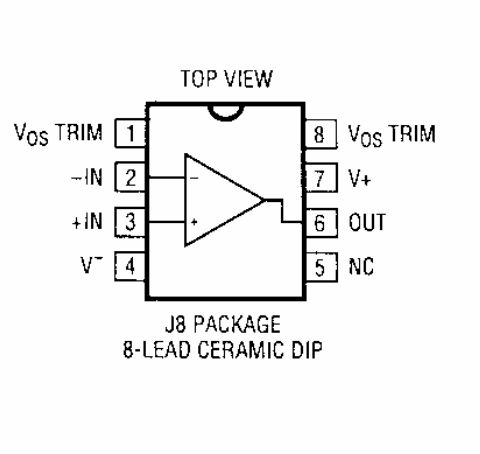



**FIGURE 5**

### DEVICE OPTION #3, GLASS SEALED 10 LEAD FLATPACK

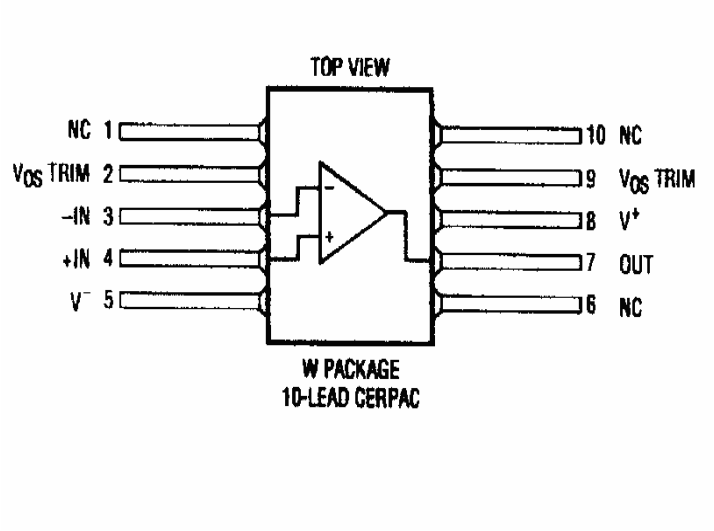
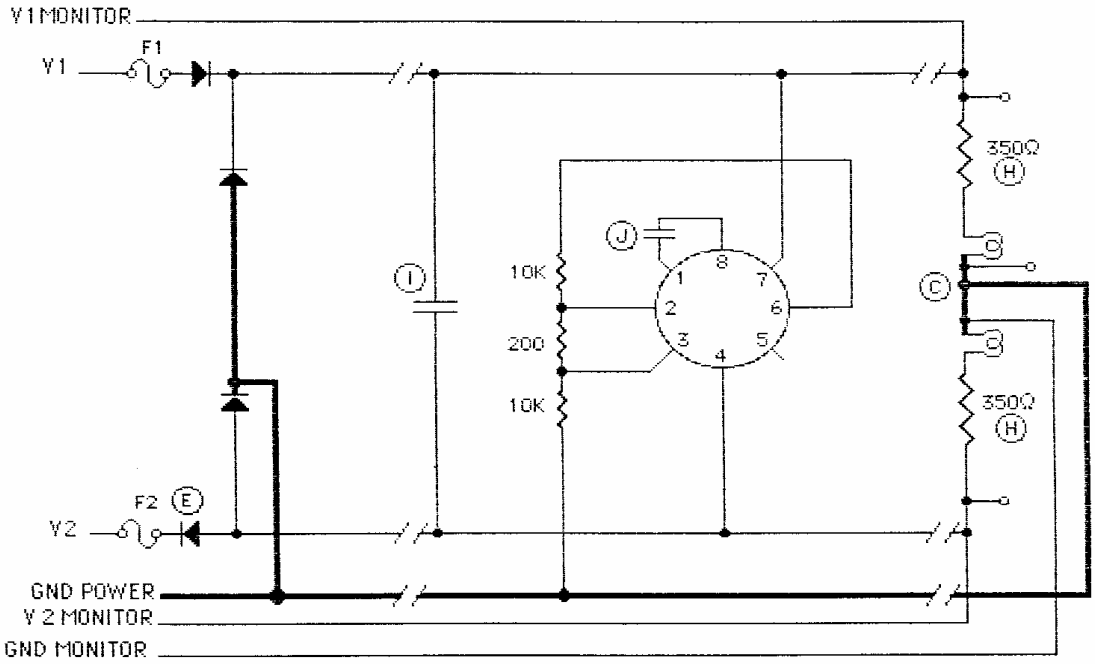


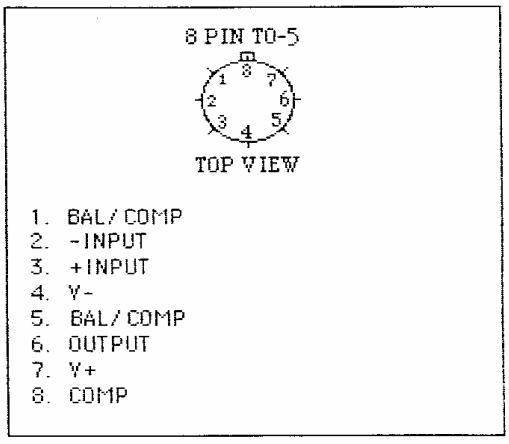

**FIGURE 6**

## STATIC BURN-IN CIRCUIT
## OPTION 1, TO5 METAL CAN / 8 LEADS




NOTES:

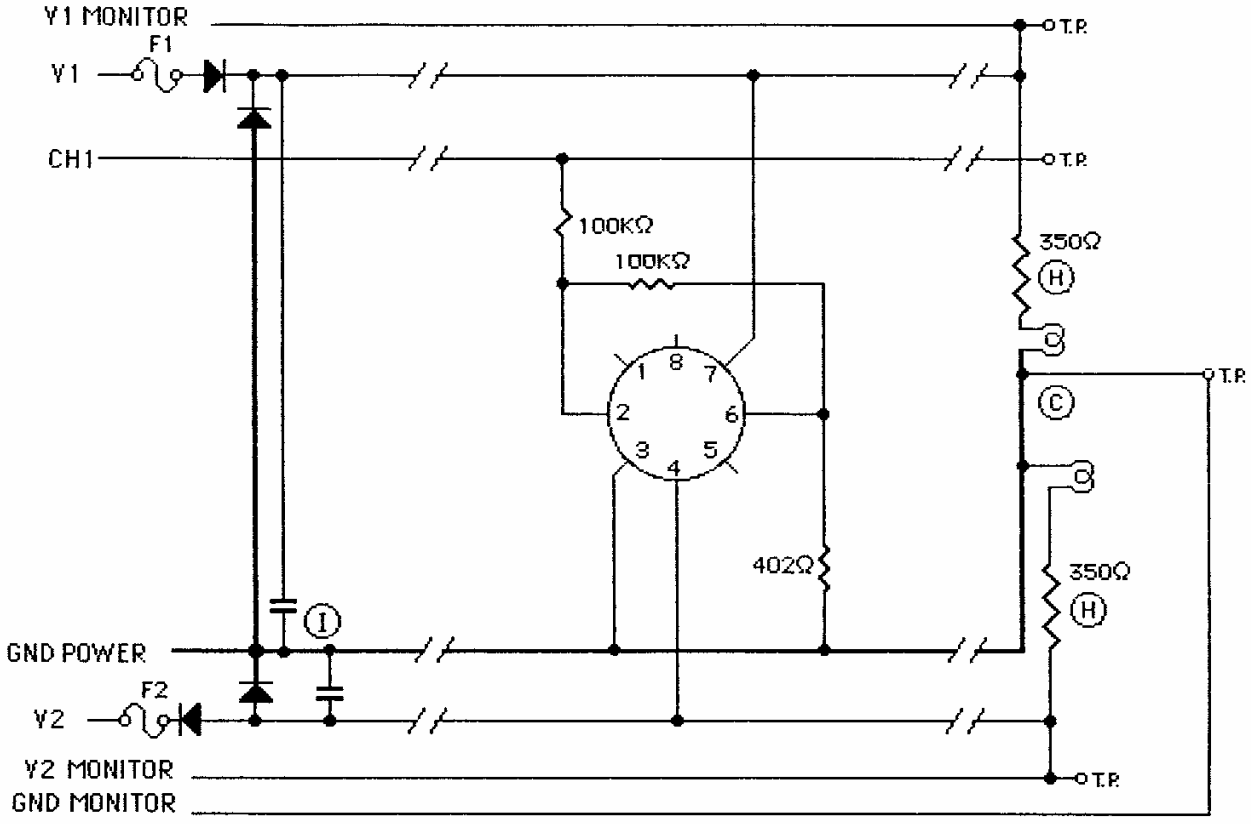
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj maximum = Varies with device being burned in.
3. Ta = 150 °C.
4. Burn-in voltages; V1 = +20V to +22V
   V2 = -20V to -22V

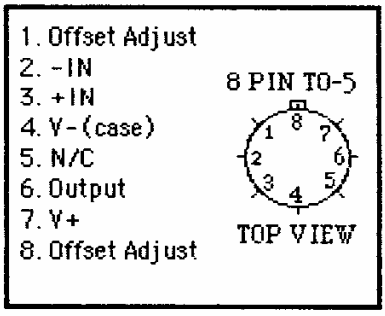



PACKAGE AND PINOUT

**FIGURE 7**

**DYNAMIC BURN-IN CIRCUIT**
**OPTION 1, TO5 METAL CAN / 8 LEADS**

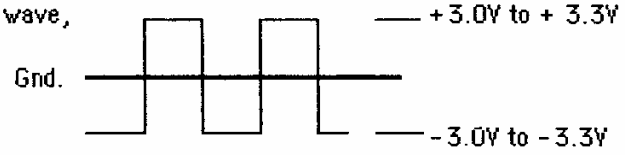



PACKAGE

NOTES:

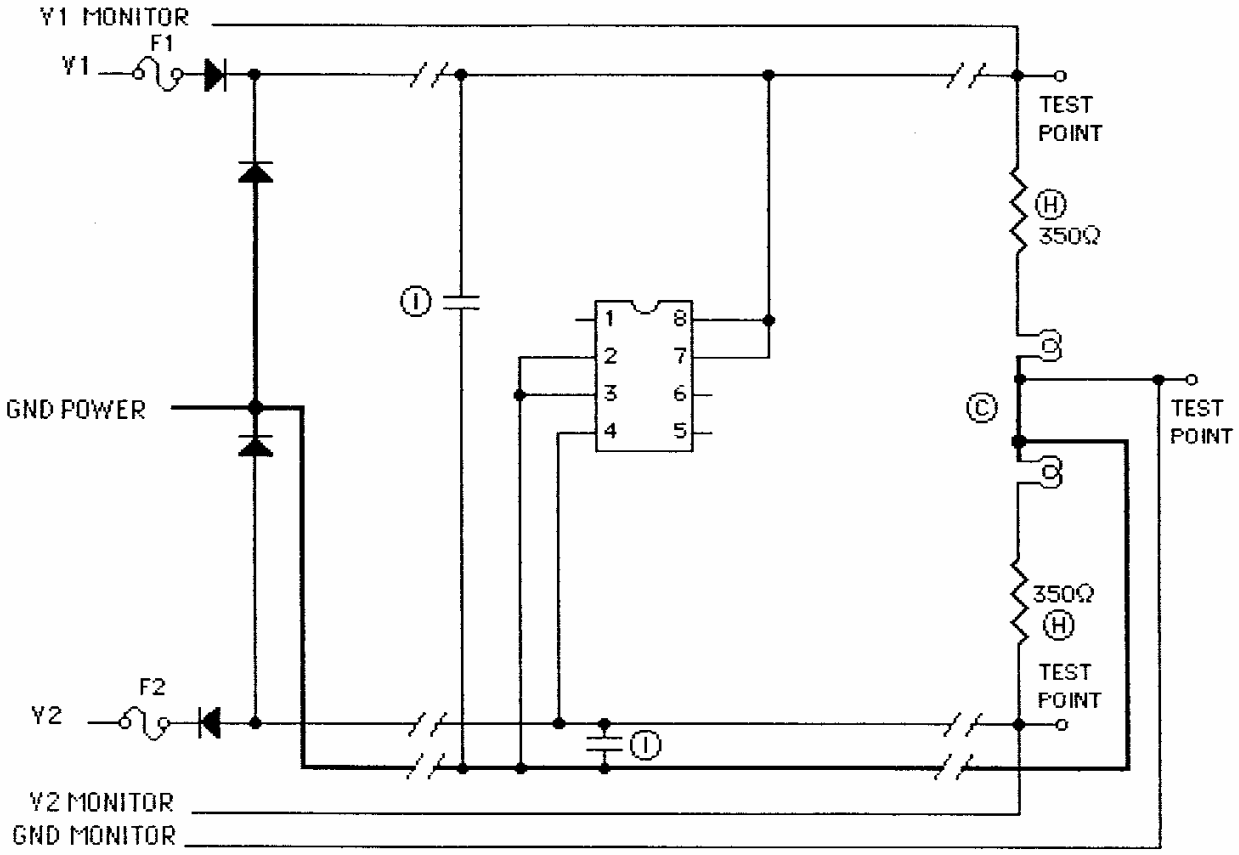
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj max = 163° C
3. Ta = 125° C
4. Burn-in Voltages: V1 = + 20V to + 22V
   V2 = - 20V to - 22V
5. CH. 1 = Square wave,




Frequency, 4.5hz(222ms) to 5.5hz(182ms)

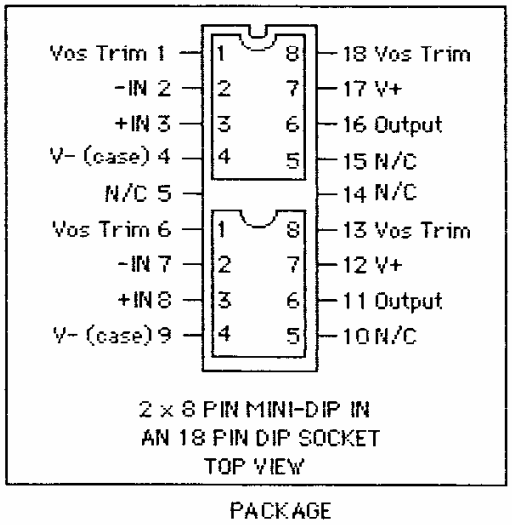
**FIGURE 8**

**STATIC BURN-IN CIRCUIT**
**OPTION #2, CERDIP / 8 LEADS**




NOTES:

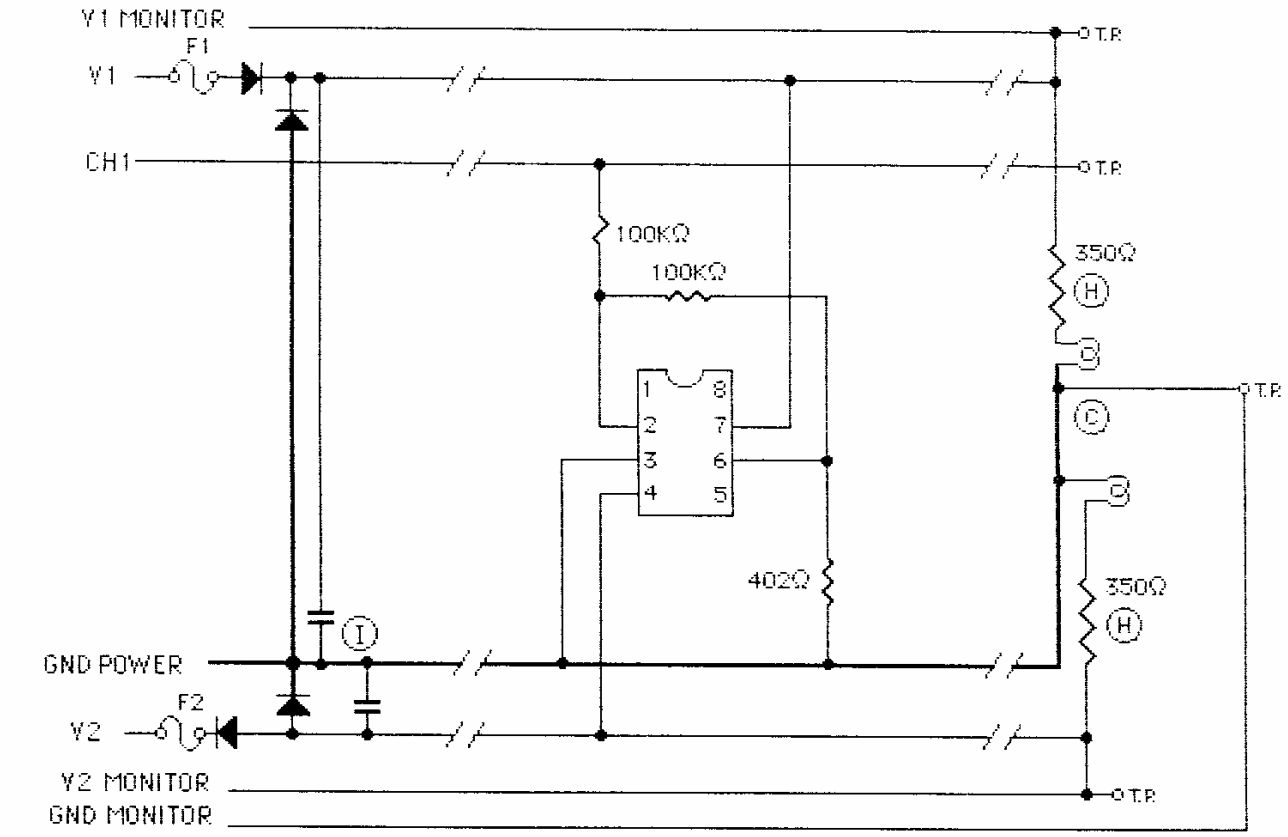
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Ta = 150° C
3. Tj = 175° C max
4. Burn-in voltages: V1 = +20V to + 22V
   V2 = - 20V to - 22V




PACKAGE

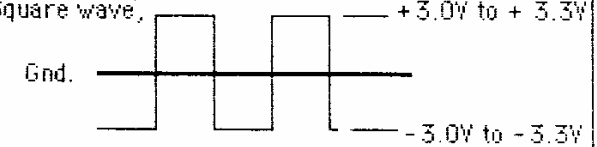
**FIGURE 9**

**DYNAMIC BURN-IN CIRCUIT**
**OPTION 2, CERDIP / 8 LEADS**

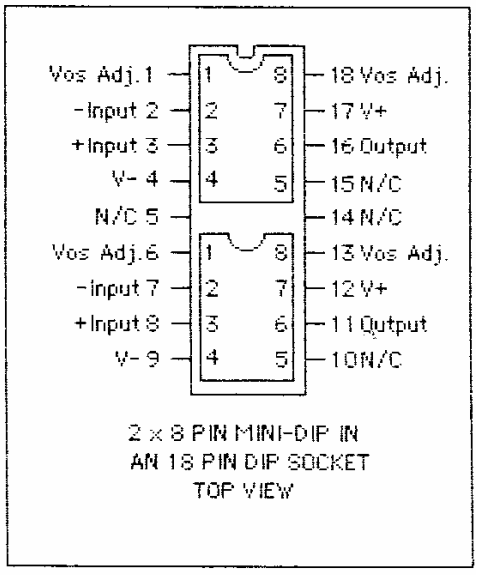



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj max = 168° C
3. Ta = 125° C
4. Burn-in Voltages: V1 = + 20V to + 22V
   V2 = - 20V to - 22V
5. CH. 1 = Square wave,



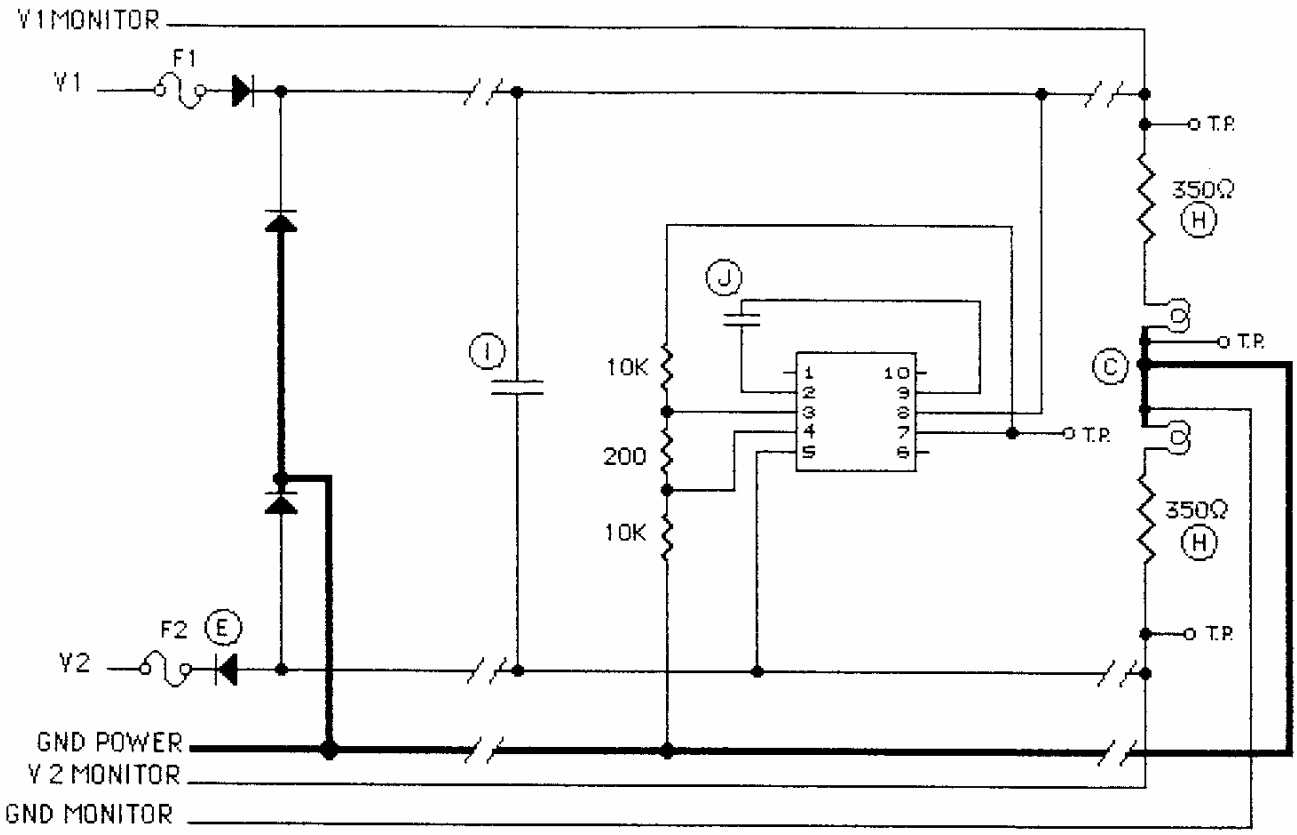

Frequency, 4.5hz(222ms) to 5.5hz(182ms)




PACKAGE

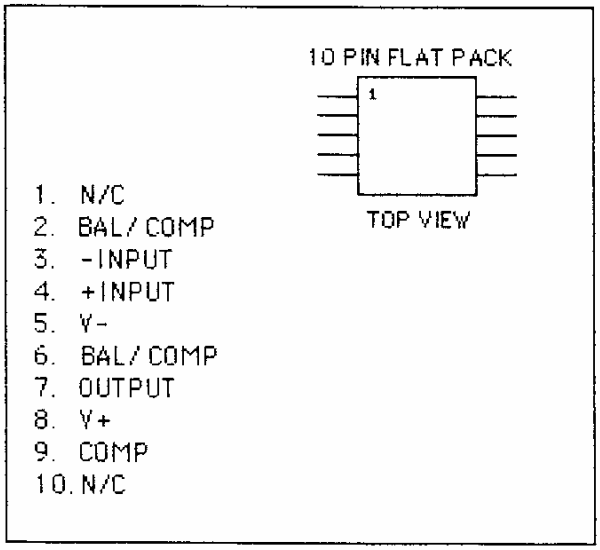
**FIGURE 10**

**STATIC BURN-IN CIRCUIT**
**OPTION 3, GLASS SEALED FLATPACK / 10 LEAD**




NOTES:

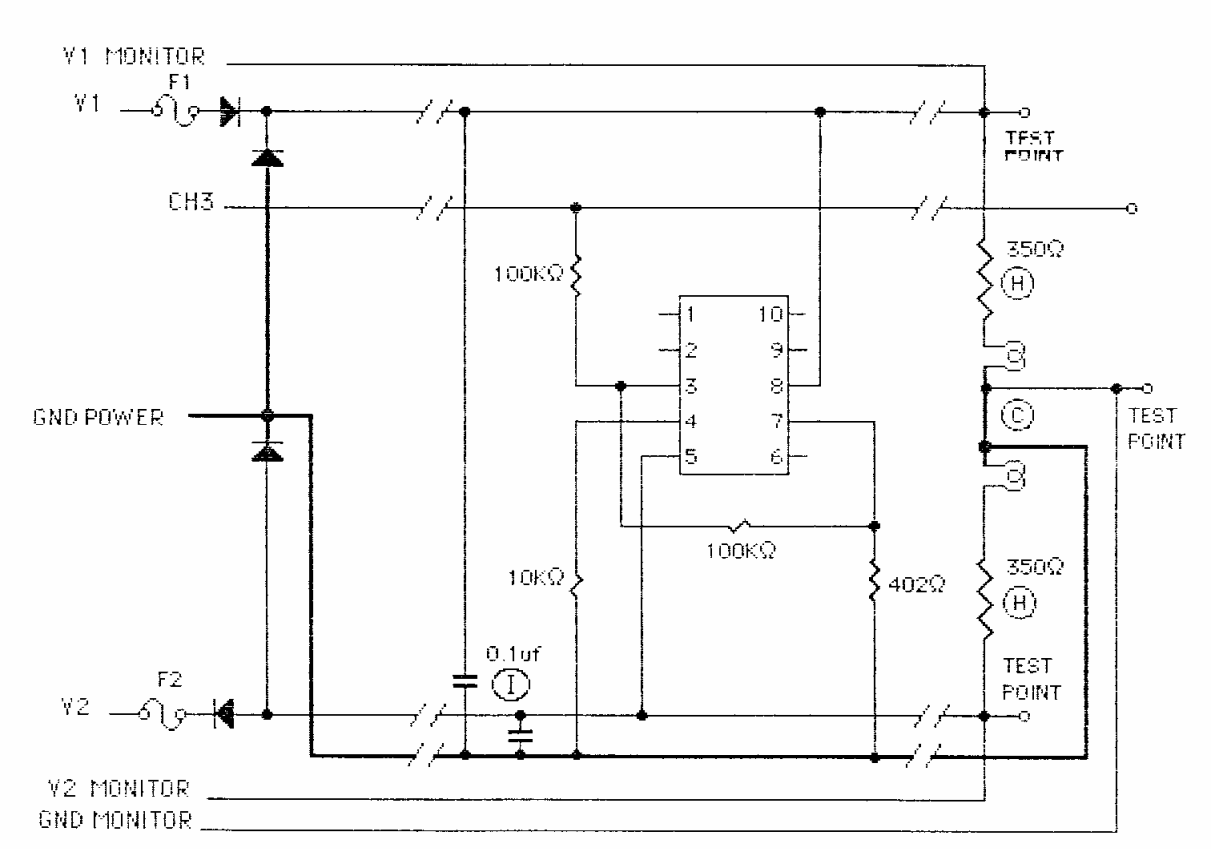
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj maximum = Varies with device being burned in.
3. Ta = 150 °C.
4. Burn-in voltages; V1 = +20V to +22V
   V2 = -20V to -22V



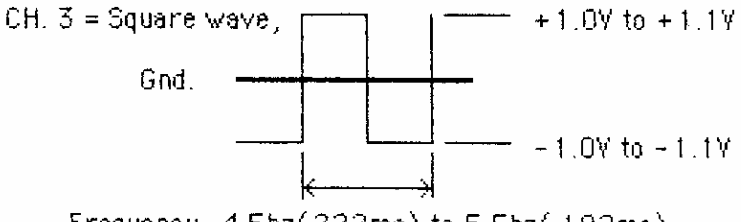

PACKAGE AND PINOUT

**FIGURE 11**

**DYNAMIC BURN-IN CIRCUIT**
**OPTION 3, GLASS SEALED FLATPACK / 10 LEAD**

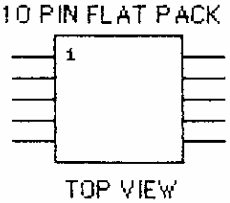



NOTES:
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = +166 ° C maximum.
3. Ta = +125 ° C .
4. Burn-in Voltages: V1 = +20V to +22V
   V2 = -20V to -22V




Frequency, 4.5hz(222ms) to 5.5hz( 182ms)

1. N/C
2. Vos TRIM
3. - INPUT
4. + INPUT
5. V-
6. N/C
7. OUTPUT
8. V+
9. Vos TRIM
10. N/C




PACKAGE

**FIGURE 12**

**TOTAL DOSE BIAS CIRCUIT**

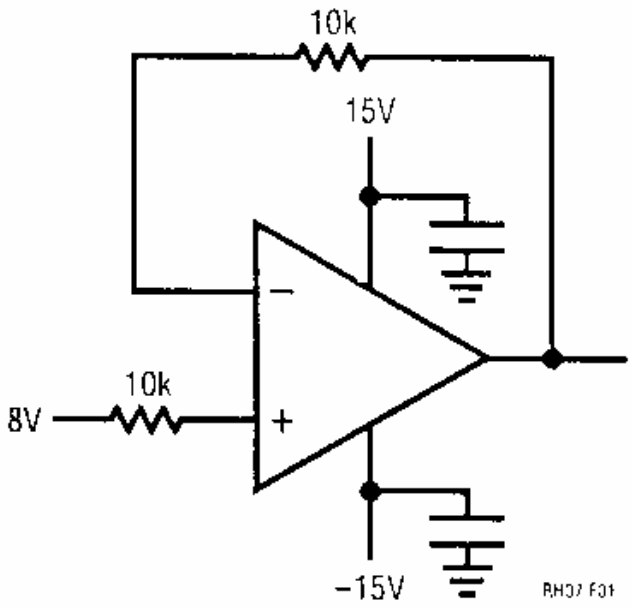



**FIGURE 13**

## TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION) NOTE 5

| SYMBOL | PARAMETER | CONDITIONS | NOTES | $T_A = 25°C$ MIN | TYP | MAX | SUB-GROUP | $-55°C \le T_A \le 125°C$ MIN | TYP | MAX | SUB-GROUP | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | 1 | | | 75 | 4 | | | 200 | 2,3 | µV |
| $\frac{\Delta V_{OS}}{\Delta Temp}$ | Avg Input Offset Voltage Drift: | | | | | | | | | | | |
| | Without External Trim | | 3 | | | | | | | 1.3 | | µV/°C |
| | With External Trim | Null Pot = 20kΩ | 3 | | | | | | | 1.3 | | µV/°C |
| $\frac{\Delta V_{OS}}{\Delta Time}$ | Long-Term Input Offset Voltage Stability | | 2,3 | | | 1 | | | | | | µV/Mo |
| $I_{OS}$ | Input Offset Current | | | | | 2.8 | 1 | | | 5.6 | 2,3 | nA |
| $\frac{\Delta I_{OS}}{\Delta Temp}$ | Avg Input Bias Current Drift | | 3 | | | | | | | 50 | | pA/°C |
| $I_B$ | Input Bias Current | | | | | ±3 | 1 | | | ±6 | 2,3 | nA |
| $\frac{\Delta I_B}{\Delta Temp}$ | Avg Input Bias Current Drift | | 3 | | | | | | | 50 | | pA/°C |
| $e_n$ | Input Noise Voltage | 0.1Hz to 10Hz | 3 | | | 0.6 | | | | | | $\mu V_{P-P}$ |
| | Input Noise Voltage Density | $f_O$ = 10Hz | 4 | | | 18 | | | | | | nV/√Hz |
| | | $f_O$ = 100Hz | 3 | | | 13 | | | | | | nV/√Hz |
| | | $f_O$ = 1000Hz | 3 | | | 11 | | | | | | nV/√Hz |
| $i_n$ | Input Noise Current | 0.1Hz to 10Hz | 3 | | | 30 | | | | | | $pA_{P-P}$ |
| | Input Noise Current Density | $f_O$ = 10Hz | 3 | | | 0.80 | | | | | | pA/√Hz |
| | | $f_O$ = 100Hz | 3 | | | 0.23 | | | | | | pA/√Hz |
| | | $f_O$ = 1000Hz | 3 | | | 0.17 | | | | | | pA/√Hz |
| $R_{IN}$ | Input Resistance: | | | | | | | | | | | |
| | Differential Mode | | 3 | 20 | | | | | | | | MΩ |
| | Common Mode | | | | 200 | | | | | | | GΩ |
| | Input Voltage Range | | 3 | ±13.5 | | | | ±13.5 | | | | V |
| CMRR | Common-Mode Rejection Ratio | $V_{CM}$ = ±13V | | 110 | | | 1 | 106 | | | 2,3 | dB |
| PSRR | Power Supply Rejection Ratio | $V_S$ = ±3V to ±18V | | 100 | | | 1 | 94 | | | 2,3 | dB |
| $A_{VOL}$ | Large-Signal Voltage Gain | $R_L \ge 2k$, $V_O$ = ±10V | | 200 | | | 4 | 150 | | | 5,6 | V/mV |
| | | $R_L \ge 500Ω$, $V_O$ = ±0.5V | 3 | 150 | | | | | | | | V/mV |
| | | $V_S$ = ±3V | | | | | | | | | | |
| $V_{OUT}$ | Maximum Output Voltage Swing | $R_L \ge 10k$ | | | | ±12.5 | 4 | | | | | |
| | | $R_L \ge 2k$ | | | | ±12.0 | 4 | | | ±12.0 | 5,6 | |
| | | $R_L \ge 1k$ | | | | ±10.5 | 4 | | | | | |
| SR | Slew Rate | $R_L \ge 2k$ | 3 | 0.1 | | | | | | | | V/µs |
| GBW | Closed-Loop Bandwidth | $A_{VCL}$ = 1 | 3 | 0.4 | | | | | | | | MHz |
| $P_D$ | Power Dissipation | $V_S$ = ±15V | | | | 120 | 1 | | | | | mW |
| | | $V_S$ = ±3V | | | | 6 | 1 | | | | | mW |

## TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION) NOTE 6

| SYMBOL | PARAMETER | CONDITIONS | NOTES | 10KRAD(Si) MIN | 10KRAD(Si) MAX | 20KRAD(Si) MIN | 20KRAD(Si) MAX | 50KRAD(Si) MIN | 50KRAD(Si) MAX | 100KRAD(Si) MIN | 100KRAD(Si) MAX | 200KRAD(Si) MIN | 200KRAD(Si) MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | 1 | | 90 | | 150 | | 200 | | 250 | | 300 | µV |
| $I_{OS}$ | Input Offset Current | | | | 2.8 | | 4 | | 8 | | 12 | | 20 | nA |
| $I_B$ | Input Bias Current | | | | ±3 | | ±10 | | ±25 | | ±50 | | ±100 | nA |
| | Input Voltage Range | | 3 | ±13.5 | | ±13.5 | | ±13.5 | | ±13.5 | | ±13.5 | | V |
| CMRR | Common-Mode Rejection Ratio | $V_{CM}$ = ±13V | | 110 | | 110 | | 105 | | 100 | | 95 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_S$ = ±3V to ±18V | | 100 | | 100 | | 100 | | 95 | | 90 | | dB |
| $A_{VOL}$ | Large-Signal Voltage Gain | $R_L \geq 2k$, $V_O$ = ±10V | | 200 | | 200 | | 180 | | 150 | | 120 | | V/mV |
| $V_{OUT}$ | Maximum Output Voltage Swing | $R_L \geq 10k$ | | ±12.5 | | ±12.5 | | ±12.5 | | ±12.5 | | ±12.5 | | V |
| SR | Slew Rate | $R_L \geq 2k$ | | 0.1 | | 0.1 | | 0.1 | | 0.075 | | 0.05 | | V/µs |
| $P_D$ | Power Dissipation | | | 120 | | 120 | | 120 | | 120 | | 120 | | mW |

**Note 1:** Offset voltage is measured with high speed test equipment approximately 0.5 seconds after power is applied.

**Note 2:** Long-term input offset voltage stability refers to the averaged trend line of $V_{OS}$ vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in $V_{OS}$ during the first 30 days are typically 2.5µV.

**Note 3:** Parameter is guaranteed by design, characterization, or correlation to other tested parameters.

**Note 4:** 10Hz noise voltage density is sample tested on every lot to an LTPD of 15. Devices 100% tested at 10Hz are available on request.

**Note 5:** $V_S$ = ±15V, $V_{CM}$ = 0V, unless otherwise noted.

**Note 6:** $T_A$ = 25°C, $V_S$ = ±15V, $V_{CM}$ = 0V, unless otherwise noted.

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

$T_A$ = 25°C, $V_{CC}$ = ±15V

| | ENDPOINT LIMIT | | DELTA | | |
|---|---|---|---|---|---|
| PARAMETER | MIN | MAX | MIN | MAX | UNITS |
| $V_{OS}$ | -175 | 175 | -100 | 100 | µV |
| $+I_{IB}$ | -4.5 | 4.5 | -1.5 | 1.5 | nA |
| $-I_{IB}$ | -4.5 | 4.5 | -1.5 | 1.5 | nA |

TABLE IV: ELECTRICAL TEST REQUIREMENTS

| MIL-STD-883 TEST REQUIREMENTS | SUBGROUP |
|---|---|
| FINAL ELECTRICAL TEST REQUIREMENTS (METHOD 5004) | 1*, 2, 3, 4, 5, 6 |
| GROUP A TEST REQUIREMENTS (METHOD 5005) | 1, 2, 3, 4, 5, 6 |
| GROUP B AND D FOR CLASS S ENDPOINT ELECTRICAL PARAMETERS (METHOD 5005) | 1, 2, 3 |

*PDA APPLIES TO SUBGROUP 1.

PDA TEST NOTE: The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1 and delta rejects after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.