

Signal Conditioning for High Impedance Sensors

By Glen Brisebois

ABSTRACT:

Dealing with high impedance sources and maintaining high impedance inputs without compromising reliability has its own set of challenges. This paper offers qualitative and quantitative discussions of issues associated with high impedance circuits, what types of sensors are high impedance, and what devices are available for buffering and protecting high impedance circuits. An application is discussed in which going higher impedance helps.

1 – Introduction

If I had the option, I wouldn't use high impedance sensors. They are so easily affected by external noise, solder flux residue, particle tracking, bias currents, and distant charges, that it can be difficult to get repeatable results. High impedance sensors have some upsides though – they don't self load, and they are inherently low power. For quantifying properties such as pH, light, acceleration, or humidity, the most practical sensors available are high impedance. Nature offers them so expediency urges that we utilize them. With careful attention to design, their tendency to be adversely affected by the world around them can be drastically reduced. As an interesting note about impedance, with the advent of practicable superconduction, impedance has an infinite achievable range. Of what else can that be said?

2 – Reference Resistors and the Fear of High Impedance

Any circuit looking into a high impedance sensor should be characterized with a high impedance source, so every engineer should have some high value reference resistors available. Vishay Techno offers surface mount resistors to 50G Ω , with samples in 1G and 2G values available off the shelf (when last I checked). I also have some very nice leaded 10G Ω and 100G Ω resistors in the "Mini-MOX" series from Ohmite (www.ohmite.com). What is amazing about these ridiculously high value resistors is that they are actually quite "stiff". For example, I was warned not to touch the resistor body lest the deposits from my skin oil "reduced the impedance", and this compelled an experiment. Applying a Keithley Model 614 electrometer across the resistor leads resulted in a meter reading of 9.9 to 10.0 G Ω . I proceeded to thoroughly touch and squeeze the resistor body from lead to lead with my oily fingers, and then backed away. The meter returned to precisely where it had been, 9.9 to 10.0 G Ω . But this shows only that my human oils are not an immediate threat to these particular reference resistors. Sound laboratory methodology would still exhort cleanliness of components, pcb's, and insulators to ensure reliability over time and humidity. Skin oil conductivity is known to vary among humans. For cleaning, Ohmite recommends isopropyl alcohol and lint free wipes and a 75C bake for 1 hour to drive off moisture.

When performing an impedance measurement like this, bear in mind that the insulator in the cable is entirely in parallel with the resistor under test. To maintain a 1% accuracy on a 100G resistor measurement requires an overall insulator impedance of no less than 10TΩ. The only way around this limitation is to perform an open circuit calibration so that any shunt resistance can be measured and calculated out. The Keithley 614 does not have this feature, but still performs well. This reinforces the fact that, compared to an insulator, a 10G resistor is indeed relatively stiff.

3 – The Enemies of High Impedance Circuits

Impedance is high when leakages, current noises, bias currents, and static voltage dominate the errors. So dealing with high impedance circuits means minimizing those quantities. The most common and addressable form of leakage is that due to solder flux residue. Boards supporting high impedance circuits should be well cleaned so that all flux is removed. Third party board manufacturers can have contaminated washers, so a clean wash may need to be specified as a production requirement. Traces should be spaced beyond the minimum design rules as real estate allows. For insulators, I have never found FR-4 to cause any problem, although it does absorb moisture while Teflon and glass do not. Some designers have had recourse to Teflon posts or wells, but this may be due to their inherent resistance to surface tracking and other effects such as dielectric absorption, rather than their purely insulative properties. To keep surface impedances high in imperfect environments may require sealing or conformal coating, but this can reduce serviceability. Traces connected to high impedance sources and inputs should be guarded by traces at similar potentials. There are many practical considerations. For example, a dual opamp has non-inverting inputs at pins 3 and 5. It is easier to protect pin 5 because it is in the corner, while pin 3 is adjacent to the negative supply.

Bias current and current noise in active devices are sources of error. Bipolar transistors require a DC base current in order to operate. FETs have input leakage. In both cases, a current noise is induced due to electron quantization through junctions. (Note that this is not true for current generally, but for currents through junctions.) For FETs, current noise rises with frequency because of Miller effects (see sidebar). While the temptation is to jump immediately to FET based input structures for their low bias currents, there are instances where super-beta bipolar input structures offer an advantage, particularly operating at high temperatures. FET input leakage doubles every 10 C, while superbeta bias current remains relatively stable. In either case, chopping techniques can be applied to remove the effects of both offset voltage and bias current. For impedances below a few MΩ, don't jump immediately to a FET input amplifier without first considering exceptionally precise and low bias current opamps like the LT6010, or LTC2054. Sometimes a better offset voltage can help defray a slightly worse bias current specification. For a given source impedance, the overall input error will be $V_{os} + I_{bias} \cdot R_{source}$. As source impedance rises, the bias current term dominates making a MOSFET input solution more attractive. This has become truer in recent years as the specifications of CMOS opamps have been improved.

Another fascinating problem encountered with high impedance circuits is their sensitivity to motion. Static charges generated by shoes on a carpet can be at kilovolt levels, so even

the tiniest capacitive coupling generates significant charge injection. When taking measurements, stand back and hold still. Shielding helps of course, but mechanical vibrations will modulate the capacitance (microphonics) between pcb traces and any local metalwork and cause charge injection. This is true even if the metalwork voltage itself is not changing, but simply at a different DC voltage than the traces. So shield your circuit, but not too closely. When mechanical motion or stress induce voltages on insulators at microscopic levels, they are usually referred to as triboelectric or piezoelectric effects. High impedance sources may require the use of low triboelectric noise cable, such as Belden type 9239 in high vibration environments.

4 – Device and Amplifier Considerations

Discrete MOSFETs offer poor leakage specifications, but in fact they can outperform their specifications by up to six orders of magnitude. The familiar 2N7002 for example specifies channel leakage of 1uA max and gate leakage of 0.1uA max. But looking at these devices in the lab with 20V on the drain and a grounded gate and source, you will find a total combined leakage of only about 1pA! Obviously the specifications are not reflective of what the device does, but rather of the cost of production test time and resolution. Better specifications require more test time and better test equipment, so you'll pay for it. Of course better specifications will also eventually impact yield.

Ultra low leakage matched pair JFETs are available from Linear Integrated Systems (<http://www.linearsystems.com>) in their LS830, and from InterFET (<http://www.interfet.com>) in their IFN424. My favorite single JFET is the Philips BF862 for its 3pA gate current, its sub nanovolt noise density, and its easy-to-deal-with -0.6V pinchoff voltage. The 2N4416 is also popular, especially for its sub-picoFarad input capacitance and respectable noise density, but it has that large and wildly variant pinchoff voltage (2V – 6V!) that has been the bane of the JFET world.

CMOS opamps have been available for many years, but the specifications have been poor and the actual results even worse. Linear Technology has historically avoided making CMOS opamps, but has just introduced two very good ones – the (precision micropower) LTC6078 and the (higher speed) LTC6241. The LTC6241 offers an input leakage current of 4pA at 70C, guaranteed under 75pA. There have also been JFET input based “electrometer grade” opamps on the market for many years, but these are relatively expensive. In the end, no opamp or semiconductor device is perfect, so the best DC results are achieved with relays and calibrating or chopping techniques.

The circuit of Figure 1 is one example, incorporating two instances of a force-balance nulling technique. To follow the operation, assume all the switches are open, then close S2 and S3. This engages ultra-precision integrating amplifier A2, forcing A1's output to ground. A1's input offset appears at its +input, and 101 times its offset is stored on C1. Opening S3 allows A1 to function normally again, but with 1uV of effective offset and a drift of about 1uV/second. Now, opening S2 puts feedback resistor R1 in circuit and causes an output voltage equal to $I_{bias} * R1$ – typically 1mV. Closing S4 and S5 nulls A1's output again, but this time through A3. A1's bias current is delivered now through

R2, and stored as a voltage on C2 at 60mV/pA. Opening S4 ends the nulling phase and closing S1 connects the input drive, shown in this case as a resistor under test (RUT) and a voltage source. But while the amplifier is now near perfect, it will not be for long. Drift on capacitors C1 and C2 will require a new nulling phase within several seconds or the amplifiers specifications may degrade beyond those of an unaided LTC6241. Figure 2 shows a much simpler method. Rather than trying to perfect the amplifier, this circuit instead chops the excitation so that the amplifier contributions can be subtracted out. Also, the RUT has been moved to the feedback path so that the output is proportion to RUT resistance rather than RUT admittance. Rise time was measured at 10ms (10-90%) with a 1G Ω RUT, so excitation should be no faster than about 10Hz to ensure adequate settling.

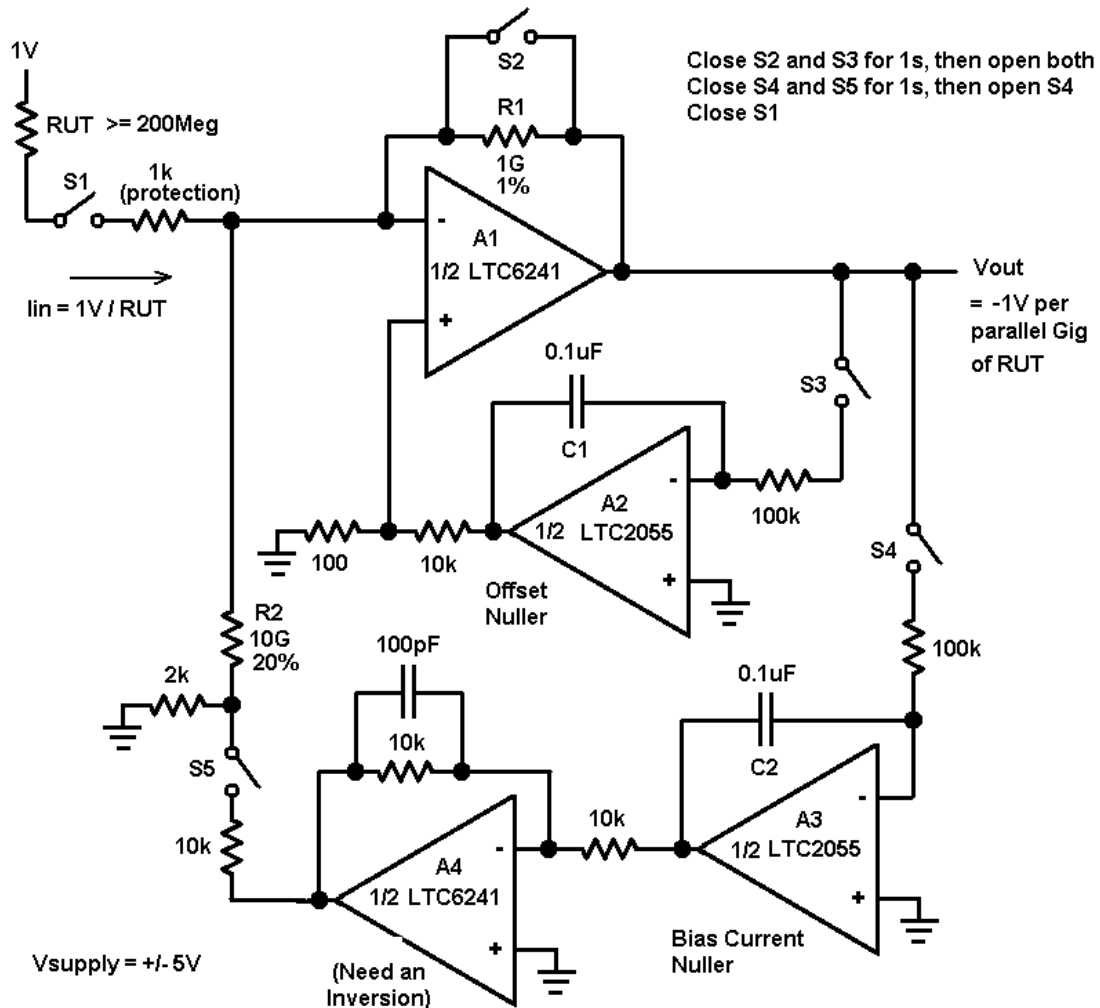


Figure 1: Using nulling techniques is tempting, and can be made to work with much effort and shielding. But making a “perfect” amplifier like this get expensive and departs from the high reliability of solid state. You may be bankrupt before getting into production.

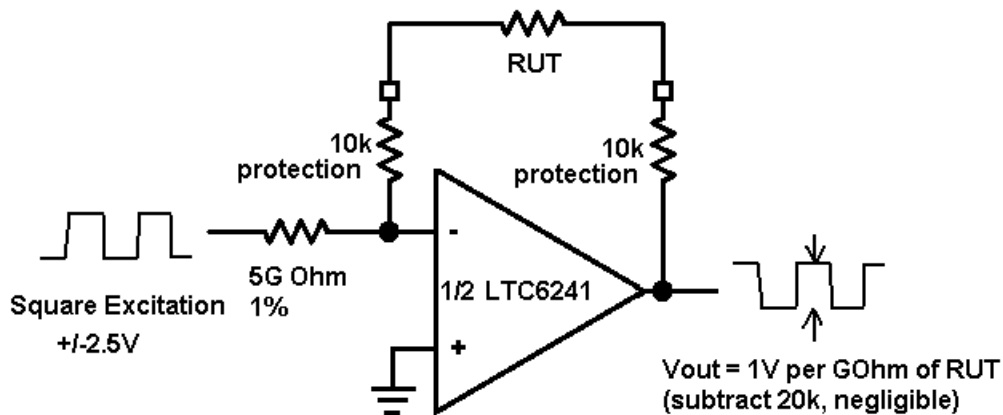


Figure 2: Similar accuracy can be achieved much more easily with chopped excitation techniques. Here the amplifier's characteristics are not enhanced but rather measured and subtracted. What are the opamp offset and bias current? It doesn't matter much.

5 - Protecting a High Impedance Circuit

But how can you protect a high impedance circuit without affecting its input impedance? Well, strictly speaking you can't, but you can come close. One of the best ways is to use a series resistor and some series inductance, even if it's just a length of trace. The inductance and parasitics will spread out an ESD pulse and improve the odds that it will jump to chassis before it gets to anything sensitive. You can further improve those odds by introducing a spark gap in the layout near the connector pin to be struck. This is cheap and effective, but it can cause problems in higher density digital designs. The spark gap re-emits a strong EMI wave (including some nice eerie blue), and I have seen this crash an on-board but distant '486 repeatably. Fortunately the hardware was unharmed, so it depends on what level of immunity is specified for the design. In our case this was a failure, as PC reset interventions were not allowed. For analog designs or simple digital designs spark gaps should not be a problem. Gas discharge tubes are also available as components.

Pretty much anything you do with diode clamps will cause leakage effects. Schottkys will probably be out of the question, as they tend to be leakier. Ultra-low leakage diodes are available such as the CMPD6001 series from Central Semiconductor (<http://www.centralsemi.com>), and the BAS416 from Philips (<http://www.semiconductors.philips.com>). But the maximum leakage specifications are actually quite high: 500pA to 5nA, and that's at cold. The hot specifications are even worse, often running into microamps. For the lowest leakage, JFET junctions still outperform diodes. The 2N4393 leaks typically 5pA at room and 3nA at 100C, and is available from Vishay in a SOT-23 package. Compare this to the maximum specified

bias current of 75pA at 70C for the LTC6241. Adding even good diodes or JFETs can cause a significant degradation. Some design work can help offset this problem however. For example, consider the Tracking limiter circuit shown in Figure 3. The diodes are back biased by A2 with the average DC voltage stored on C1. Overvoltages and spikes will be shunted to the reservoir capacitor, but the DC is allowed through (with unity gain). This protects the inputs, and also improves input overload recovery time. Where DC gain is desired, simply short C1 and move the input of A2 to the inverting input of A1. Inverting circuits are easier to protect because the diodes can simply be taken to ground.

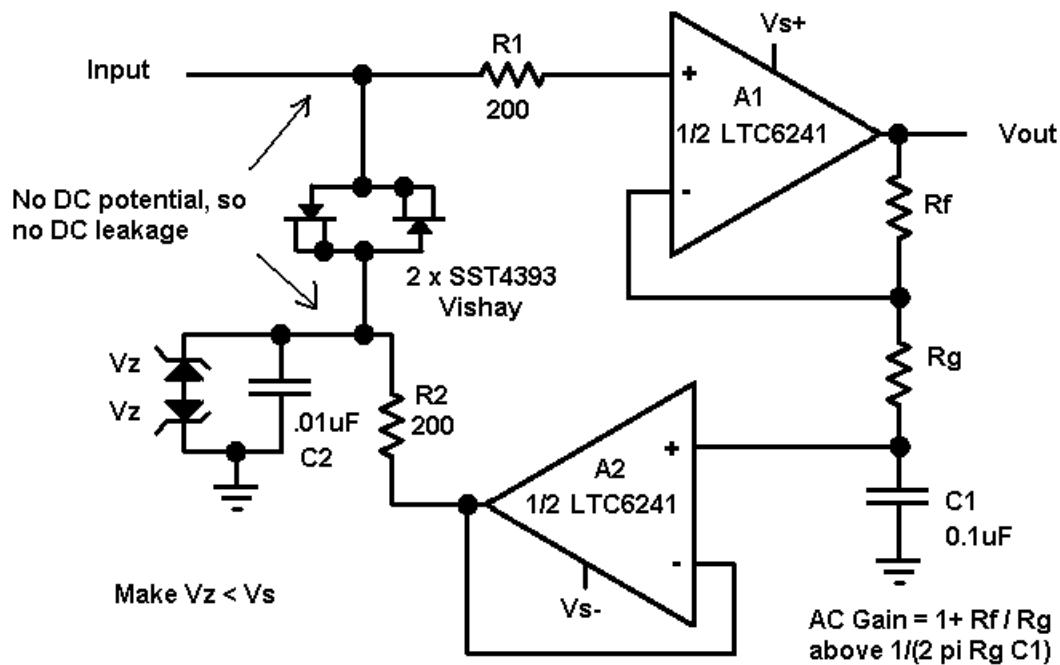


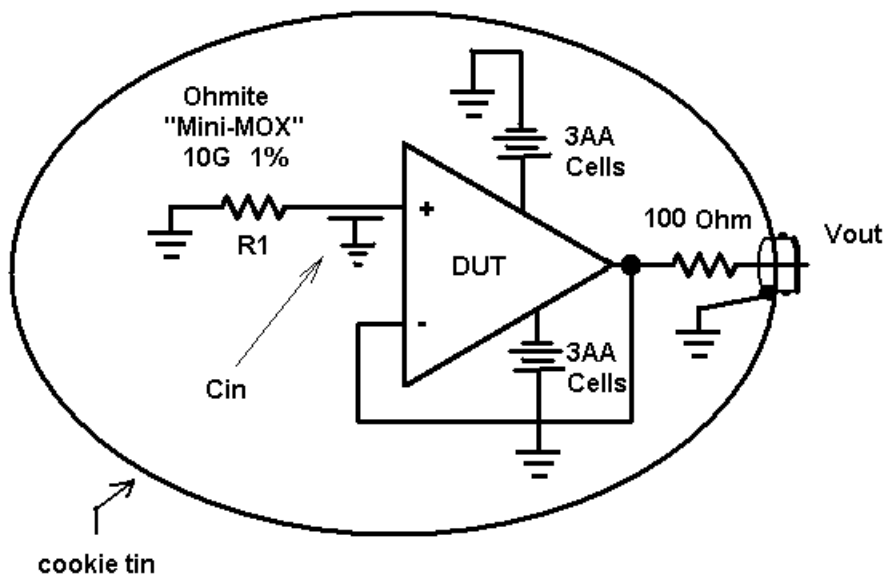
Figure 3: Tracking clamp has JFETs as protection diodes, but A2 back-drives these to the same voltage as the input. The zener and its capacitor carry most of the clamp current. R1 and R2 keep current away from the amplifiers.

6 – Sidebar: Current Noise Measurements

Measuring something is easy when there is lots to measure, and difficult when there's little to measure. Good FETs have very little current noise, especially at low frequency, and that makes it inherently difficult to measure. At high frequency, FET input current noise rises due to either Miller effects in the drain or tail current noise blowing back through the gate-source capacitance, depending on circuit topology. The fact that there is more current noise at high frequency would make it easier to measure, but for the fact that bandwidth rolls off in any practical high impedance circuit.

For the low frequency measurement, simply configure the opamp (I'll limit my discussion to opamps for simplicity) as a unity gain buffer with a 10G source resistor to ground, as shown in Figure 4. Use batteries and enclose the circuit in a cookie tin with a BNC through connector to access the output. Measure the output DC voltage and make sure that it's reasonable given the opamp's typical specified bias current ($I_{bias} = V_{out}/10G\Omega$). If it looks reasonable, then make a note of the measured value. (If it's not an LTC opamp, you may have to correct for offset voltage first.) Now look at the low frequency output content, using a spectrum analyzer. Make sure you are looking below the rolloff of the input circuit. An input capacitance of 3pF acting on a 10G source will cause a lowpass rolloff 3dB down at 5.3Hz. Below that frequency, and using averaging because noise is noisy, you should be able to see the 13uV/ $\sqrt{\text{Hz}}$ (at room temperature) noise density of the 10G resistor take shape, as in Figure 5. Properly functioning and shielded, any additional output noise is due to input current noise acting on the 10G source, because the amplifier's input voltage noise is relatively miniscule.

This single plot of output noise gives us two measurements: low frequency input current noise and input capacitance C_{in} . The low frequency input current noise is derived from the 13.6uV/ $\sqrt{\text{Hz}}$ output noise density measured at 0.22Hz (Figure 5, DUT is LTC6241). Subtracting the expected 13uV/ $\sqrt{\text{Hz}}$ resistor noise RMS-wise leaves a net 4uV/ $\sqrt{\text{Hz}}$ [$\sqrt{13.6^2 - 13^2} = 4$] attributed to opamp current noise. Dividing the 4uV/ $\sqrt{\text{Hz}}$ by 10G arrives at an input current noise measurement of 0.4fA/ $\sqrt{\text{Hz}}$. This number can be compared with the expected theoretical current noise density of $\sqrt{2 \cdot q \cdot I_{bias}}$, where q is the electron charge 1.6e-19 Coulombs, and I_{bias} is the bias current measured above. The input capacitance C_{in} can be derived from the -3dB point of 4.3Hz shown in the same plot. The -3dB point occurs at $C_{in} = 1/2\pi \cdot R \cdot f$, where $R = 10G\Omega$ and $f = 4.3\text{Hz}$, giving us $C_{in} = 3.7\text{pF}$.



Low Frequency Current Noise Measurement Circuit

Figure 4: Simple circuit for measuring low frequency current noise. The 10G resistor contributes $13\mu\text{V}/\sqrt{\text{Hz}}$ and this is buffered to the output. Extra noise seen at the output is due to current noise $\times 10\text{G}\Omega$. The same circuit without modification also yields the input capacitance C_{in} . Supply noise and interference are eliminated by powering on batteries inside a cookie tin.

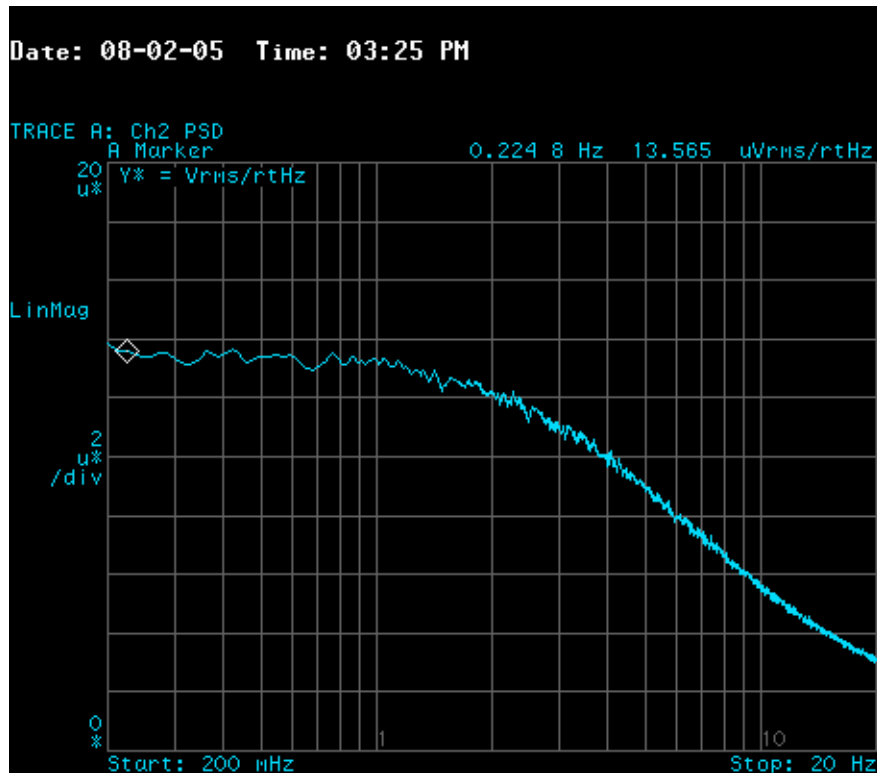


Figure 5: Output noise spectrum of the circuit of Figure 4 (averaged for 27 Hours). The resistor contributes $13\mu\text{V}/\sqrt{\text{Hz}}$, with the additional $0.6\mu\text{V}/\sqrt{\text{Hz}}$ coming from the $0.5\text{fA}/\sqrt{\text{Hz}}$ of the LTC6241 working into the $10\text{G}\Omega$ source (adding RMS wise). Response is -3dB at 4.3Hz , indicating a total input capacitance of 3.7pF including all parasitics.

Using the same circuit, but looking at higher frequency, you can also see the effect of the rising current noise – Figure 5a. Note that the output voltage noise goes flat at high frequency. This is because although the current noise is rising, it is looking into the input capacitance which has falling impedance with frequency. So the product is flat. At 100kHz the 3.7pF input capacitance looks like $430\text{k}\Omega$. So the $50\text{nV}/\sqrt{\text{Hz}}$ output noise divided by $430\text{k}\Omega$ must be due to $116\text{fA}/\sqrt{\text{Hz}}$ of input current noise at 100kHz . We can now plot the input current noise as a function of frequency (thus far measured only at the +input) as in Figure 5b. At low frequency it is a flat $0.4\text{fA}/\text{rtHz}$, rising at a rate of $116\text{fA}/\text{rtHz}$ per kHz at high frequency. (Or put in more fundamental units, the rate of rise of current noise with frequency is $1.16\text{attoAmps}\cdot\text{Hz}^{-3/2}$).

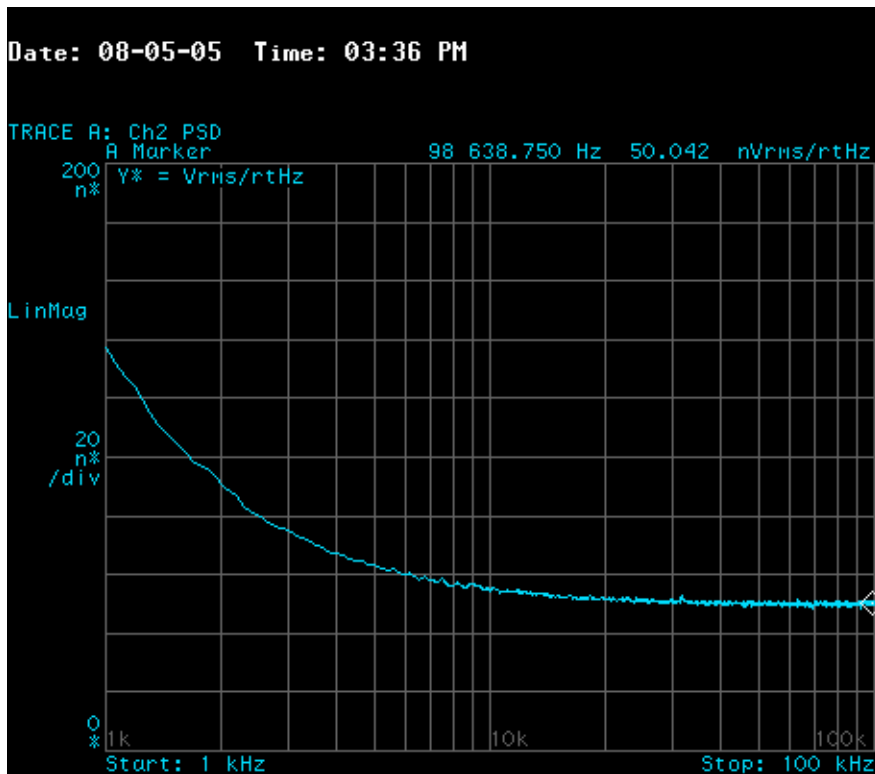


Figure 5a: High Frequency Output noise spectrum of the circuit of Figure 4. The current noise is rising with frequency, but the input capacitance impedance is falling with frequency. Combined effect is flat output noise at high frequency. At 100kHz the 3.7pF input C looks like 430k Ω . The 50nV/ $\sqrt{\text{Hz}}$ output noise shown here thus implies a 116fA/ $\sqrt{\text{Hz}}$ input current noise at 100kHz.

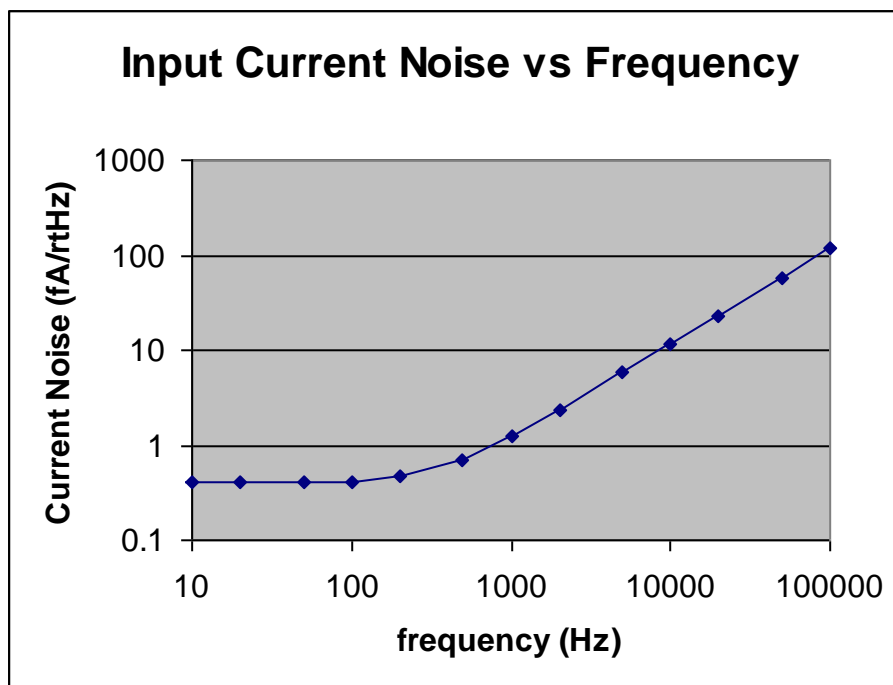


Figure 5b: Input Current Noise vs Frequency for +input of the LTC6241, calculated from Figures 5 and 5a. Current noise is flat at low frequency, and rises 116fA /rtHz per kHz. Entire plot is gleaned from one circuit, without modifications.

But for the high frequency case many engineers prefer to have a test circuit that is closer topologically to the intended application circuit. A transimpedance circuit is most commonly employed because it is the most frequent application circuit for low current noise high impedance circuits (usually applied to photodiodes). Refer to Figure 6. This circuit emulates a transimpedance photodiode amplifier with C2 taking the place of a 1.5pF photodiode and C1 being a short circuit at high frequency. The bandwidth rolls off due to the combination of finite opamp gain bandwidth and the noise gain of the R2:C2 feedback network increasing with frequency. This is much more complicated than the single RC input encountered previously! Fortunately the current noise rises with frequency, which is usually undesirable except when trying to measure it. Figure 7 shows the circuit's raw output noise spectrum with V_{in} open. The flat region at left is dominated by the 20M resistor noise at $582\text{nV}/\sqrt{\text{Hz}}$, and the noise figure there is very near 0dB. The noise clearly rises with frequency, but this could be due to either rising current noise or to voltage noise and rising noise gain. A quick calculation can help decide if either one is dominating, but first we should perform a gain calibration with frequency. R1 and C1 provide the window for excitation and thereby a gain measurement.

At a glance the whole circuit of Figure 6 is an integrator followed by a differentiator, so it should have flat response. In fact, at low frequencies response rolls off because the R1:C1 integrator has no gain. But we're not interested in low frequencies. At frequencies well above $R1 \cdot C1$, the current through C2 goes constant with frequency (as with an ideal photodiode) and the gain does indeed go flat as shown in figure 8. The midband gain factor is $R2 \cdot C2 / R1 \cdot C1$, or about 30mV out per 1V excitation in. This is easy to confirm in the lab, and with an accurate measurement the component tolerances become unimportant and the measured gain (attenuation in fact) can be normalized. At still higher frequencies, the differentiator starts to have bandwidth trouble due to the finite gain bandwidth of the opamp and the noise gain of the circuit, and the parasitic capacitances around R2. The result is that the gain drops with frequency – but we knew it would and that's why we're measuring it.

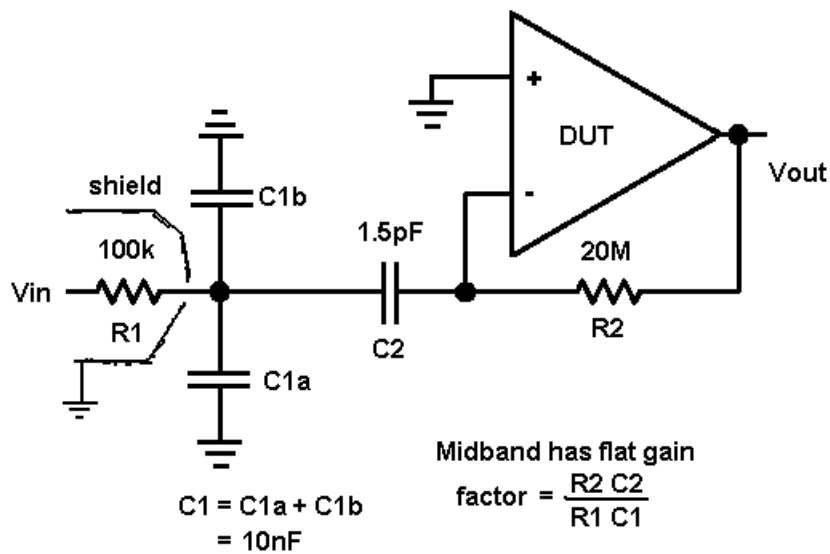
The important thing is that the output noise is measured with exactly the same circuit as the gain, including the opamp and the parasitics, but with the excitation removed. Taking the resulting output noise vs frequency data and dividing by the normalized gain vs frequency data yields a bandwidth-corrected version of output noise as if the opamp had infinite gain bandwidth and the feedback resistor had no parasitics. Some Signal Analyzers, such as the HP3562, do an excellent job of waveform divides and plot generation while maintaining correct units for this analysis. But unfortunately I don't have one and it is still confusing for novices anyway, so I offer a sample calculation instead. If you can perform the calculation at one frequency, eventually it becomes easy to perform them at all frequencies.

Again using an LTC6241 as the DUT, I measured a midband gain of 0.0290 at 4kHz (down from the nominal 0.030, probably due to C2 tolerance) as shown in Figure 8. At 100kHz, the gain has rolled off to 0.0212, or about 0.73 of the midband gain. We can now apply this gain correction to the noise measurement at 100kHz.

Refer again to Figure 7. At high frequency, the noise is rising even though the response is falling. At 100kHz, we measure $1.61\mu\text{V}/\sqrt{\text{Hz}}$ output noise. To correct for the gain rolloff, we divide by the 0.73 from the gain curve and get $2.20\mu\text{V}/\sqrt{\text{Hz}}$, still output referred. This would be the output noise with an infinitely fast opamp and no shunt capacitance around the feedback 20M. In order to refer this noise to the input, many TIA designers simply divide by the 20M feedback impedance, for a $110\text{fA}/\sqrt{\text{Hz}}$ input referred current noise.

But this neglects the fact that some of the output noise is due to input voltage noise. We need to perform the calculation mentioned earlier to determine which noise is dominant. The voltage noise of the opamp gets to the output multiplied by the noise gain. The LTC6241 input capacitance of 3.5pF ($C_{dm} + C_{cm}$) combines with C1 to make 5pF. Let's assume 1pF of additional parasitics for a total of 6pF. At 100kHz, this looks like $265\text{k}\Omega$. Noise gain is $1 + Z_f / Z_{shunt}$, or $1 + 20\text{M} / 265\text{k} = 76$. The input voltage noise of the LTC6241 is $7\text{nV}/\sqrt{\text{Hz}}$, so at the output it would contribute $76 * 7\text{nV} = 532\text{nV}/\sqrt{\text{Hz}}$. Subtracting this RMS-wise from the $2.20\mu\text{V}/\sqrt{\text{Hz}}$ gives $2.13\mu\text{V}/\sqrt{\text{Hz}}$. This is not an appreciable correction at all, but it does reduce the $110\text{fA}/\sqrt{\text{Hz}}$ current noise calculated above to $107\text{fA}/\sqrt{\text{Hz}}$.

When measuring an opamp's current noise in this way, it is critical to sift out the effects of voltage noise. The circuit of Figure 5 did not have this complexity because the voltage noise was swamped in all cases, the noise gain was a solid unity, and the bandwidth was uncompromised. So the fact that the two measurement techniques on two different devices on two different inputs yield current noise results within 10% of each other reveals that the opamp has a good symmetric input structure and repeatability device to device, and that the techniques are reliable. The odds are small that everything is haywire and we still managed to fool ourselves.



Gain Correction Test Circuit for High Frequency
Current Noise

Figure 6: High frequency current noise measurement circuit emulates a photodiode transimpedance amplifier with C2 replacing the photodiode. R1 and C1 are provided for high frequency gain calibration. C1 is a parallel combination to minimize parasitic inductance.

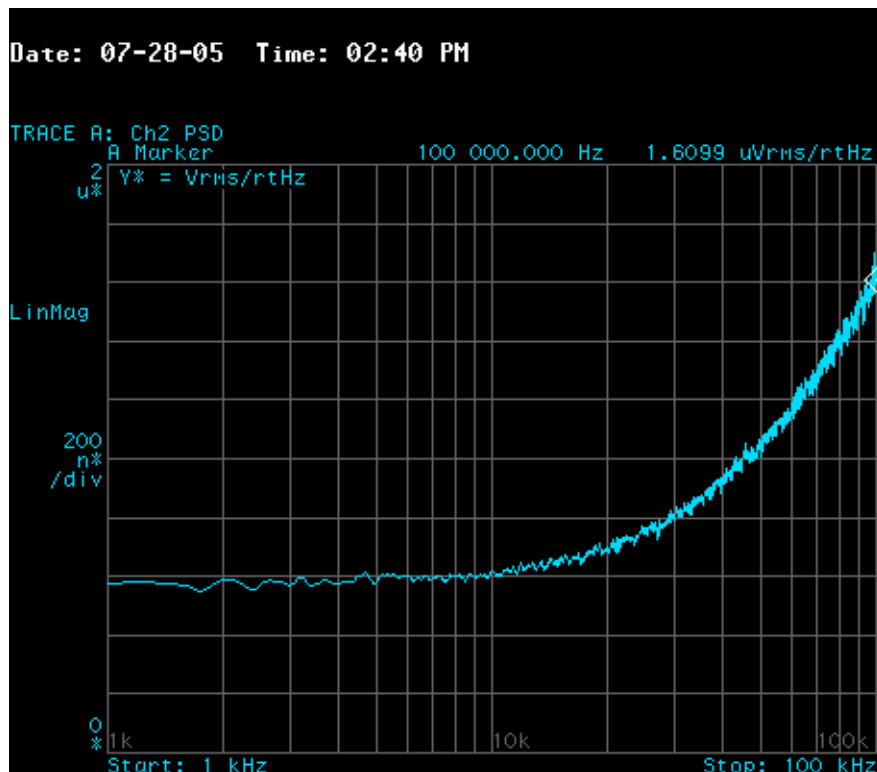


Figure 7: Output noise spectrum with Vin open circuited, showing 1.61uV/√Hz output noise density at 100kHz. To correct for the gain rolloff, we need the gain correction curve shown in Figure 8. Corrected output noise at 100kHz would be $1.61\mu\text{V}/\sqrt{\text{Hz}} / 0.73 = 2.2\mu\text{V}/\sqrt{\text{Hz}}$. To calculate input referred current noise, divide by 20MΩ to get 110fA/rtHz.

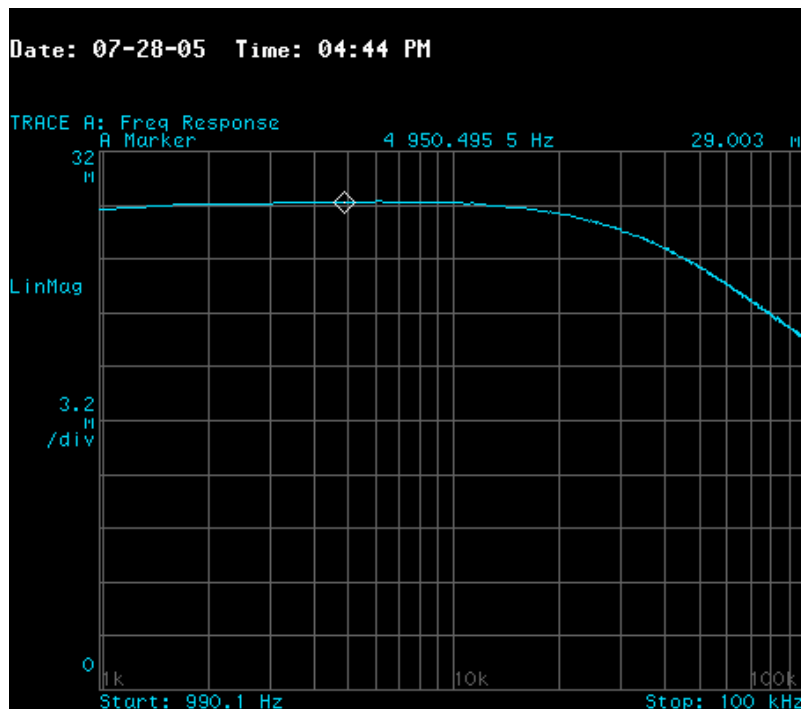


Figure 8: Gain vs frequency of the Circuit of Figure 6. Midband “flat” gain is 0.0290, rolling off to 0.0212 at 100kHz. This indicates a relative gain of 0.73 at 100kHz.

7 – Charge Amp Tradeoffs for Piezoelectric Accelerometers – How Going Higher Impedance Actually Helps

Figures 9 and 10 show two different approaches to amplifying signals from a capacitive sensor. The sensor in both cases is a 770pF piezoelectric shock sensor accelerometer, which generates charge under physical acceleration. Figure 9 shows the classical “charge amplifier” approach. The opamp is in the inverting configuration so the sensor looks into a virtual ground. All of the charge generated by the sensor is forced across the feedback capacitor by the op amp action. Because the feedback capacitor is 100 times smaller than the sensor, it will be forced to 100 times what would have been the sensor’s open circuit voltage. So the circuit gain is 100. The benefit of this approach is that the signal gain of the circuit is independent of any cable capacitance introduced between the sensor and the

amplifier. Hence this circuit is favored for remote accelerometers where the cable length may vary. Difficulties with the circuit are inaccuracy of the gain setting with the small capacitor, and low frequency cutoff due to the bias resistor working into the small feedback capacitor.

Figure 10 shows a non-inverting amplifier approach. This approach has many advantages. First of all, the gain is set accurately with resistors rather than with a small capacitor. Second, the low frequency cutoff is dictated by the bias resistor working into the large 770pF sensor, rather than into a small feedback capacitor, for lower frequency response. Third, the non-inverting topology can be paralleled and summed (as shown) for scalable reductions in voltage noise. The only drawback to this circuit is that the parasitic capacitance at the input reduces the gain slightly. This circuit is favored in cases where parasitic input capacitances such as traces and cables will be relatively small and invariant.

When you calculate the bias resistance required for the desired low frequency cutoff, consider that you may want to make the bias resistor still larger. This reduces the noise floor at low frequency. For example if we want to support frequencies down to 10Hz at -3dB, the bias resistor would work out to $1/2\pi \cdot 10\text{Hz} \cdot 770\text{pF} = 20\text{M}\Omega$. At 10Hz, the 20M resistor would contribute $580\text{nV}/\sqrt{\text{Hz}}$ of noise, and be 3dB down just like the signal. Making the resistor $1\text{G}\Omega$ as shown, it's $4000\text{nV}/\sqrt{\text{Hz}}$ voltage noise would be attenuated down to effectively $80\text{nV}/\sqrt{\text{Hz}}$ by the accelerometer capacitance, while the signal would barely be attenuated at all. Sometimes going higher impedance than conventionally required can actually help!

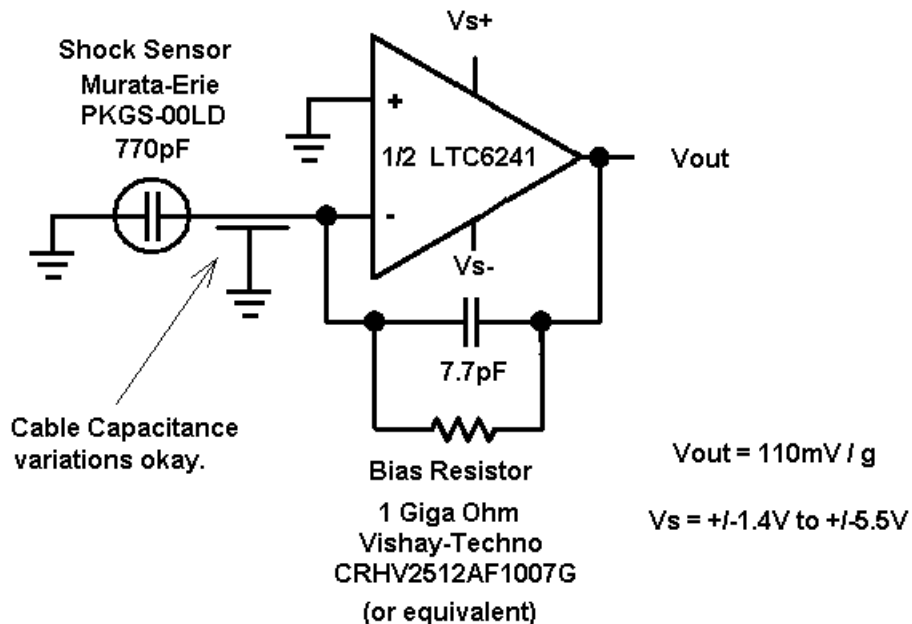
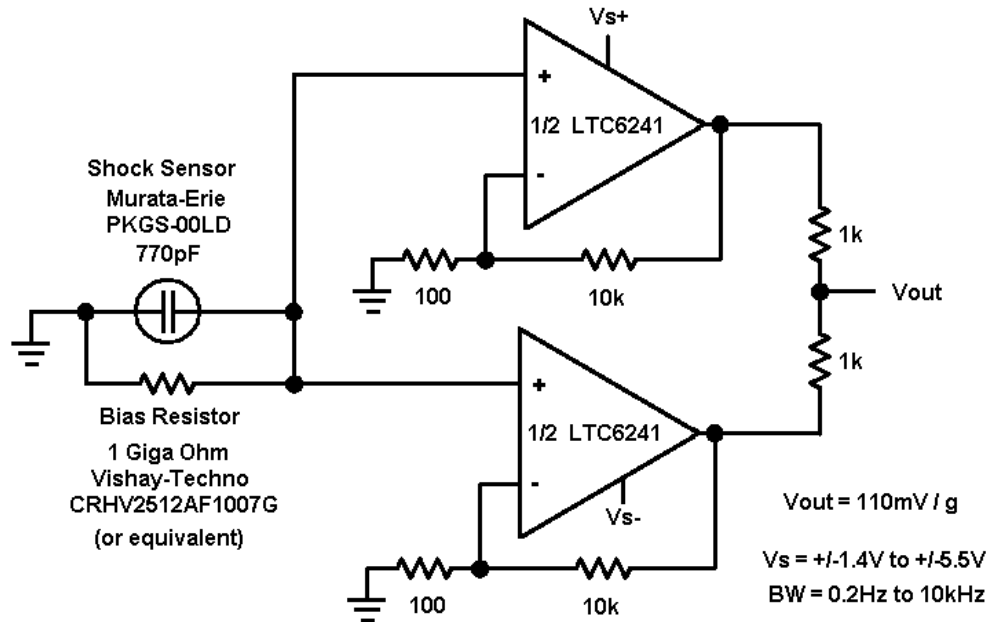


Figure 9: Classical Inverting Charge Amplifier. Variations in cable capacitance (ie length) do not affect the signal gain. Use this circuit when the accelerometer is remote from the amplifier and the cable length is unspecified. Drawbacks: Gain is set by the low valued feedback capacitor. Low frequency performance is set by the bias resistor working into the same.



Low Noise Shock Sensor Amplifier

Figure 10: Non-inverting Charge Amplifier offers several advantages. Stages can be paralleled for lower voltage noise. Bias resistor works into higher capacitance for better low frequency response.

Conclusion

Devices and materials are available to support and protect very high impedances. Dealing with high impedances requires a knowledge of what are otherwise miniscule phenomena. Sometimes quantization of these phenomena – such as current noise – can be challenging in itself. But with the right circuit techniques, measurements become meaningful and repeatable. A proper breakdown of error sources such as leakage, settling time, voltage noise and current noise, help the circuit designer to know what to expect, and to get it.

Acknowledgements

Peter Haak, of Holland, for his input on gain calibration during current noise measurements in transimpedance circuits.